

TC74LVX157F, TC74LVX157FN, TC74LVX157FT

Quad 2-Channel Multiplexer

The TC74LVX157F/ FN/ FT is a high-speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

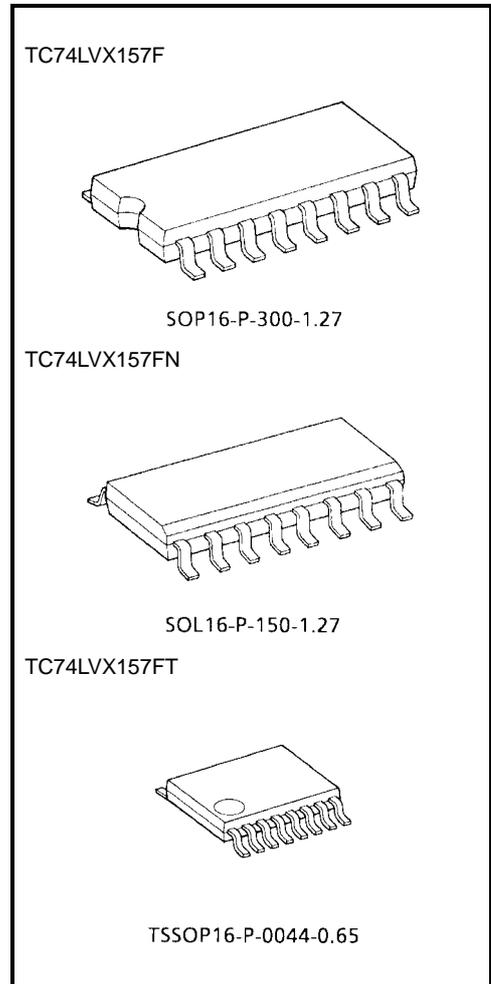
This device consist of four 2-input digital multiplexers with common select and strobe inputs. When the **STROBE** input is held H-level, selection of data is inhibited and all the outputs become L-level. The select decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

An input protection circuit ensures that 0 to 5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

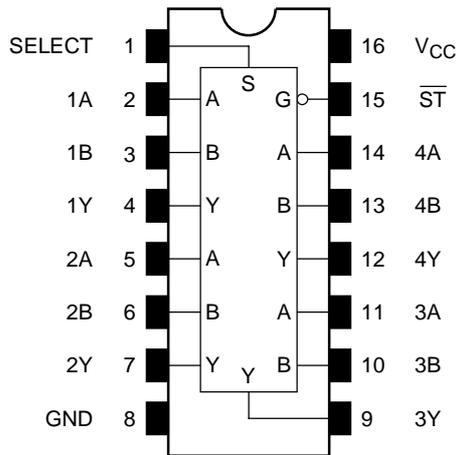
- High-speed: t_{pd} : $t_{pd} = 5.1 \text{ ns (typ.) (VCC = 3.3 V)}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A (max) (Ta = 25^\circ\text{C})}$
- Input voltage level: $V_{IL} = 0.8 \text{ V (max) (VCC = 3 V)}$
 $V_{IH} = 2.0 \text{ V (min) (VCC = 3 V)}$
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 0.5 \text{ V (max)}$
- Pin and function compatible with 74HC157

Note: xxxFN (JEDEC SOP) is not available in Japan.

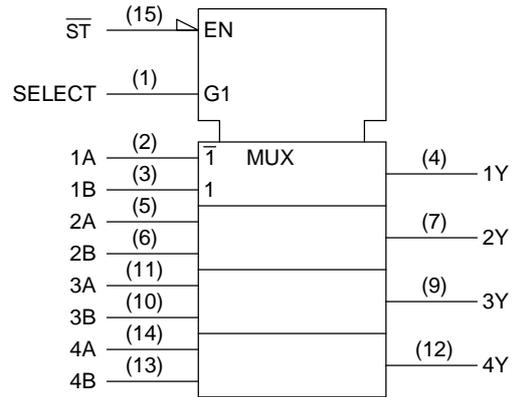


Weight
 SOP16-P-300-1.27: 0.18 g (typ.)
 SOL16-P-150-1.27: 0.12 g (typ.)
 TSSOP16-P-0044-0.65: 0.06 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol

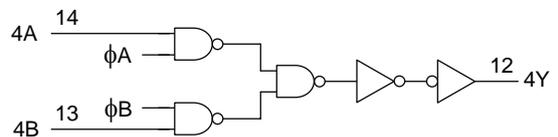
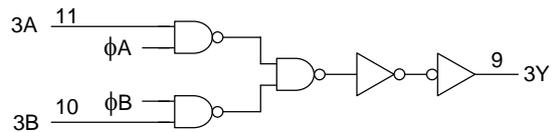
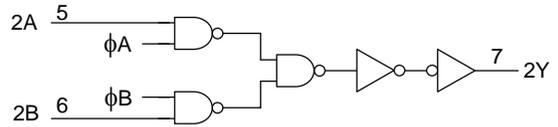
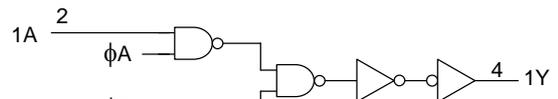
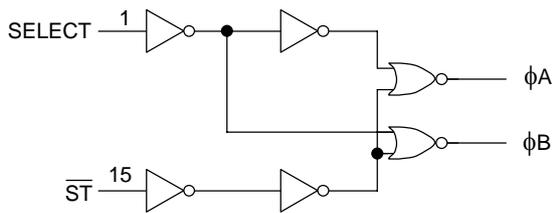


Truth Table

Inputs				Outputs
ST-bar	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don't care

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 100	ns/V

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
					V _{CC} (V)	Min	Typ.	Max	Min		Max
Input voltage	H-level	V _{IH}	—		2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	L-level	V _{IL}	—		2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				I _{OH} = -50 μA	3.0	2.9	3.0	—	2.9	—	
				I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0	0.1	—	0.1	
				I _{OL} = 50 μA	3.0	—	0	0.1	—	0.1	
				I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (A, B-Y)	t _{pLH}	—	2.7	15	—	6.6	12.5	1.0	15.5	ns
				50	—	9.1	16.0	1.0	19.0	
	3.3 ± 0.3		15	—	5.1	7.9	1.0	9.5		
			50	—	7.6	11.4	1.0	13.0		
Propagation delay time (SELECT-Y)	t _{pLH}	—	2.7	15	—	8.9	16.9	1.0	20.5	ns
				50	—	11.4	20.4	1.0	24.0	
	3.3 ± 0.3		15	—	7.0	11.0	1.0	13.0		
			50	—	9.5	14.5	1.0	16.5		
Propagation delay time (\overline{ST} -Y)	t _{pLH}	—	2.7	15	—	9.1	17.6	1.0	20.5	ns
				50	—	11.6	21.1	1.0	24.0	
	3.3 ± 0.3		15	—	7.2	11.5	1.0	13.5		
			50	—	9.7	15.0	1.0	17.0		
Output to output skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C _{IN}	(Note 2)		—	4	10	—	10	pF	
Power dissipation capacitance	C _{PD}	(Note 3)		—	20	—	—	—	pF	

Note 1: Parameter guaranteed by design.
 ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

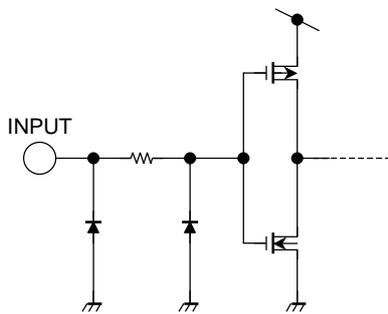
And the total C_{PD} when n pcs. of gate operate can be gained by the following equation:

$$C_{PD (total)} = 13 + 7 \cdot n$$

Noise Characteristics (Ta = 25°C, input: tr = tf = 3 ns, CL = 50 pF)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Limit	Unit
Quiet output maximum dynamic	V _{OL}	V _{OLP}	3.3	0.3	0.5	V
Quiet output minimum dynamic	V _{OL}	V _{OLV}	3.3	-0.3	-0.5	V
Minimum high level dynamic input voltage	V _{IH}	V _{IHD}	3.3	—	2.0	V
Maximum low level dynamic input voltage	V _{IL}	V _{ILD}	3.3	—	0.8	V

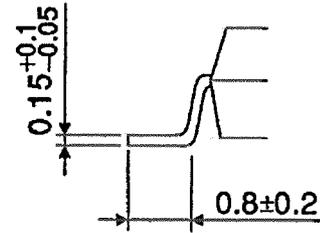
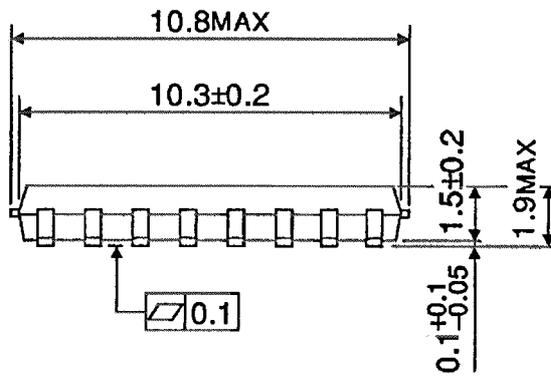
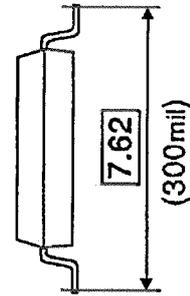
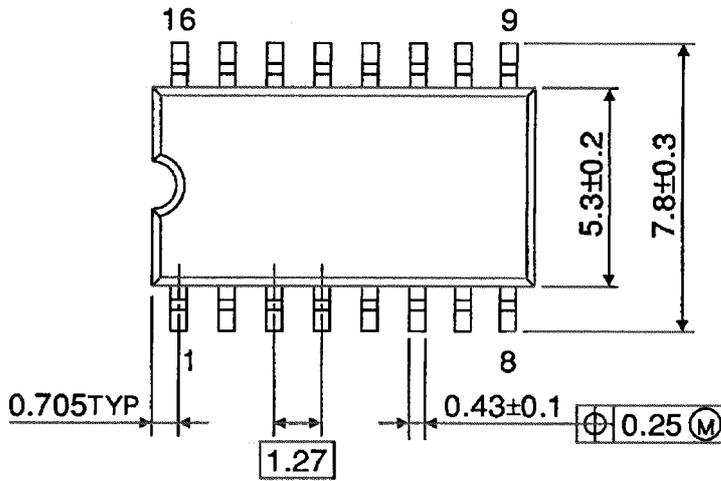
Input Equivalent Circuit



Package Dimensions

SOP16-P-300-1.27

Unit : mm

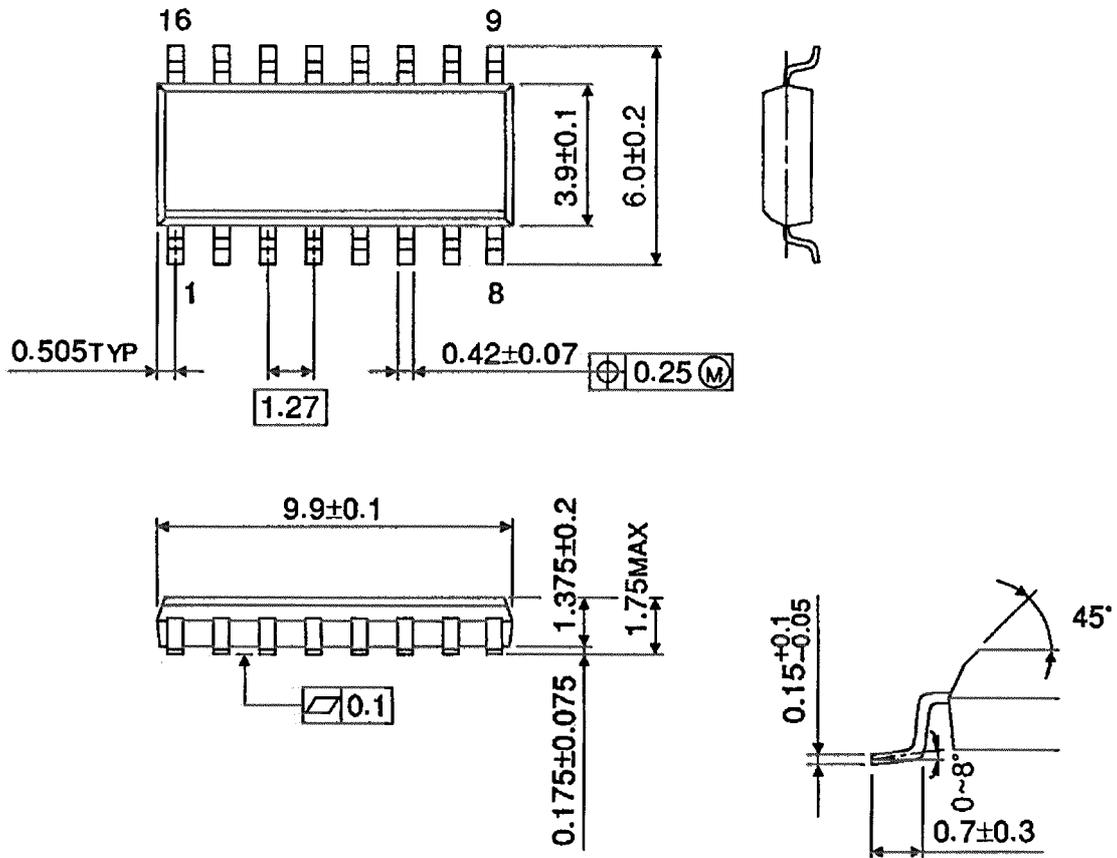


Weight: 0.18 g (typ.)

Package Dimensions

SOL16-P-150-1.27

Unit : mm

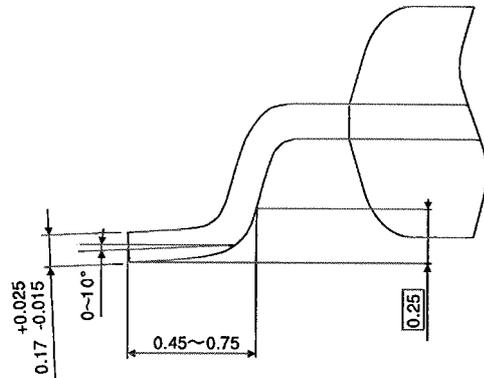
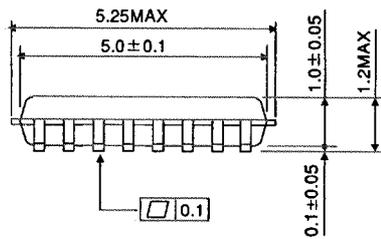
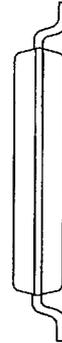
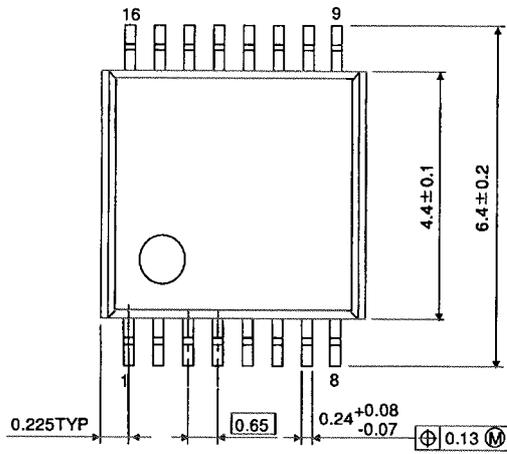


Weight: 0.12 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65

Unit : mm



Weight: 0.06 g (typ.)

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