SGS TDA 2006

LINEAR INTEGRATED CIRCUIT

10W AUDIO AMPLIFIER

The TDA 2006 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class "AB" amplifier. At ± 12V, d = 10% typically it provides 12W output power on a 4Ω load and 8W on a 8Ω. The TDA 2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA 2006 is pin to pin equivalent to the TDA 2030.

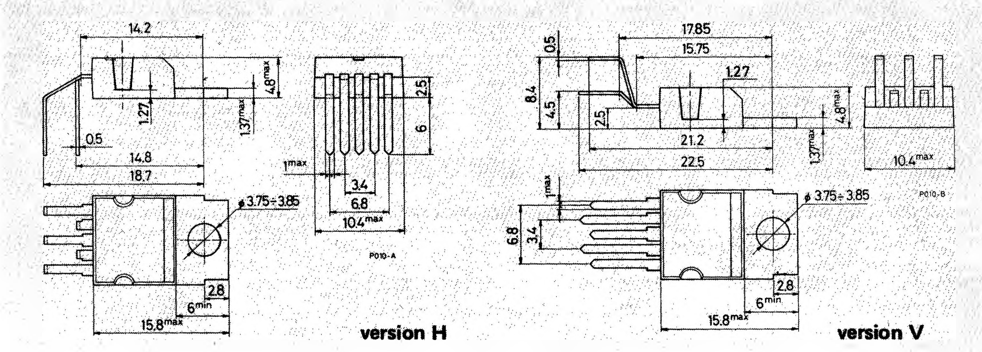
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 12	V
I_o	Output peak current (internally limited)	3	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

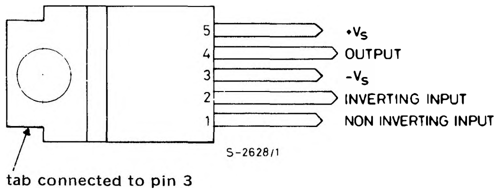
ORDERING NUMBERS: TDA 2006H; TDA 2006V

MECHANICAL DATA

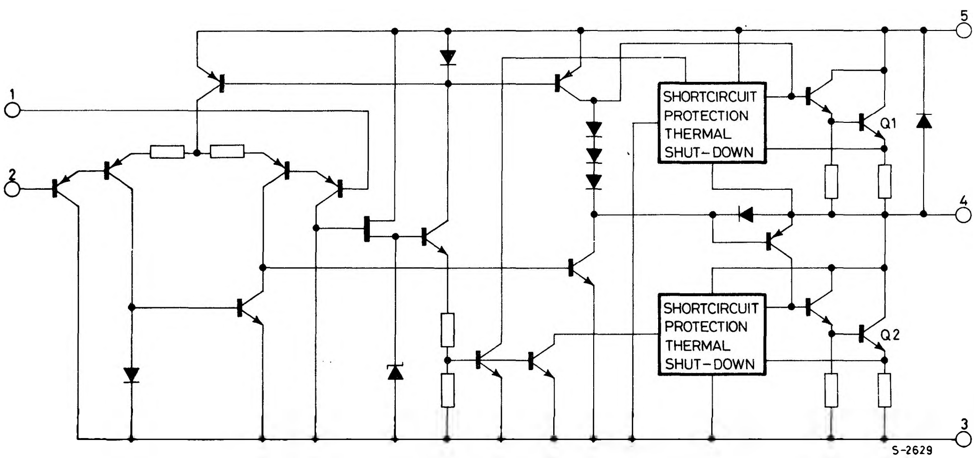
Dimensions in mm



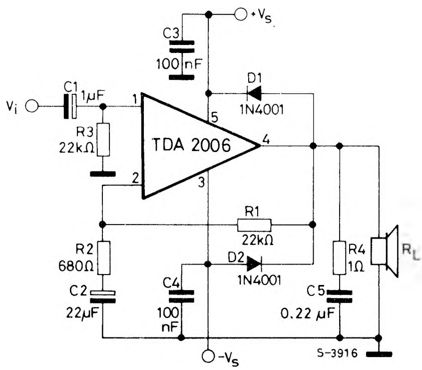
CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th\text{-}j\ case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s= ±12V, T_{amb}= 25°C unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 15	V
I_d	Quiescent drain current	V_s = ± 15V		40	80	mA
I_b	Input bias current			0.2	3	μA
V_{OS}	Input offset voltage			± 8		mV
I_{OS}	Input offset current			± 80		nA
V_{OS}	Output offset voltage			± 10	± 100	mV
P_o	Output power	d = 10% f = 1 KHz R_L= 4Ω R_L= 8Ω	 6	 12 8		 W W

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Units
d	Distortion	P_o= 0.1 to 8W R_L= 4Ω f = 1 KHz		0.2		%
		P_o= 0.1 to 4W R_L= 8Ω f = 1 KHz		0.1	1	%
V_i	Input sensitivity	f = 1 KHz P_o= 10W R_L= 4Ω P_o= 6W R_L= 8Ω		200 220		mV mV
B	Frequency response (-3 dB)	P_o= 8W R_L= 4Ω	10 to 140,000			Hz
R_i	Input resistance (pin 1)	f = 1 KHz	0.5	5		MΩ
G_v	Voltage gain (open loop)	f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	f = 1 KHz	29.5	30	30.5	dB
e_N	Input noise voltage	B (-3 dB) = 22Hz to 22kHz R_L= 4Ω		3	10	μV
i_N	Input noise current	B (-3 dB) = 22Hz to 22kHz R_L= 4Ω		80	200	pA
SVR	Supply voltage rejection	R_L= 4Ω R_g= 22 KΩ f_{ripple}= 100 Hz (*)	40	50		dB
I_d	Drain current	P_o= 12W R_L= 4Ω P_o= 8W R_L= 8Ω		850 500		mA mA
T_j	Thermal shut down junction temperature			145		°C

(*) Referring to fig. 15, single supply.

Fig. 1 - Output power vs. supply voltage

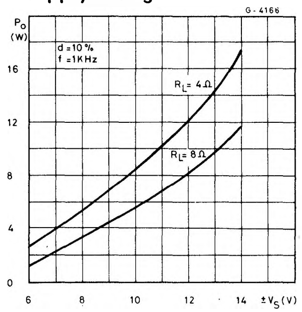


Fig. 2 - Distortion vs. output power

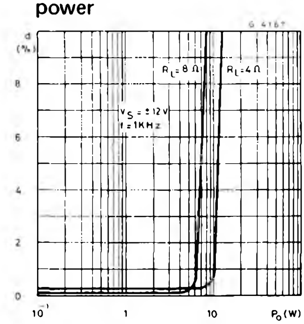


Fig. 3 - Distortion vs. frequency

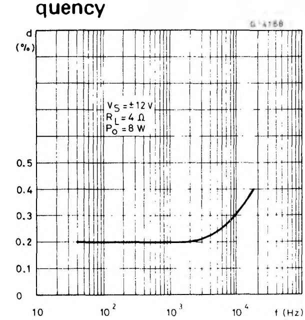


Fig. 4 - Distortion vs. frequency

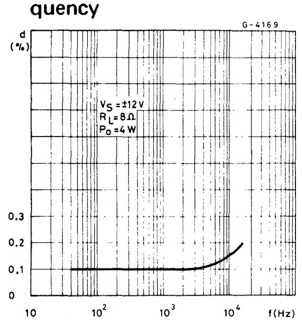


Fig. 5 - Sensitivity vs. output power

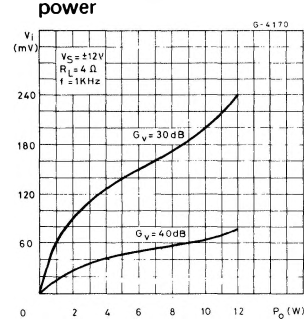


Fig. 6 - Sensitivity vs. output power

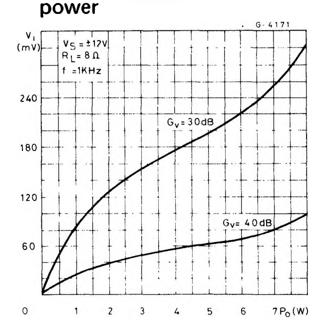


Fig. 7 - Frequency response with different values of the rolloff capacitor C_8 (see fig. 13)

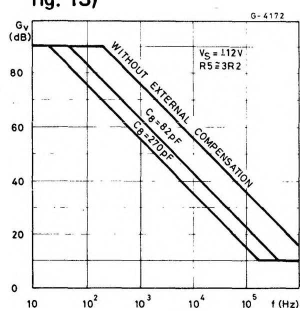


Fig. 8 - Value of C_8 vs. voltage gain for different bandwidths (see fig. 13)

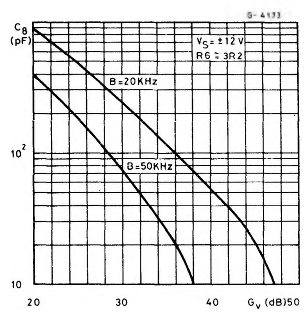


Fig. 9 - Quiescent current vs. supply voltage

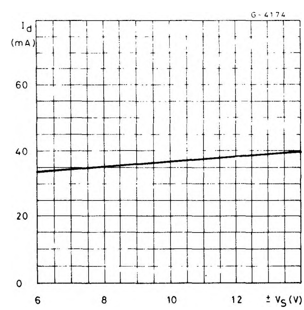


Fig. 10 - Supply voltage rejection vs. voltage gain

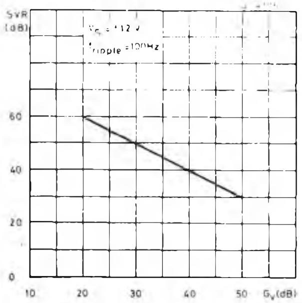


Fig. 11 - Power dissipation and efficiency vs. output power

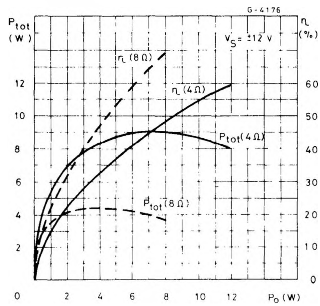


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)

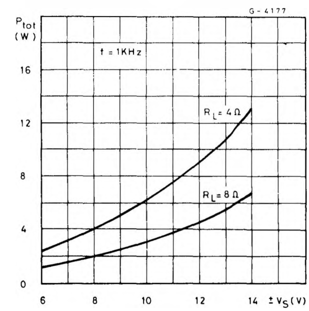


Fig. 13 - Application circuit with split power supply

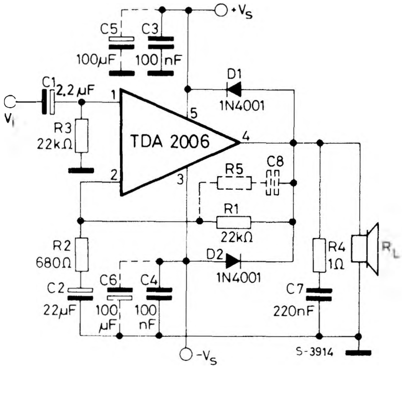


Fig. 14 - P.C. board and component layout for the circuit of fig. 13

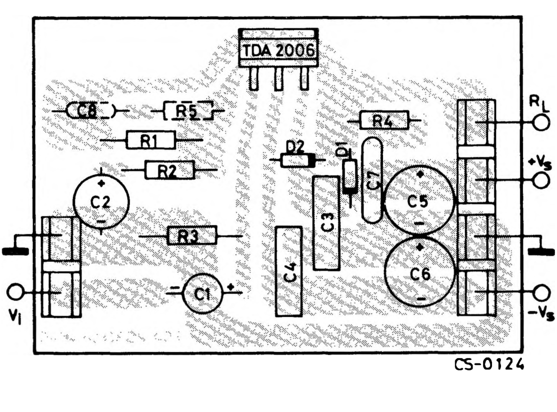


Fig. 15 - Application circuit with single power supply

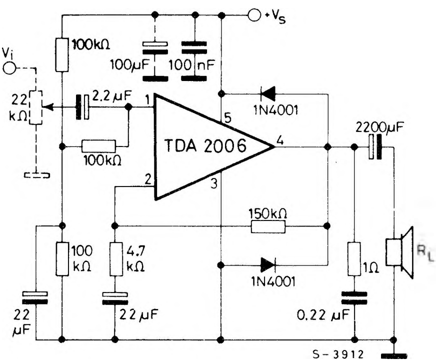


Fig. 16 - P.C. board and component layout for the circuit of fig. 15

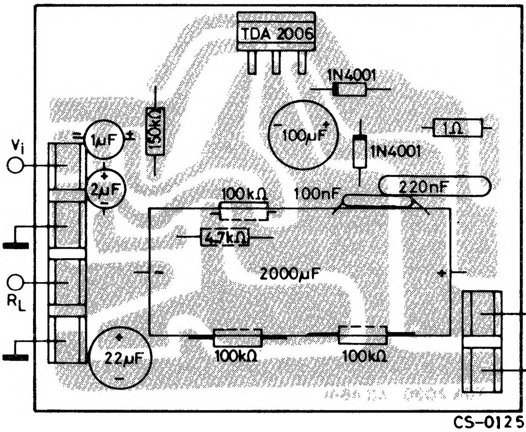
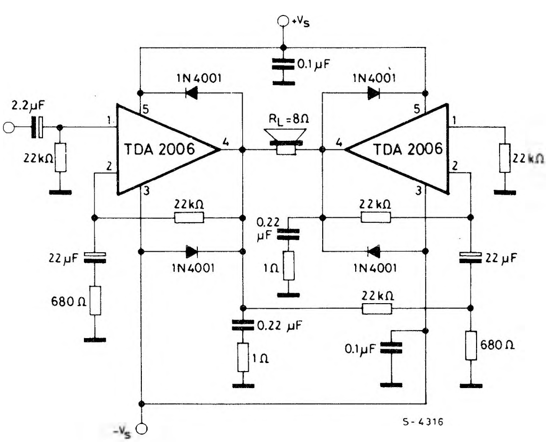


Fig. 17 - Bridge amplifier configuration with split power supply (Po = 24W, $V_S = \pm$ 12V)



PRACTICAL CONSIDERATION

Printed circuit board

The layout shown in fig. 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

Application suggestion

The recommended values of the components are the ones shown on application circuits of fig. 13. Different values can be used. The following table can help the designers.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R_1	22 KΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R_2	680Ω	Closed loop gain setting	Decrease of gain	Increase pf gain
R_3	22 KΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_5	$3 R_2$	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C_1	2.2 μF	Input DC decoupling		Increase of low freqencies cut off
C_2	22 μF	Inverting input DC decoupling		Increase of low frequencies cutoff
C_3C_4	0.1 μF	Supply voltage by pass		Danger of oscillation
C_5C_6	100 μF	Supply voltage by pass		Danger of oscillation
C_7	0.22 μF	Frequency stability		Danger of oscillation
C_8	$\frac{1}{2\pi B R_1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
D_1D_2	1N4001	To protect the device against output voltage spikes.		

SHORT CIRCUIT PROTECTION

The TDA 2006 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (fig. 19).
This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2006 is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shutdown protection keeps the junction temperature within safe limits.

Fig. 18 - Maximum output current vs. voltage $V_{Ce(sat)}$ across each output transistor

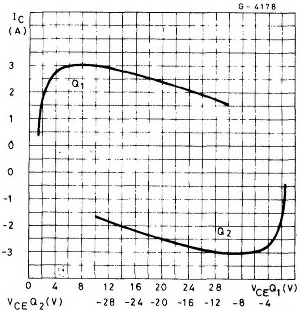
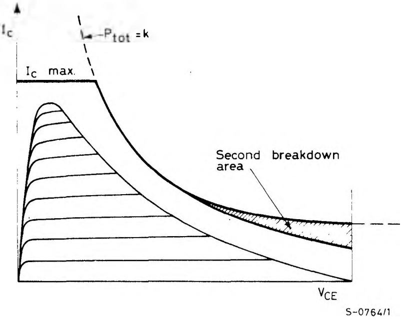


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

   If for any reason, the junction temperature increases up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

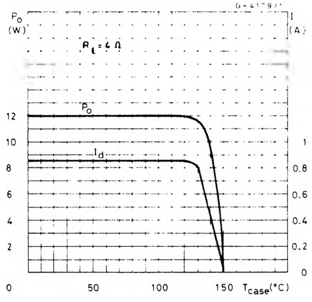
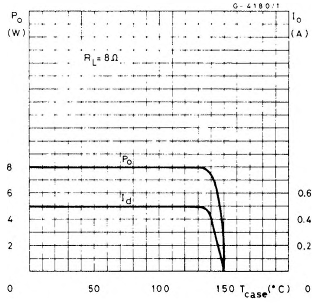


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistances.

Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

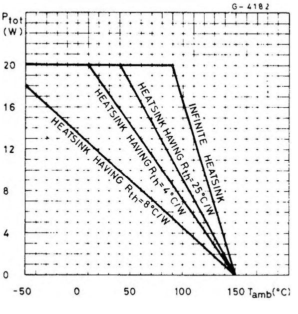
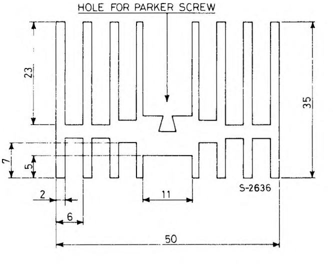


Fig. 23 - Example of heatsink



Dimension suggestion

The following table shows the lenght of the heatsink in fig. 23 for several values of P_{tot} and R_{th}.

P_{tot} (W)	12	8	6
Lenght of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3