Signetics

TDA2579
Synchronization Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA2579 generates and synchronizes horizontal and vertical signals. The device has a 3-level sandcastle output, a transmitter identification signal and also 50/60Hz identification.

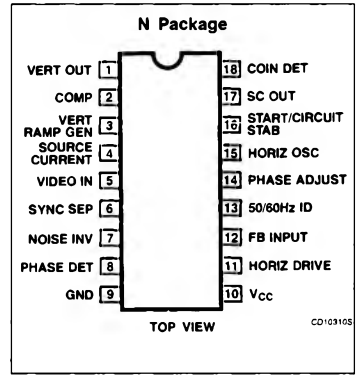
FEATURES

- **Horizontal phase detector, (sync to osc), sync separator and noise inverter**
- **Triple current source in the phase detector with automatic selection**
- **Inhibit of horizontal phase detector and video transmitter identification**
- **Second phase detector for storage compensation of the horizontal output stage**
- **Stabilized direct starting of the horizontal oscillator and output stage**
- **Horizontal output pulse with constant duty cycle value of 29μs**
- **Duty factor of the horizontal output pulse is 50% when horizontal flyback pulse is absent**
- **Internal vertical sync separator and two integration selection times**
- **Divider system with three different reset enable windows**
- **Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified**
- **Vertical comparator with a low DC feedback signal**
- **50/60Hz identification output combined with mute function**
- **Automatic amplitude adjustment for 50 and 60Hz and blanking pulse duration**

APPLICATIONS

- **Video terminals**
- **Television**
- **Video tape recorder**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-102HE)	0 to +70°C	TDA2579N

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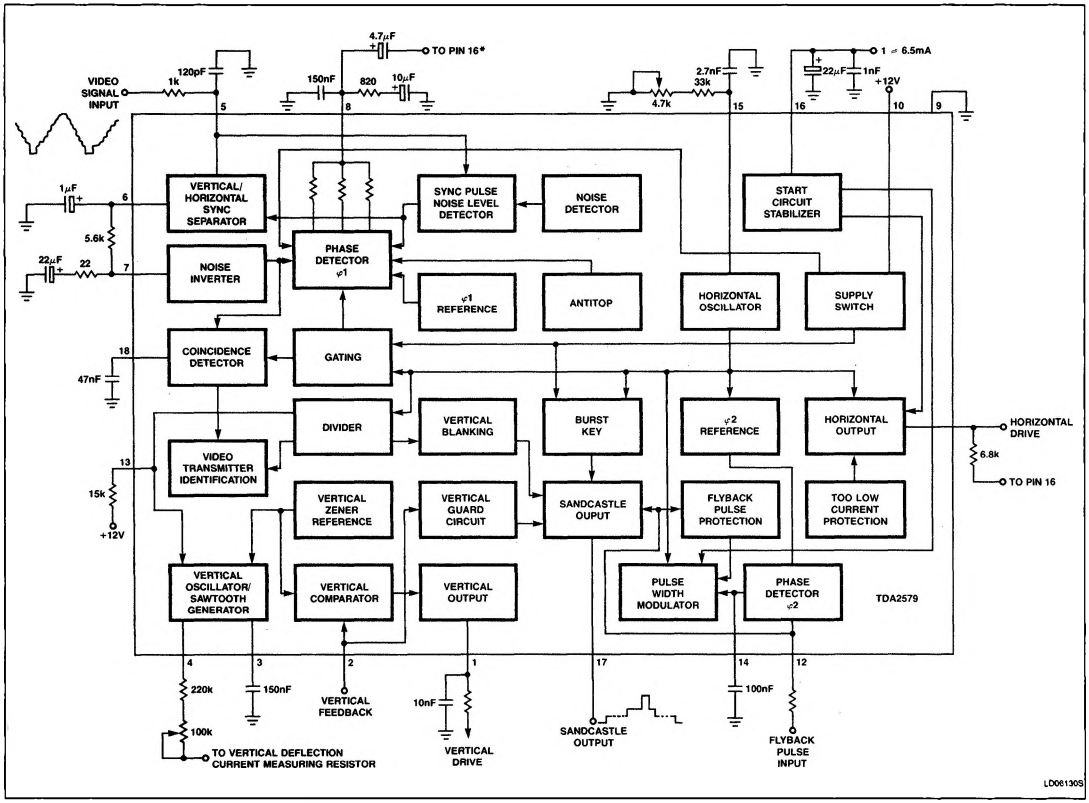
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
I_{16}	Start current	10	mA
V_{10}	Supply voltage	13.2	V
P_{TOT}	Power dissipation	1.2	W
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient in free air	50	°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
I_{16}	Supply current, Pin 16 $V_{10} = 0V$	6.5		10	mA
I_{16}	Supply current, Pin 16 $V_{10} = 9.5V$	2.5		10	mA
V_{16}	Stabilized voltage, Pin 16	8.1	8.7	9.3	V
I_{10}	Current consumption, Pin 10		68	85	mA
V_{CC}	Supply voltage range, Pin 10	9.5	12	13.2	V
Video input (Pin 5)					
V_5	Top sync. level	1.5	3.1	3.75	V
V_5	Sync. pulse amplitude[1]	0.1	0.6	1	V_{CC}
	Slicing level[2]	35	50	65	%
	Delay between video input and det. output (see also Figure 2)	0.2	0.3	0.5	μs
	Sync. pulse noise level detector circuit active		600		mV_{TT}
Sync. Pulse					
	Noise level detector circuit hysteresis		3		dB
Noise gate (Pin 5)					
V_5	Switching level		+0.7	+1	V
First control loop (Pin 8) (Horizontal osc. to sync.)					
Δf	Holding range		±800		Hz
Δf	Catching range	±600	±800	±1100	Hz
	Control sensitivity video with respect to burstkey and flyback pulse				
	Slow time constant		2.5		kHz/μs
	Normal time constant		10		kHz/μs
	Fast time constant		5		kHz/μs
	Phase modulation due to hum on the supply line Pin 10[3]		0.2		$μs/V_{TT}$
	Phase modulation due to hum on input current Pin 16[3]		0.08		$μs/mA_{TT}$
Second control loop (Pin 14) (Horizontal flyback to horizontal oscillator)					
$\Delta t_d/\Delta t_o$	Control sensitivity $t_D = 10μs$	200	300	600	μs
t_D	Control range	1		> 45	μs
t_D	Control range for constant duty cycle horizontal output	1	29 (-t flyback pulse)		
	Controlled edge of horizontal output signal Pin 11		positive		
Phase adjustment (Pin 14) (via second control loop)					
	Control sensitivity $t_D = 10μs$		25		μA/μs
I_{14}	Maximum allowed control current			±60	μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal oscillator (Pin 15) ($C = 2.7nF$; $R_{OSC} = 33k\Omega$					
f	Frequency (no sync.)		15625		Hz
Δf	Spread (fixed external component, no sync.)			±4	%
Δf	Frequency deviation between starting point output signal and stabilized condition		+5	+8	%
TC	Temperature coefficient		10		°C
Horizontal output (Pin 11) (Open-collector)					
V_{11}	Output voltage high			13.2	V
V_{11}	Start voltage protection (internal zener diode)	13		15.8	V
I_{16}	Low input current Pin 16 protection output enabled		5.5	6.5	mA
V_{11}	Output voltage low start condition ($I_{11} = 10mA$)		0.1	0.5	V
	Duty cycle output current during starting $I_{16} = 6.5mA$	55	65	75	%
V_{11}	Output voltage low normal condition ($I_{11} = 25mA$)		0.3	0.5	V
	Duty cycle output current without flyback pulse Pin 12	45	50	55	%
	Duration of the output pulse high $t_D = 8\mu s$	27	29	31	μs
	Controlled edge		positive		
	Temperature coefficient horizontal output pulse		−0.05		$\mu s/°C$
Sandcastle output signal (Pin 17) ($I_{LOAD} = 1mA$)					
	Output voltage during:				
V_{17}	burstkey	9.75	10.6		V
V_{17}	horizontal blanking	4.1	4.5	4.9	V
V_{17}	vertical blanking	2	2.5	3	V
V_{17}	Zero level output voltage $I_{SINK} = 0.5mA$			0.7	V
	Pulse width:				
t_P	burstkey	3.45	3.75	4.1	μs
V_{12}	horizontal blanking		1		V
	Phase position burstkey Time between middle synchronization pulse at Pin 5 and start burst at Pin 17	2.3	2.7	3.1	μs
	Time between start sync. pulse and end of burst pulse, Pin 17			9.2	μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Coincidence detector, video transmitter identification circuit and time constant switching levels (see also Figure 1)					
I_{18}	Detector output current		0.25		mA
V_{18}	Voltage level for in sync. condition (φ1 normal)		6.5		V
V_{18}	Voltage for noisy sync. pulse (φ1 slow and gated)	9	10		V
V_{18}	Voltage level for noise only[5]		0.3		V
V_{18}	Switching level normal-to-fast	3.2	3.5	3.8	V
V_{18}	Switching level Mute output active and fast-to-slow	1.0	1.2	1.4	V
V_{18}	Switching level frame period counter (3 periods fast)	0.08	0.12	0.16	V
V_{18}	Switching level Slow-to-fast (locking) Mute output inactive	1.5	1.7	1.9	V
V_{18}	Switching level fast-to-normal (locking)	4.7	5.0	5.3	V
V_{18}	Switching level normal-to-slow (gated sync. pulse)	7.4	7.8	8.2	V
Video transmitter identification output (Pin 13)					
V_{13}	Output voltage active (no sync., $I_{13} = 2mA$)		0.15	0.32	V
I_{13}	Sink current active (no sync.), $V_{13} < 1V$			5	mA
I_{13}	Output current inactive (sync. 50Hz)			1	μA
50/60Hz identification (Pin 13) (R_{13} positive supply 15kΩ)					
V_{13}	Emitter-follower, PNP 60Hz: $\frac{2 \times fH}{fV}$ < 576 voltage	7.2	7.65	8.1	V
V_{13}	50Hz: $\frac{2 \times fH}{fV}$ > 576 voltage		V_{10}		V
Flyback input pulse (Pin 12)					
V_{12}	Switching level		+1		V
I_{12}	Input current	+0.2		+4	mA
V_{12}	Input pulse			12	V_{CC}
R_{IN}	Input resistance		3		kΩ
	Phase position without shift				
t_D	Time between the middle of the sync. pulse at Pin 5 and the middle of the horizontal blanking pulse of Pin 17		2.5		μs
Vertical ramp generator (Pin 3)					
	Pulse width charge current		26		clock pulses
I_3	Charge current		3		mA
	Top level ramp signal voltage				
V_3	Divider in 50Hz mode[6]	5.1	5.5	5.9	V
V_3	Divider in 60Hz mode[6]	4.35	4.7	5.05	V
	Ramp amplitude $C_3 = 150nF$, $R_4 = 330k\Omega$, 50Hz[6] $R_4 = 330k\Omega$, 60Hz[6]		3.1 2.5		V_{CC} V_{CC}

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Current source (Pin 4)					
$V_{4.9}$	Output voltage $I_4 = 20\mu A$	6.6	7.1	7.6	V
I_4	Allowed current range	10		55	μA
	Temperature coefficient output voltage				
TC	$I_4 = 20\mu A$		+50		$10^{-6}/°C$
TC	$I_4 = 40\mu A$		+20		$10^{-6}/°C$
TC	$I_4 = 50\mu A$		−40		$10^{6}/°C$
Comparator (Pin 2) $C_3 = 150nF$; $R_4 = 330k\Omega$					
	Input voltage				
V_{2-9}	DC level[6]	0.9	1	1.1	V
V_{2-9}	AC level		0.8		V_{CC}
	Deviation amplitude 50/60Hz			2.5	%
	Vertical output stage, Pin 1 (NPN) emitter follower				
V_{1-9}	Output voltage I_O Pin 1 = +1.5mA	4.8	5.2	5.6	V
R_S	Sync. separator resistor		160		Ω
	Continuous sink current		0.25		mA
Vertical guard circuit (Pin 2) Active ($V_{17} = 2.5V$)					
V_2	Switching level low[6]	> 1.7	1.9	2.1	V
V_2	Switching level high[6]	< 0.3	0.4	0.5	V

NOTES:

1. Up to $1V_{P-P}$ the slicing level is constant, at amplitudes exceeding $1V_{P-P}$ the slicing level will increase.
2. The slicing level is fixed by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100\% \quad (R_S \text{ value in } k\Omega)$$

3. Measured between Pin 5 and sandcastle output Pin 17.
4. Divider in search (large) mode:
   start: reset divider = start vertical sync. plus 1 clock pulse
   stop:

$$n = \frac{2 \times fH}{fV} > 576 \text{ clock pulse } 42$$

$$n = \frac{2 \times fH}{fV} < 576 \text{ clock pulse } 34$$

   Divider in small window mode:
   start: clock pulse 517 (60Hz) clock pulse 619 (50Hz)
   stop: clock pulse 34 (60Hz) clock pulse 42 (50Hz)
5. Depends on DC level of Pin 5, given value is valid for $V_5 \approx 5V$.
6. Value related to internal zener diode reference voltage source spread includes the complete spread of reference voltage.

FUNCTIONAL DESCRIPTION

Vertical Part (Pins 1, 2, 3, 4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at Pin 3. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency and one line period equals 2 clock pulses. Due to the divider system, no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60Hz to 50Hz system. The divider system operates with 3 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its counter value by 1 for each time the separated vertical sync. pulse is within the searched window. The count is reduced by 1 when the vertical sync. pulse is not present.

Large (Search) Window: Divider Ratio Between 488 and 722

This mode is valid for the following conditions:

1. Divider is looking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Non-standard TV-signal condition detected while a double or enlarged vertical sync. pulse is still found after the internally-generated antitop flutter pulse has ended. This means a vertical sync. pulse width larger than 8 clock pulses (50Hz), that is, 10 clock pulses (60Hz). In general this mode is activated for video tape recorders operating in the feature/trick mode.
4. Up/down counter value of the divider system operating in the narrow window mode drops below count 1.
5. Externally setting. This can be reached by loading Pin 18 with a resistor of 180kΩ to earth or connecting a 3.6V diode stabistor between Pin 18 and ground.

Narrow Window: Divider Ratio Between 522 – 528 (60Hz) or 622 – 628 (50Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync. pulses. When the divider operates in this mode and a vertical sync. pulse is missing within the window, the divider is reset at the end of the window and the counter value is lowered by 1. At a counter value below count 1 the divider system switches over to the large window mode.

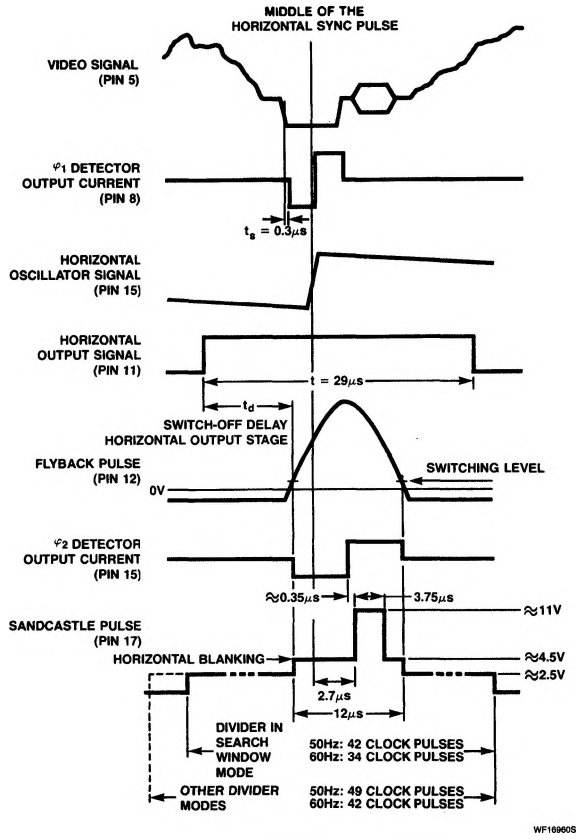


Figure 1. Timing Diagram of the TDA2579

Standard TV Norm

When the up/down counter has reached its maximum value of 12 in the narrow window mode, the information applied to the up/down counter is changed such that the standard divider ratio value is tested. When the counter has reached a value of 14, the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync. pulse is missing. A missed vertical sync. pulse lowers the counter value by 1. When the counter reaches the value of 10, the divider system is switched over to the large window mode. The standard TV norm condition gives maximum protection for video recorders playing tapes with anti-copy guards.

No TV Transmitter Found: (Pin 18 < 1.2V)

In this condition, only noise is present, the divider is reset to count 628. In this way a stable picture display at normal height is achieved.

Video Tape Recorders in Feature Mode

It should be noted that some VTRs operating in the feature modes, such as picture search, generate such distorted pictures that the no TV transmitter detection circuit can be activated as Pin V_{18} drops below 1.2V. This would imply a rollowing picture (condition d). In general, VTR machines use a reinserted vertical sync. pulse in the feature mode. Therefore, the divider system has been made such that the automatic reset of the divider at count 628 when V_{18} is below 1.2V is inhibited when a vertical sync. pulse is detected.

The divider system also generates the anti-top flutter pulse which inhibits the phase 1 detector during the vertical sync. pulse. The width of this pulse depends on the divider mode. For the divider mode a, the start is

generated at the reset of the divider. In modes b and c, the anti-top flutter pulse starts at the beginning of the first equalizing pulse. The anti-top flutter pulse ends at count 8 for 50Hz and count 10 for 60Hz. The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34 (17 lines for 60Hz, and at count 42 (21 lines) for 50Hz systems. The vertical blanking pulse generated at the sandcastle output Pin 17 is made by adding the anti-top flutter pulse and the blank pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b or c mode. For generating a vertical linear sawtooth voltage a capacitor should be connected to Pin 3. The recommended value is 150nF to 330nF (see Block Diagram).

The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is activated also at reset. When the capacitor has reached a voltage value of 5.5V for the 50Hz system or 4.7V for the 60Hz system the voltage is kept constant until the charging period ends. The charge period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an NPN transistor current source, the value of which can be set by an external resistor between Pin 4 and ground (Pin 9). Pin 4 is connected to a PNP transistor current source which determines the current of the NPN current source. The PNP current source on Pin 4 is connected to an internal zener diode reference voltage which has a typical voltage of ≈ 7.1V. The recommended operating current range is 10 to 50μA. The resistance at pin R_4 should be 140 to 700kΩ. By using a double current mirror concept the vertical sawtooth pre-correction can be set on the desired value by means of external components between Pin 4 and Pin 3, or by connecting the Pin 4 resistor to the vertical current measuring resistor of the vertical output stage. The vertical amplitude is set by the current of Pin 4. The vertical feedback voltage of the output stage has to be applied to Pin 2. For the normal amplitude adjustment the values are DC = 1V and AC = 0.8V. Due to the automatic system adaption both values are valid for 50Hz and 60Hz.

The low DC-voltage value improves the picture bounce behaviour as less parabola compensation is necessary. Even a fully DC-coupled feedback circuit is possible.

Vertical Guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on Pin 2. When the level on Pin 2 is below 0.4V or higher than 1.9V, the guard circuit inserts a continuous level of 2.5V in the sandcastle output signal of Pin 17. This results in the blanking of the picture displayed, thus preventing a burnt-in horizontal line. The guard levels specified refer to the zener diode reference voltage source level.

Driver Output

The driver output is at Pin 1, it can deliver a drive current of 1.5mA at 5V output. The internal impedance is about 150Ω. The output pin is also connected to an internal current source with a sinking current of 0.25mA.

Sync. Separator, Phase Detector and TV Station Identification, (Pins 5, 6, 7, 8, and 18)

The video input signal is connected to Pin 5. The sync. separator is designed such that the slicing level is independent of the amplitude of the sync. pulse. The black level is measured and stored in the capacitor at Pin 7. The slicing level value is stored in the capacitor at Pin 6. The slicing level value can be chosen by the value of the external resistor between Pins 6 and 7. The value is given by the formula:

$$P = \frac{R_S \times 100}{5.3 + R_S} \quad (R_S \text{ value in } k\Omega)$$

Where R_S is the resistor between Pins 6 and 7 and top sync. level equals 100%. The recommended resistor value is 5.6kΩ.

Black Level Detector

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty cycle of 50% and the flyback pulse at Pin 12. In this way the TV transmitter identification operates also for all DC conditions at input Pin 5 (no video modulation, plain carrier only).

During the frame interval the slicing level detector is inhibited by a signal which starts with the anti-top flutter pulse and ends with the reset vertical divider circuit. In this way shift of the slicing level due to the vertical sync. signal is reduced and separation of the vertical sync. pulse is improved.

Noise Inverter

An internal noise inverter is activated when the video level at Pin 5 drops below 0.7V. The IC embodies also a built-in sync. pulse noise level detection circuit. This circuit is directly connected to Pin 5 and measures the noise level at the middle of the horizontal sync. pulse. When a noise level of 600mV_{P-P} is detected, a counter circuit is activated. A video input signal is processed as "acceptable noise-free" when 12 out of 16 sync. pulses have a noise level below 600mV for two succeeding frame periods. The sync. pulses are processed during a 16 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of about 150mV (≈ 3dB).

When the "acceptable noise-free" condition is found, the phase detector of Pin 8 is switched to not-gated and normal time constant. When a higher sync. pulse noise level is found, the phase detector is switched over to slow time constant and gated sync. pulse phase detection. At the same time the integration time of the vertical sync. pulse separator is adapted.

Phase Detector

The phase detector circuit is connected to Pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of Pin 18 and the state of the sync. pulse noise detection circuit.

All three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top flutter pulse period, and the separated vertical sync. pulse time.

As a result, phase jumps in the video signal related to video head takeover of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period, the phase detector time constant is lowered by 2.5 times. In this way no need for external VTR time constant switching exists, so all station numbers are suitable for signals from VTR, video games or home computers.

For quick locking of a new TV station starting from a noise-only signal condition (normal time constant), a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage drop below 0.1V at Pin 18. This will activate a frame period counter which switches the phase detector to fast for 3 frame periods.

Horizontal Oscillator

The horizontal oscillator will now lock to the new TV station and as a result, the voltage on Pin 18 will increase to about 6.5V. When Pin 18 reaches a level of 1.8V the mute output transistor of Pin 13 is switched off and the divider is set to the large window. In general the mute signal is switched off within 5ms (pin C_{18} = 47nF) after reception of a new TV signal. When the voltage on Pin 18 reaches a level of 5V, usually within 15ms, the frame counter is switched off and the time constant is switched from fast to normal.

If the new TV station is weak, the sync. noise detector is activated. This will result in a changeover of Pin 18 voltage from 7V to ≈ 10V. When Pin 18 exceeds the level of 7.8V the phase detector is switched to slow time constant and gated sync. pulse condition.

When desired, most conditions of the phase detector can also be set by external means in the following way:

a. Fast time constant TV transmitter identification circuit not active, connect Pin 18 to earth (Pin 9).

b. Fast time constant TV transmitter identification circuit active, connect a resistor of 180kΩ between Pin 18 and ground. This condition can also be set by using a 3.6V stabistor diode instead of a resistor.

c. Slow time constant, (with exception of frame blanking period), connect Pin 18 via a resistor of 10kΩ to +12V, Pin 10. In this condition the transmitter identification circuit is not active.

d. No switching to slow time constant desired (transmitter identification circuit active), connect a 6.8V zener diode between Pin 18 and ground.

Figure 2 illustrates the operation of the 3 phase detector circuits.

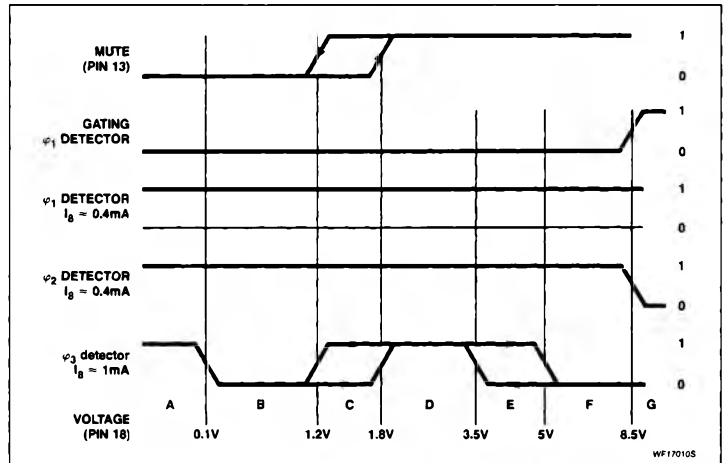


Figure 2. Timing Diagram, Phase Detectors.

Supply (Pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage can start operating by application of a very low supply current into Pin 16.

The horizontal oscillator starts at a supply current of about 4.5mA. The horizontal output stage is forced into the non-conducting stage until the supply current has a typical value of 5.5mA. The circuit has been designed so that after starting the horizontal output function a current drop of ≈ 1mA is allowed. The starting circuit gives the possibility to derive the main supply (Pin 10), from the horizontal output stage. The horizontal output signal can also be used as the oscillator signal for synchronized switch-mode power supplies. The maximum allowed starting current is 10mA. The main supply should be connected to Pin 10, and Pin 9 should be used as ground. When the voltage on Pin 10 increases from zero to its final value (typically 12V) a part of the supply current of the starting circuit is taken from Pin 10 via internal diodes, and the voltage on Pin 16 will stabilize to a typical value of 8.7V.

In stabilized condition (Pin $V_{10} > 9.5V$) the minimum required supply current to Pin 16 is ≈ 2.5mA. All other IC functions are switched on via the main supply voltage on Pin 10. When the voltage on Pin 10 reaches a value of ≈ 7V the horizontal phase detector circuit is activated and the vertical ramp on Pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on Pin 10 reaches the stabilized voltage value of Pin 16 which is typically 8.7V.

For closing the second phase detector loop, a flyback pulse must be applied to Pin 12. When no flyback is detected, the duty cycle of the horizontal output stage is 50%.

For remote switch-off Pin 16 can be connected to ground (via an NPN transistor with a series resistor of ≈ 500Ω) which switches off the horizontal output.

Horizontal Oscillator, Horizontal Output Transistor, and Second Phase Detector (Pins 11, 12, 14 and 15)

The horizontal oscillator is connected to Pin 15. The frequency is set by an external RC combination between Pin 15 and ground, Pin 9. The open collector horizontal output stage is connected to Pin 11. An internal zener diode configuration limits the open voltage of Pin 11 to ≈ 14.5V.

The horizontal output transistor at Pin 11 is blocked until the current into Pin 16 reaches a value of ≈ 5.5mA.

A higher current results in a horizontal output signal at Pin 11, which starts with a duty cycle of ≈ 35% HIGH.

The duty cycle is set by an internal current source-loaded NPN emitter-follower stage connected to Pin 14 during starting. When Pin 16 changes over to voltage stabilization, the NPN emitter-follower and current source load at Pin 14 are switched off and the second phase detector circuit is activated, provided a horizontal flyback pulse is present at Pin 12. When no flyback pulse is detected at Pin 12 the duty cycle of the horizontal output stage is set to 50%.

The phase detector circuit at Pin 14 compensates for storage time in the horizontal deflection output stage. The horizontal output pulse duration in 29μs HIGH for storage times between 1μs and 17μs (29μs flyback pulse of 12μs). A higher storage time increases the HIGH time. Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor of Pin 14.

Mute Output and 50/60Hz Identification (Pin 13)

The collector of an NPN transistor is connected to Pin 13. When the voltage on Pin 18 drops below 1.2V (no TV transmitter) the NPN transistor is switched ON.

When the voltage on Pin 18 increases to a level of ≈ 1.8V (new TV transmitter found) the NPN transistor is switched OFF.

Pin 13 has also the possibility for 50/60Hz identification. This function is available when Pin 13 is connected to Pin 10 (+12V) via an external pull-up resistor of 10 – 20kΩ. When no TV transmitter is identified, the voltage on Pin 13 will be LOW (< 0.5V). When a TV transmitter with a divider ratio > 576 (50Hz) is detected the output voltage of Pin 13 is HIGH (+12).

When a TV transmitter with a divider ratio < 576 (60Hz) is found an internal PNP transistor with its emitter connected to Pin 13 will force this pin output voltage down to ≈ 7.5V.

Sandcastle Output (Pin 17)

The sandcastle output pulse generated at Pin 17, has three different voltage levels. The highest level, (11V), can be used for burst gating and black level clamping. The second level, (4.5V), is obtained from the horizontal flyback pulse at Pin 12, and is used for horizontal blanking. The third level, (2.5V), is used for vertical blanking and is derived via

the vertical divider system. For 50Hz the blanking pulse duration is 42 clock pulses and for 60Hz it is 34 clock pulses started from the vertical divider reset. For TV signals which have a divider ratio between 622 and 628 or 522 and 528 the blanking pulse is started at the first equalizing pulse.

TYPICAL APPLICATION

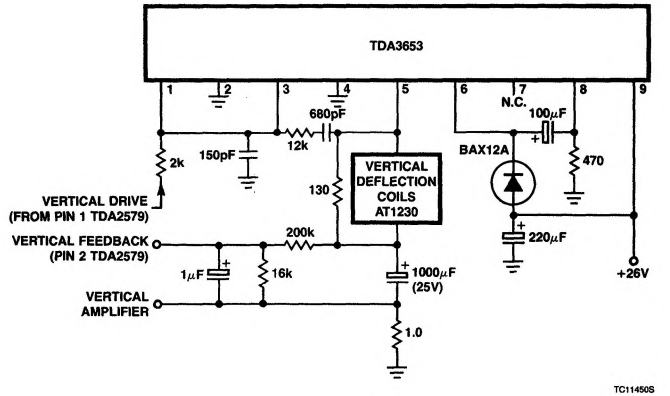


Figure 3