HORIZONTAL COMBINATION TDA2595

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12 V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50 mV
Horizontal output current	I_4	max.	30 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

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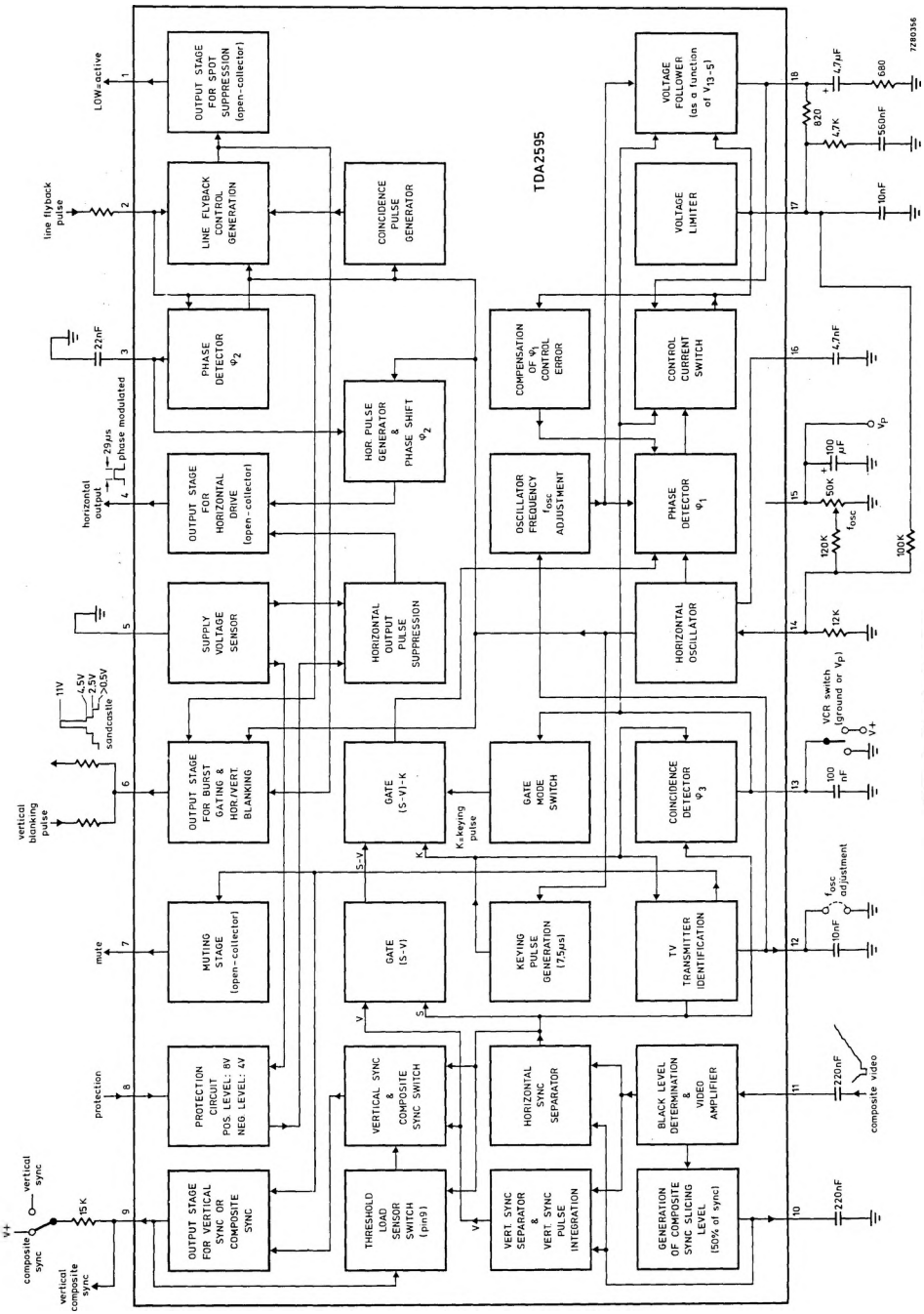

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15-5} = V_P$	max.	13.2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7-5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18-5}$	max.	V_P	V
pin 11 (range)	V_{11-5}		−0.5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0.2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	30	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude					
Capacitor current during:					
video	I_{10}	–	12	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 25% (50% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	V_{14-5}	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15-5}/V_{15-5}}$	–	± 0.05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
charging	$-I_{16}$	–	1024	–	μA
discharging	I_{16}	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 30 mA	V_{4-5}	–	–	0.5	V
Pulse duration (HIGH)	t_p	–	29 ± 1.5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3.55	–	8.3	V
Leakage current at $V_{17\text{-}5}$ = 3.55 to 8.3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1.8	2	2.2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9.5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9.5 V	$\pm I_{17}$	1.8	2	2.2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	Δf_{osc}	–	± 680	–	Hz
spread of catching and holding range	Δf_{osc}	–	± 10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2.9 to 9.5 V	t_p	–	7.5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9.5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9.5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	V_{13-5}	–	–	1	V
without coincidence without composite video signal (noise)	V_{13-5}	–	–	2	V
with coincidence with composite video signal	V_{13-5}	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13-5} = V_P - 0.5$ V	I_{13}	–	–	100	μA
at $V_{13-5} = 0.5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison	V_{2-5}	–	3	–	V
Switching level for horizontal blanking and flyback control	V_{2-5}	–	3	–	V
Input voltage limiting	V_{2-5}	–	–0.7	–	V
	or:	–	+4.5	–	V
Switching current					
at horizontal flyback	I_2	0.01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0.2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 μs (note 2)	Δt	–	2.6 ± 0.7	–	μs
If additional adjustment is required, it can be arranged by applying a current at pin 3, such that for applied current:	$\Delta I/\Delta t$	–	30	–	μA/μs
Burst gating pulse (pin 6; note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3.7	4	4.3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2.15	2.65	3.15	μs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4.2	4.5	4.9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0.5	V
Clamping circuit for vertical blanking pulse (pin 6; note 3)					
Output voltage at I_6 = 2.8 mA	V_{6-5}	2.15	2.5	3	V
Minimum output current at $V_{6-5} > 2.15$ V	I_{6min}	–	2.3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3.3	–	mA
TV-transmitter identification (pin 12)					
Output voltage no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	V_{7-5}	–	–	0.5	V
Output resistance at I_7 = 3 mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0.8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0.4	–	V
Current limiting for V_{8-5} = 1 to 8.5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8-5} > 8.5$ V	R_{8-5}	–	3	–	kΩ
Response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_1 = 3 mA	V_{1-5sat}	–	–	0.5	V
Output leakage current in case of break in transmission	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.