

TDA3047 IR Preamplifier

Product Specification

Linear Products

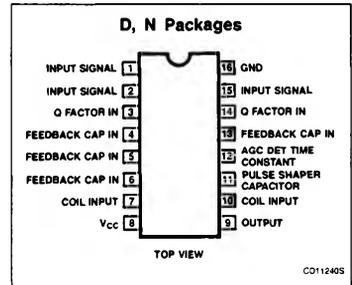
DESCRIPTION

The TDA3047 is for infrared reception with low power consumption.

FEATURES

- HF amplifier with a control range of 66dB
- Synchronous demodulator and reference amplifier
- AGC detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the AGC circuit
- Input voltage limiter

PIN CONFIGURATION



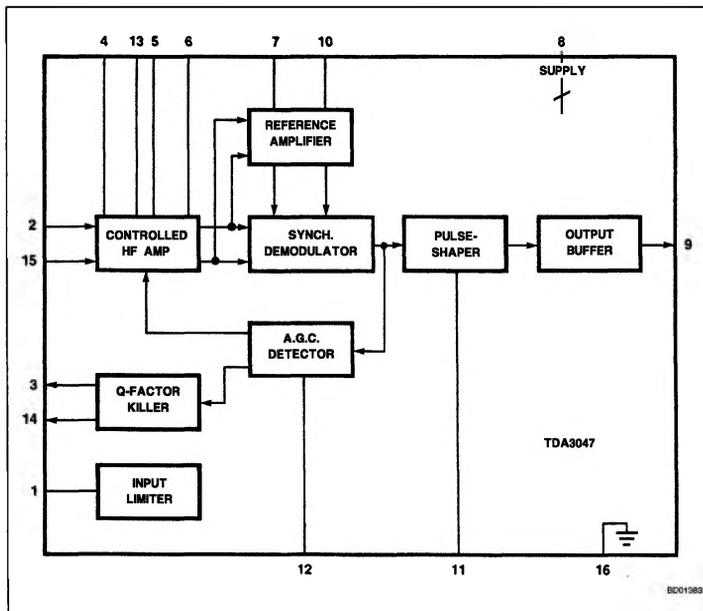
APPLICATION

- IR remote control systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	-25°C to +125°C	TDA3047N
16-Pin Plastic SO (SOT-109A)	0 to +70°C	TDA3047TD

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 8)	13.2	V
I_{11}	Output current pulse shaper (Pin 11)	10	mA
V_{2-15}	Voltages between pins ¹ Pins 2 and 15 Pins 4 and 13 Pins 5 and 6 Pins 7 and 10 Pins 9 and 11	4.5	V
V_{4-13}		4.5	V
V_{5-6}		4.5	V
V_{7-10}		4.5	V
V_{9-11}		4.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-25 to +125	°C

NOTE:

1. All pins except Pin 11 are short-circuit protected.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = V_B = 5V$; $T_A = 25^\circ C$, measured in Figure 3, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 8)					
V_{CC}	Supply voltage	4.65	5.0	5.35	V
$I_{CC} = I_B$	Supply current	1.2	2.1	3.0	mA
Controlled HF amplifier (Pins 2 and 15)					
$V_{2-15(P-P)}$ $V_{2-15(P-P)}$	Minimum input signal (peak-to-peak value) at $f = 36kHz^1$ at $f = 36kHz^2$		15	25 5	μV μV
	AGC control range (without Q-killing)	60	66		dB
$V_{2-15(P-P)}$	Input signal for correct operation (peak-to-peak value) ³	0.02		200	mV
$V_{2-15(P-P)}$	Q-killing inactive ($I_B = I_{14} < 0.5\mu A$) peak-to-peak value)			140	μV
$V_{2-15(P-P)}$	Q-killing active ($I_{14} = I_B = \text{max.}$) (peak-to-peak value)	28			mV
	Q-killing range	Figure 1			
Inputs					
V_2	Input voltage (Pin 2)	2.25	2.45	2.65	V
V_{15}	Input voltage (Pin 15)	2.25	2.45	2.65	V
R_{2-15}	Input resistance (Pin 2)	10	15	20	$k\Omega$
C_{2-15}	Input capacitance (Pin 2)		3		pF
V_{1-16}	Input limiting (Pin 1) at $I_1 = 3mA$		0.8	0.9	V
Outputs					
$-V_{9-8}$	Output voltage HIGH (Pin 9) at $-I_9 = 75\mu A$		0.1	0.5	V
V_9	Output voltage LOW (Pin 9) at $I_9 = 75\mu A$		0.1	0.5	V
$-I_9$ $-I_9$ $-I_9$	Output current; output voltage HIGH at $V_9 = 4.5V$ at $V_9 = 3.0V$ at $V_9 = 1.0V$	75 75 75	120 130 140		μA μA μA
I_9	Output current; output voltage LOW at $V_9 = 0.5V$	75	120		μA
R_{7-10}	Output resistance between Pins 7 and 10	3.1	4.7	6.2	$k\Omega$

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DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_B = 5V$; $T_A = 25^\circ C$, measured in Figure 3, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Pulse shaper (Pin 11)					
V_{11}	Trigger level in positive direction (voltage Pin 9 changes from HIGH to LOW)	3.75	3.9	4.05	V
V_{11}	Trigger level in negative direction (voltage Pin 9 changes from LOW to HIGH)	3.4	3.55	3.7	V
ΔV_{11}	Hysteresis of trigger levels	0.25	0.35	0.45	V
AGC detector (Pin 12)					
$-I_{12}$	AGC capacitor charge current	3.3	4.7	6.1	μA
I_{12}	AGC capacitor discharge current	67	100	133	μA
Q-factor killer (Pins 3 and 14)					
$-I_3$	Output current (Pin 3) at $V_{12-16} = 2V$	2.5	7.5	15	μA
$-I_{14}$	Output current (Pin 14) at $V_{12-16} = 2V$	2.5	7.5	15	μA

NOTES:

1. Voltage Pin 9 is HIGH; $-I_3 = 75\mu A$.
2. Voltage Pin 9 remains LOW.
3. Undistorted output pulse with 100% AM input.

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5V supply and has a current consumption of 2mA. The output is a current source which can drive or suppress current of $> 75\mu A$ with a voltage swing of 4.5V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of $> 600mV$ by an input limiter. The typical input is an AM signal at a frequency of 36kHz. Figures 2 and 3 show the circuit diagrams for the application of narrow-band and wide-band receivers, respectively. Circuit description of the eight sections shown in the Block Diagram are given below.

Controlled HF Amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three DC amplifier stages connected in cascade. The overall gain of the circuit is approximately 83dB and the gain control range is in the order of 66dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the DC coupled amplifier are minimized by two negative feedback loops. These also allow the circuit to have some series resis-

tance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference Amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous Demodulator

In the synchronous demodulator, the input signal and reference signal are multiplied. The demodulator output current is $25\mu A$ peak-to-peak. The output signal of the demodulator is fed to the input of the AGC detector and to the input of the pulse-shaper circuit.

AGC Detector

The AGC detector comprises two NPN transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the AGC circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-Shaper

The pulse-shaper comprises two NPN transistors operating as a differential pair con-

nected in parallel with the AGC differential pair. The slicing level of the pulse shaper is lower than the slicing level of the AGC detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to Pin 11 which is applied directly to the output buffer.

Output Buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at Pin 9 is active HIGH.

Q-factor Killer

Figure 2 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at Pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; Pin 3 to Pin 2, and Pin 14 to Pin 15.

Input Limiter

In the narrow-band application, high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0.7V. Limiting is 0.9V maximum at $I_1 = 3mA$.

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