Signetics

# TDA3566

## PAL/NTSC Decoder With RGB Inputs

*Product Specification*

**Linear Products**

### DESCRIPTION

The TDA3566 is a monolithic, integrated decoder for the PAL® and/or NTSC color television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore, it contains a luminance amplifier, and an RGB matrix and amplifier. These amplifiers supply output signals up to $4V_{P-P}$ (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analog as well as digital, which can be used for text display systems (e.g., Teletext/broadcast antiope), channel number display, etc.

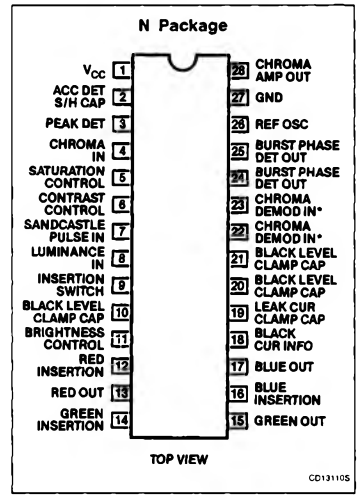
### FEATURES

- **A black current stabilizer which controls the black currents of the three electron guns to a level low enough to omit the black level adjustment**
- **Contrast control of inserted RGB signals**
- **No black level disturbance when nonsynchronized external RGB signals are available on the inputs**
- **NTSC capability with hue control**
- **Single-chip chroma and luminance processor**
- **ACC with peak detector**
- **DC control settings**
- **External linear or digital RGB inputs**
- **High-level RGB outputs**
- **Luminance signal with clamp**
- **On-chip hue control for NTSC**

### APPLICATIONS

- **Video monitors and displays**
- **Text display systems**
- **TV receivers**
- **Graphic systems**
- **Video processing**

### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 28-Pin Plastic DIP (SOT-117) | −25°C to +70°C | TDA3566N |

### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC} = V_{1-27}$ | Supply voltage (Pin 1) | 13.2 | V |
| $P_{TOT}$ | Total power dissipation | 1.7 | W |
| $T_{STG}$ | Storage temperature range | −65 to +150 | °C |
| $T_A$ | Operating ambient temperature range | −25 to +70 | °C |
| $\theta_{JA}$ | Thermal resistance from junction to ambient (in free air) | 40 | °C/W |

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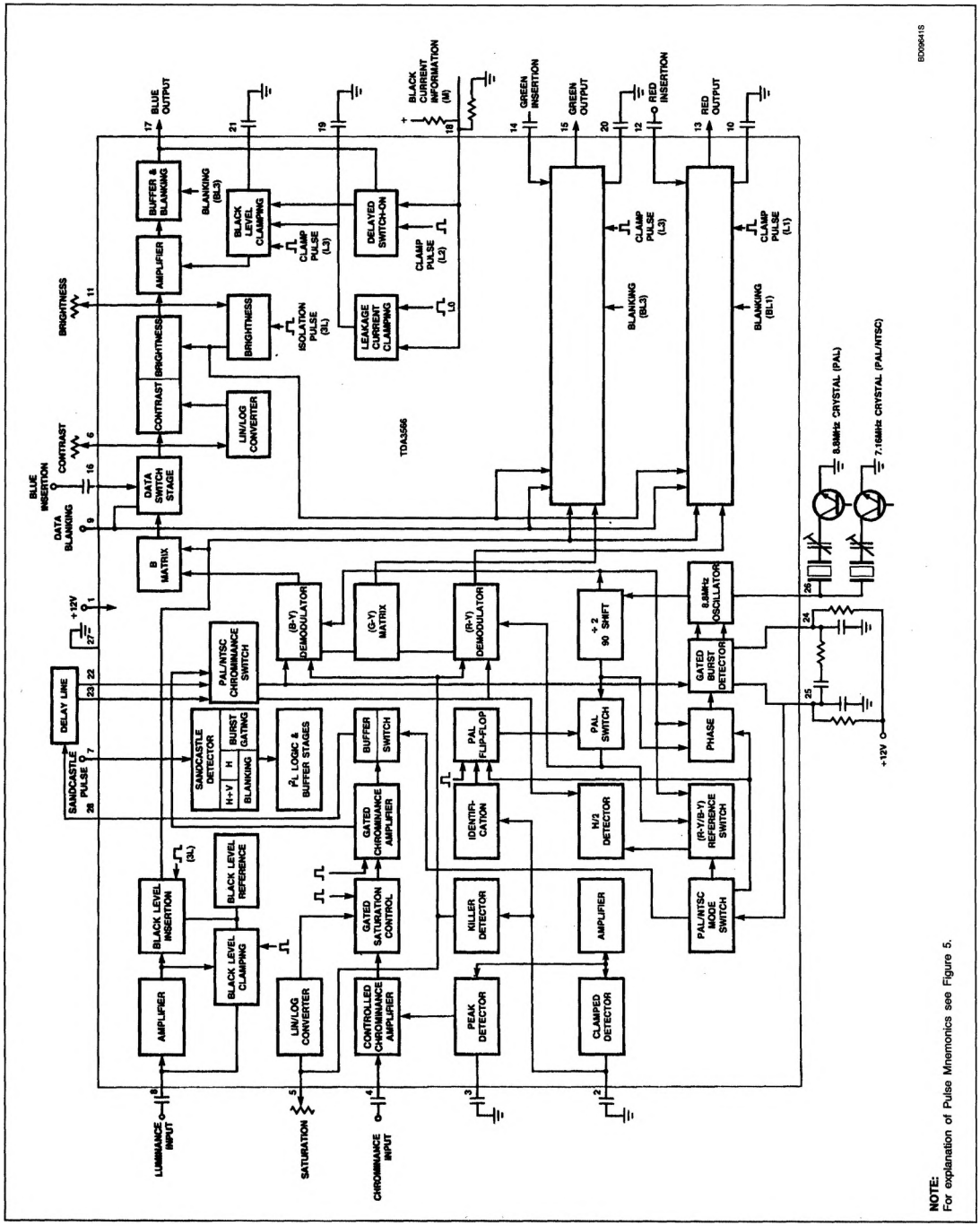
## BLOCK DIAGRAM




**NOTE:**
For explanation of Pulse Mnemonics see Figure 5.

**DC AND AC ELECTRICAL CHARACTERISTICS** $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Supply (Pin 1)** | | | | | |
| $V_{CC} = V_{1-27}$ | Supply voltage | 10.8 | 12 | 13.2 | V |
| $I_{CC} = I_1$ | Supply current | | 80 | 110 | mA |
| $P_{TOT}$ | Total power dissipation | | 0.95 | 1.3 | W |
| **Luminance amplifier (Pin 8)** | | | | | |
| $V_{8-27(P-P)}$ | Input voltage[1] (peak-to-peak value) | | 0.45 | 0.63 | V |
| $V_{8-27}$ | Input level before clipping | | | 1 | V |
| $I_8$ | Input current | | 0.1 | 1 | μA |
| | Contrast control range (see Figure 1) | −15 | | +5 | dB |
| $I_7$ | Input current contrast control | | | 15 | μA |
| **Chrominance amplifier (Pin 4)** | | | | | |
| $V_{4-27(P-P)}$ | Input voltage[2] (peak-to-peak value) | 40 | 390 | 1100 | mV |
| $\lvert Z_{4-27} \rvert$ | Input impedance (Pin 4) | | 10 | | kΩ |
| $C_{4-27}$ | Input capacitance | | | 6.5 | pF |
| | ACC control range | 30 | | | dB |
| $\Delta V$ | Change of the burst signal at the output over the whole control range | | | 1 | dB |
| $A_V$ | Gain at nominal contrast/saturation Pin 4 to Pin 28[3] | 34 | | | dB |
| | Chrominance to burst ratio at nominal saturation at Pin 28[2, 3] | | 12 | | dB |
| $V_{28-27(P-P)}$ | Maximum output voltage range (peak-to-peak value); $R_L = 2k\Omega$ | 4 | 5 | | V |
| d | Distortion of chrominance amplifier at $V_{28-27(P-P)} = 2V$ (output) up to $V_{4-27(P-P)} = 1V$ (input) | | | 5 | % |
| $\alpha_{28-4}$ | Frequency response between 0 and 5MHz | | | −2 | dB |
| | Saturation control range (see Figure 2) | 50 | | | dB |
| $I_5$ | Input current saturation control (Pin 5) | | | 20 | μA |
| | Cross-coupling between luminance and chrominance amplifier[4] | | | −46 | dB |
| S/N | Signal-to-noise ratio at nominal input signal[5] | 56 | | | dB |
| $\Delta\varphi$ | Phase shift between burst and chrominance at nominal contrast/ saturation | | | ±5 | deg |
| $\lvert Z_{28-27} \rvert$ | Output impedance of chrominance amplifier | | 10 | | Ω |
| $I_{28}$ | Output current | | | 15 | mA |

**DC AND AC ELECTRICAL CHARACTERISTICS** (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Reference part** | | | | | |
| | Phase-locked loop | | | | |
| $\Delta f$ | catching range[6] | 500 | 700 | | Hz |
| $\Delta\varphi$ | phase shift for ±400Hz deviation of $f_{OSC}$[6] | | | 5 | deg |
| | Oscillator | | | | |
| $TC_{OSC}$ | temperature coefficient of oscillator frequency[6] | | −2 | −3 | Hz/°C |
| $\Delta f_{OSC}$ | frequency variation when supply voltage increases from 10 to 13.2V[6] | | 40 | 100 | Hz |
| $R_{26-27}$ | input resistance (Pin 26) | 280 | 400 | 520 | Ω |
| $C_{26-27}$ | input capacitance (Pin 26) | | | 10 | pF |
| | ACC generation (Pin 2) | | | | |
| $V_{2-27}$ | control voltage at nominal input signal | | 4.6 | | V |
| $V_{2-27}$ | control voltage without chrominance input | | 2.6 | | V |
| $V_{2-27}$ | color-off voltage | | 3.4 | | V |
| $V_{2-27}$ | color-on voltage | | 3.6 | | V |
| $V_{2-27}$ | identification-on voltage | | 2.0 | | V |
| | change in burst amplitude with temperature | | 0.1 | 0.25 | %/°C |
| $V_{3-27}$ | voltage at Pin 3 at nominal input signal | | 5.1 | | V |
| **Demodulator part** | | | | | |
| $V_{23-27(P-P)}$ | Input burst signal amplitude[7] (peak-to-peak value) between Pins 23 and 27 | 68 | 80 | 95 | mV |
| $\lvert Z_{22-27/23-27} \rvert$ | Input impedance between Pins 22 or 23 and 27 | 0.7 | 1 | 1.3 | kΩ |
| | Ratio of demodulated signals[8] | | | | |
| $\frac{V_{17-27}}{V_{13-27}}$ | (B-Y)/(R-Y) | | 1.78± 10% | | |
| $\frac{V_{15-27}}{V_{13-27}}$ | (G-Y)/(R-Y); no (B-Y) signal | | −0.51± 10% | | |
| $\frac{V_{15-27}}{V_{17-27}}$ | (G-Y)/(B-Y); no (R-Y) signal | | −0.19± 10% | | |
| $\alpha_{17}$ | Frequency response between 0 and 1MHz | | | −3 | dB |
| | Cross-talk between color difference signals | 40 | | | dB |
| $\Delta\varphi$ | Phase difference between (R-Y) signal and (R-Y) reference signals | | | 5 | deg |
| $\Delta\varphi$ | Phase difference between (R-Y) signal and (B-Y) reference signals | 85 | 90 | 95 | deg |

**DC AND AC ELECTRICAL CHARACTERISTICS** (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **RGB matrix and amplifiers** | | | | | |
| $V_{13, 15, 17-27(P-P)}$ | Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white)[3] | 3.5 | 4 | 4.5 | V |
| $V_{13-27(P-P)}$ | Output voltage at Pin 13 (peak-to-peak value) at nominal contrast/ saturation and no luminance signal to (R-Y) | | 4.2 | | V |
| $V_{13, 15, 17(m)}$ | Maximum peak-white level | 9.7 | 10 | 10.3 | V |
| $I_{13, 15, 17}$ | Available output current (Pins 13, 15, 17) | 10 | | | mA |
| $\Delta V_{13, 15, 17-27}$ | Difference between black level and measuring level at the output for a brightness control voltage at Pin 11 of 2V[9] | | 0 | | V |
| $\Delta V$ | Difference in black level between the three channels without black current stabilization[10] | | | 100 | mV |
| | Control range of black-current stabilization $V_{CC1} = 3V$; $V_{11-17} = 2V$ | | | ±2 | V |
| $\Delta V$ | Black level shift with vision contents | | | 40 | mV |
| | Brightness control voltage range | | see Figure 2 | | |
| $I_{11}$ | Brightness control input current | | | 5 | μA |
| $\Delta V/\Delta T$ | Variation of black level with temperature | | 0 | | mV/°C |
| $\Delta V$ | Variation of black level with contrast* | | | 100 | mV |
| | Relative spread between the R, G, and B output signals | | | 10 | % |
| $\Delta V$ | Relative black-level variation between the three channels during variation of contrast, brightness, and supply voltage (±10%)* | | 0 | 20 | mV |
| $\Delta V$ | Differential black-level drift over a temperature range of 40°C | | 0 | 20 | mV |
| $V_{BL}$ | Blanking level at the RGB outputs | | 0.95 | 1.1 | V |
| $V_{BL}$ | Difference in blanking level of the three channels | | 0 | | mV |
| $V_{BL}$ | Differential drift of the blanking levels over a temperature range of 40°C | | 0 | 10 | mV |
| $\frac{\Delta V_{BL}}{V_{BL}} \times \frac{V_{CC}}{\Delta V_{CC}}$ | Tracking of output black level with supply voltage | 0.9 | 1 | 1.1 | |
| | Tracking of contrast control between the three channels over a control range at 10dB | | | 0.5 | dB |
| $V_O$ | Output signal during the clamp pulse (3L) after switch-on | 7.5 | | | V |
| S/N | Signal-to-noise ratio of output signals[5] | 62 | | | dB |
| $V_{R(P-P)}$ | Residual 4.4MHz signal at RGB outputs (peak-to-peak value) | | | 50 | mV |
| $V_{R(P-P)}$ | Residual 8.8MHz signal and higher harmonics at the RGB outputs (peak-to-peak value) | | | 150 | mV |
| $\lvert Z_{13, 15, 17-27} \rvert$ | Output impedance of RGB outputs | | 50 | | Ω |
| $\alpha$ | Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5MHz | | −1 | −3 | dB |
| $I_O$ | Current source of output stage | 2 | 3 | | mA |
| $\Delta V$ | Difference of black level at the three outputs at nominal brightness* | | | 10 | mV |
| | Tracking of brightness control | | | 2 | % |

**NOTE:**
*With respect to the measuring pulses.

**DC AND AC ELECTRICAL CHARACTERISTICS** (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Signal insertion (Pins 12, 14, and 16)** | | | | | |
| $V_{12, 14, 16-27(P-P)}$ | Input signals (peak-to-peak value) for RGB output voltage of 4V (peak-to-peak) at nominal contrast | 0.9 | 1 | 1.1 | V |
| $\Delta V$ | Difference between the black levels of the RGB signals and the inserted signals at the output[11] | | | 100 | mV |
| $t_R$ | Output rise time | | 50 | 80 | ns |
| $t_D$ | Differential delay time for the three channels | | 0 | 40 | ns |
| $I_{12, 14, 16}$ | Input current | | | 10 | μA |
| **Data blanking (Pin 9)** | | | | | |
| $V_{9-27}$ | Input voltage for no data insertion | | | 0.4 | V |
| $V_{9-27}$ | Input voltage for data insertion | 0.9 | | | V |
| $V_{9-27(m)}$ | Maximum input voltage | | | 3 | V |
| $t_D$ | Delay of data blanking | | | 20 | ns |
| $R_{9-27}$ | Input resistance | 7 | 10 | 13 | kΩ |
| | Suppression of the internal RGB signals when $V_{9-27} > 0.9V$ | 46 | | | dB |
| **Sandcastle input (Pin 7)** | | | | | |
| $V_{7-27}$ | Level at which the RGB blanking is activated | 1 | 1.5 | 2 | V |
| $V_{7-27}$ | Level at which the horizontal pulses are separated | 3 | 3.5 | 4 | V |
| $V_{7-27}$ | Level at which burst gating and clamping pulse are separated | 6.5 | 7.0 | 7.5 | V |
| $t_D$ | Delay between black level clamping and burst gating pulse | | 0.6 | | μs |
| $-I_7$<br>$I_7$<br>$I_7$ | Input current<br>at $V_{7-27} = 0$ to 1V<br>at $V_{7-27} = 1$ to 8.5V<br>at $V_{7-27} = 8.5$ to 12V | | | 1<br>50<br>2 | mA<br>μA<br>mA |
| **Black current stabilization (Pin 18)** | | | | | |
| $V_{18-27}$ | Bias voltage (DC) | 3.5 | 5 | 7.0 | V |
| $\Delta V$ | Difference between input voltage for 'black' current and leakage current | 0.35 | 0.5 | 0.65 | V |
| $I_{18}$ | Input current during 'black' current | | | 1 | μA |
| $I_{18}$ | Input current during scan | | | 10 | mA |
| $V_{18-27}$ | Internal limiting at Pin 10 | 8.5 | 9 | 9.5 | V |
| $V_{18-27}$ | Switching threshold for 'black' current control ON | 7.6 | 8 | 8.4 | V |
| $R_{18-27}$ | Input resistance during scan | 1 | 1.5 | 2 | kΩ |
| $I_{10, 20, 21}$ | Input current during scan at Pins 10, 20, and 21 (DC) | | | TBD | nA |
| | Maximum charge/discharge current during measuring time | | 1 | | nA |

**DC AND AC ELECTRICAL CHARACTERISTICS** (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **NTSC** | | | | | |
| $V_{24-25}$ | Level at which the PAL/NTSC switch is activated (Pins 24 and 25) | | 8.8 | 9.2 | V |
| $I_{24+25(AV)}$ | Average output current[12] | 75 | 90 | 105 | μA |
| | Hue control | see Figure 4 | | | |

**NOTES:**

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a color bar with 75% saturation; chrominance to burst ratio is 2.2:1.
3. Nominal contrast is specified as the maximum contrast — 5dB and nominal saturation as the maximum saturation — 6dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to RMS noise.
6. All frequency variations are referred to 4.4MHz carrier frequency.
7. These signal amplitudes are determined by the ACC circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5V), but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discoloration during adjustment of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150Ω and the black level clamp pulse width is 4μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at Pins 24 and 25 can be changed by connecting the load resistors (10kΩ in this application) to the slider bar of the hue control potentiometer (see Figure 7). When the transistor is switched on, the voltage at Pins 24 and 25 is reduced below 9V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4μs typical.

## FUNCTIONAL DESCRIPTION

The TDA3566 is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566 are as follows:

- The NTSC application has largely been simplified. In the case of NTSC, the chroma signal is now internally coupled to the demodulators, ACC, and phase detectors. The chroma output signal (Pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566. Furthermore, there is no difference between the amplitude of the color output signals in the PAL or NTSC mode. The PAL/NTSC switch and the hue control of the TDA3566 and the TDA3562A are identical.
- The switch-on and the switch-off behavior of the TDA3566 has been improved. This has been obtained by suppressing the output signals during the switch-on and switch-off periods.
- The clamp capacitors connected to the Pins 10, 20, and 21 can be reduced to 100nF for the TDA3566. The clamp capacitors also receive a pre-bias voltage to avoid colored background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10pF.

### Luminance Amplifier

The luminance amplifier is voltage driven and requires an input signal of 450mV peak-to-peak (positive video). The luminance delay line must be connected between the IF amplifier and the decoder. The input signal is AC coupled to the input (Pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed DC level by the black clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via Pin 11 (brightness). At the same time, the RGB signals are clamped. Noise and residual signals have no influence during clamping; thus, simple internal clamping circuitry is used.

### Chrominance Amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be AC coupled (Pin 4) and have a minimum amplitude of $40mV_{p-p}$. The gain control stage has a control range in excess of 30dB; the maximum input signal must not exceed $1.1V_{p-p}$ or clipping of the input signal will occur. From the gain-control stage, the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via Pin 5. The control voltage range is 2 to 4V, the input impedance is high, and the saturation control range is in excess of 50dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12dB higher gain during the chrominance signal. As a result, the signal at the output (Pin 28) has a burst-to-chrominance ratio which is 6dB lower than that of the input signal when the saturation control is set at −6dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (Pins 22 and 23). These signals are fed to the burst phase detector. In the case of NTSC, the chroma signal is internally coupled to the demodulators, ACC, and phase detector.

### Oscillator and Identification Circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (Pin 7). In the detector, the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared to the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at Pins 24 and 25, and is also applied to the 8.8MHz oscillator. The 4.4MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the ACC. To avoid 'blooming-up' of the picture under weak input signal conditions, the ACC voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (Pin 5) provides a delayed switch-on after killing.

Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between Pins 24 and 25 (see Figure 6). With this application, the trimmer capacitor in series with the 8.8MHz crystal (Pin 26) can be replaced by a fixed value capacitor to compensate for imbalance of the phase detector.

### Demodulator

The (R-Y) and (B-Y) demodulators are driven by the color difference signals from the delay-line matrix circuit and the reference signals from the 8.8MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G matrix. The demodulation circuits are killed and blanked by bypassing the input signals.

### NTSC Mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (Pins 24 and 25) is adjusted below 9V. To ensure reliable application, the phase detector load resistors are external. When the TDA3566 is used only for PAL, these two 33kΩ resistors must be connected to +12V (see Figure 6). For PAL/NTSC application, the value of each resistor must be reduced to 10kΩ and connected to the slider of a potentiometer (see Figure 7). The switching transistor brings the voltage at Pins 24 and 25 below 9V, which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal.)

Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at Pins 24 and 25 between 7.5V and 8.5V, nominal position 8.0V. The hue control characteristic is shown in Figure 4.

### RGB Matrix and Amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described. The luminance and the color difference signals are added in the matrix circuit to obtain the color signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to Pin 6 (high-input impedance). The control range is +3dB to −17dB nominal. The relationship between the control voltage and the gain is linear (see Figure 1).

During the 3-line period after blanking, a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at Pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1V to 3V.

While this offset level is present, the 'black-current' input impedance (Pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at Pin 19 with the voltage developed across the external resistor network $R_A$ and $R_B$ (Pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from Pins 10, 20, and 21 to ground, which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to Pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10V. When the signal tends to exceed this level, the output signal is clipped. The black level at the outputs (Pins 13, 15, and 17) will be about 3V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used, it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (Pin 18) via a resistor network.

## Data Insertion

Each color amplifier has a separate input for data insertion. A $1V_{P-P}$ input signal provides a $4V_{P-P}$ output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore, AC coupling is required for the data inputs.

To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150Ω.

The data insertion circuit is activated by the data blanking input (Pin 9). When the voltage at this pin exceeds a level of 0.9V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid colored edges, the data blanking switching time is short.

The amplitude of the data output signals is controlled by the contrast control at Pin 6. The black level is equal to the video black level and can be varied between 2 and 4V (nominal condition) by the brightness control voltage at Pin 11. Non-synchronized data signals do not disturb the black level of the internal signals.

## Blanking of RGB and Data Signals

Both the RGB and data signals can be blanked via the sandcastle input (Pin 7). A slicing level of 1.5V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking, a level of +1V is available at the output. To prevent parasitic oscillations on the third overtone of the crystal, the optimal tuning capacitance should be 10pF.

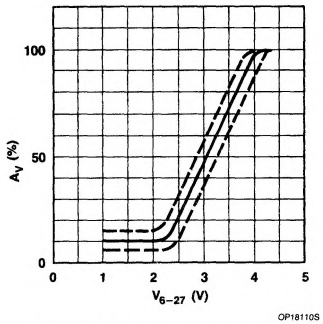



**Figure 1. Contrast Control Voltage Range**

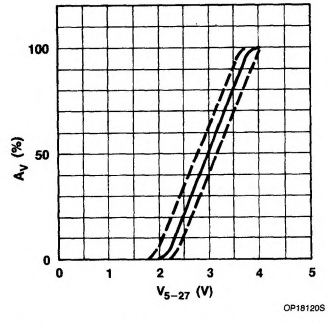



**Figure 2. Saturation Control Voltage Range**

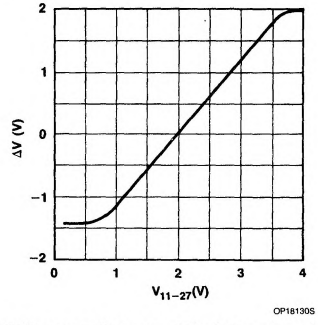



**Figure 3. Difference Between Black Level and Measuring Level at the RGB Outputs (ΔV) as a Function of the Brightness Control Input Voltage ($V_{11-27}$)**

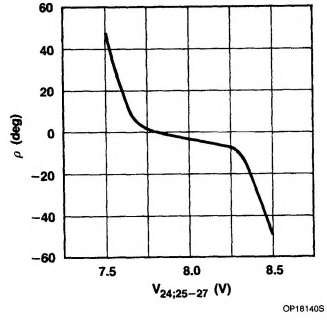



**Figure 4. Hue Control Voltage Range**

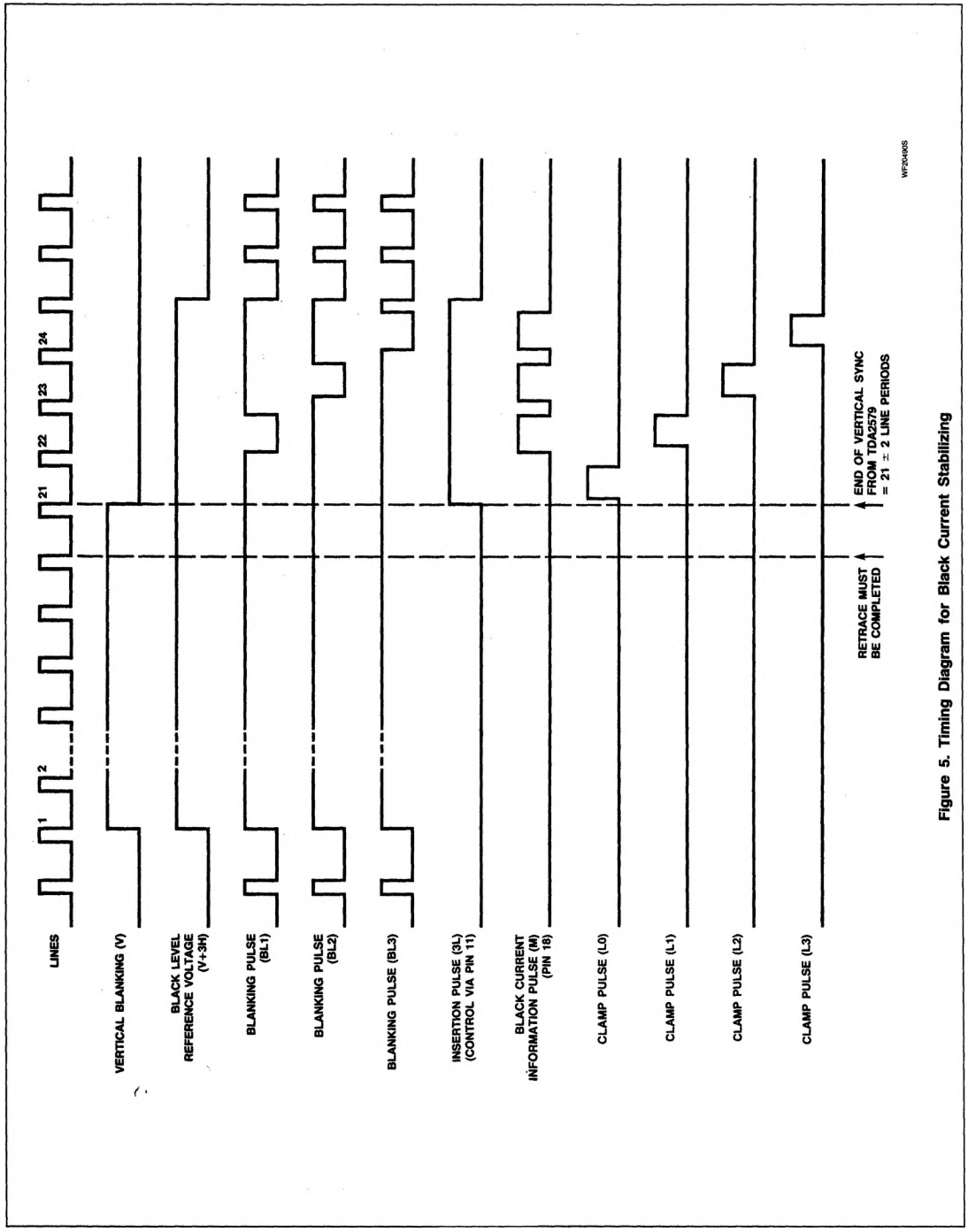
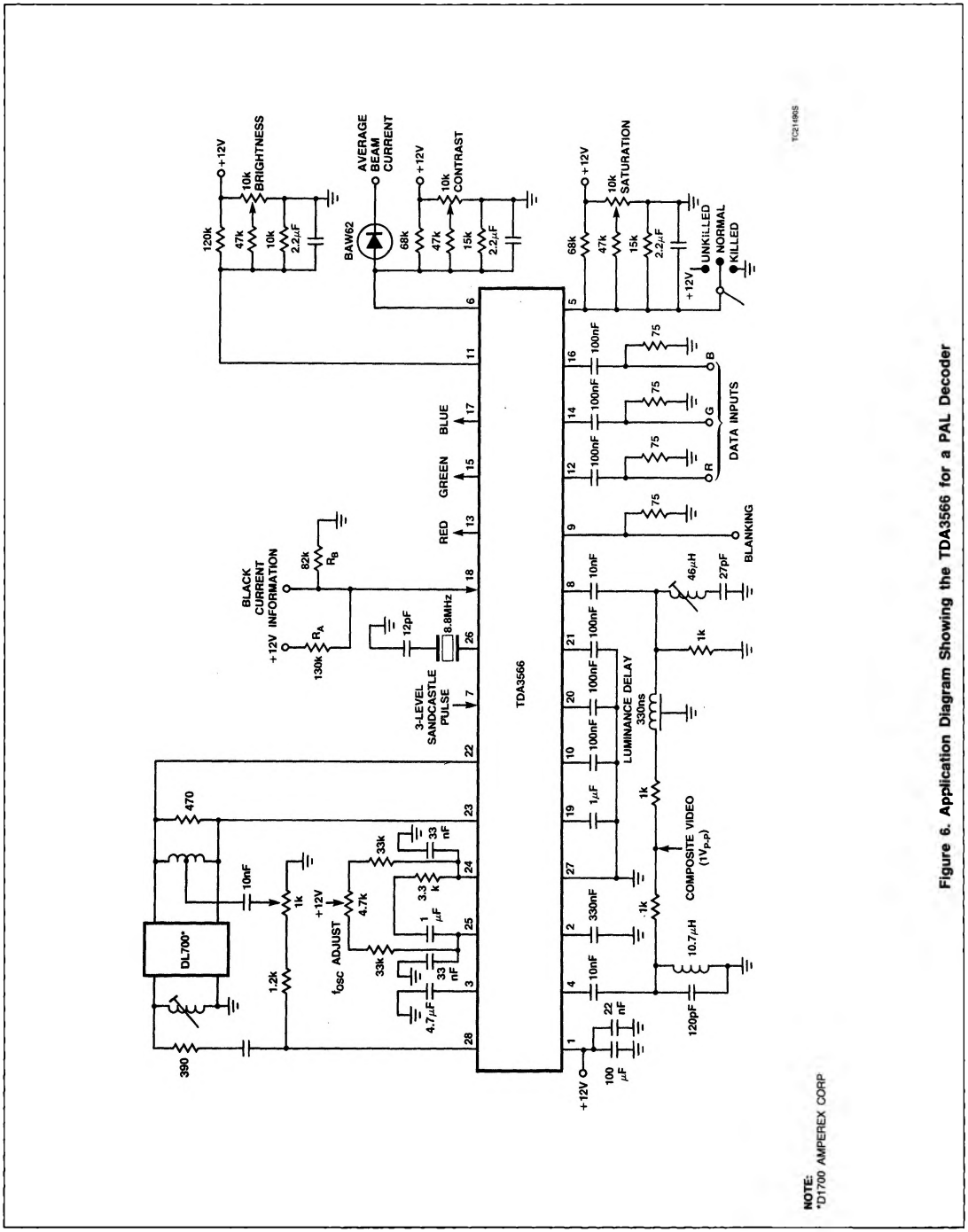



Figure 5. Timing Diagram for Black Current Stabilizing




NOTE:
*DT700 AMPEREX CORP

Figure 6. Application Diagram Showing the TDA3566 for a PAL Decoder

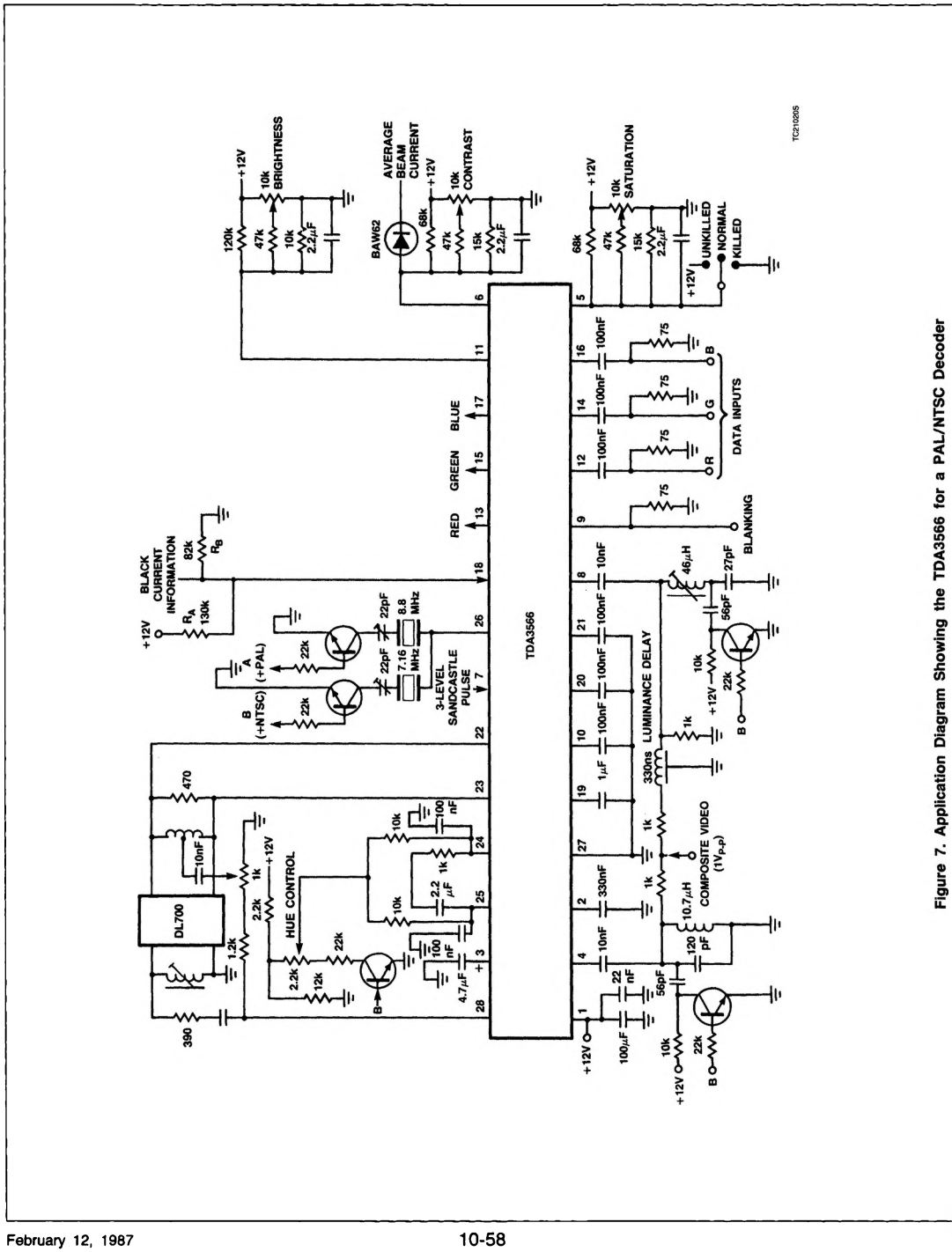
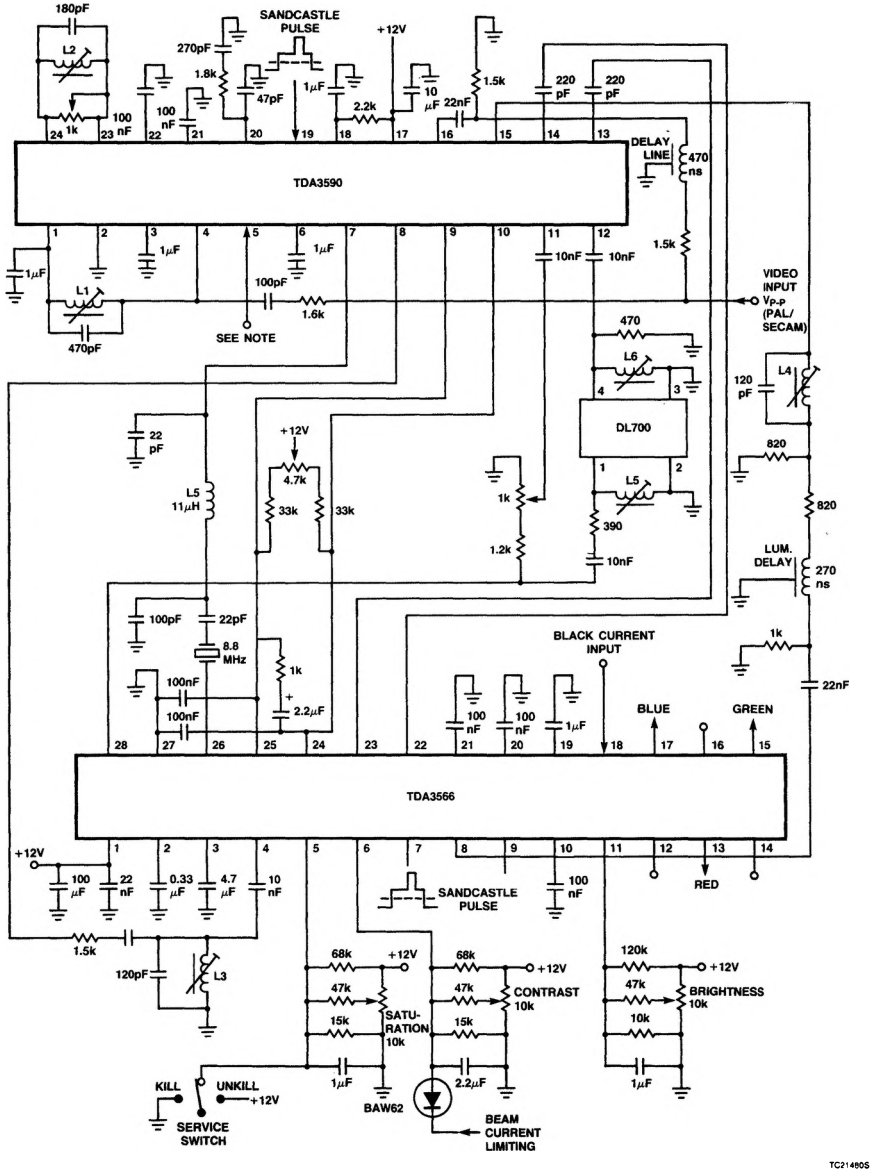



Figure 7. Application Diagram Showing the TDA3566 for a PAL/NTSC Decoder




**NOTES:**
Note to Pin 5 TDA3590:
$V_{5-2} < 1V$; horizontal identification and black level clamping.
$V_{5-2} > 11V$; vertical identification and artificial black level.
$V_{5-2} = 5$ to 7V; horizontal identification and artificial black level.

**Figure 8. PAL/SECAM Application Circuit Diagram Using the TDA3590 and TDA3566**