Signetics

TDA4505

Small-Signal Subsystem IC for Color TV

Preliminary Specification

Linear Products

DESCRIPTION

The TDA4505 is a TV subsystem circuit intended to be used for base-band demodulation applications. This circuit consists of all small-signal functions (except the tuner) required for a quality color television receiver. The only additional circuits needed to complete a receiver are a tuner, the deflection output stages, and a color decoder. The TDA3563 or 67, NTSC color decoder, and the TDA3654 vertical output, are ideal complements for the TDA4505.

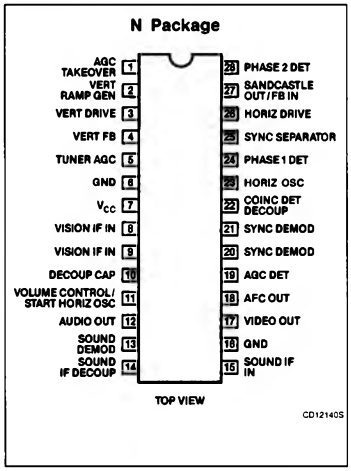
FEATURES

- **Vision IF amplifier with synchronous demodulator**
- **Tuner AGC (negative-going control voltage with increasing signal)**
- **AGC detector for negative modulation**
- **AFC circuit**
- **Video preamplifier**
- **Sound IF amplifier, demodulator and preamplifier**
- **DC volume control**
- **Horizontal synchronization circuit with two control loops**
- **Extra time constant switches in the horizontal phase detector**
- **Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 or 60Hz**
- **Three-level sandcastle pulse generation**

APPLICATIONS

- **Color television receiver**
- **CATV converters**
- **Base-band processing**

PIN CONFIGURATION



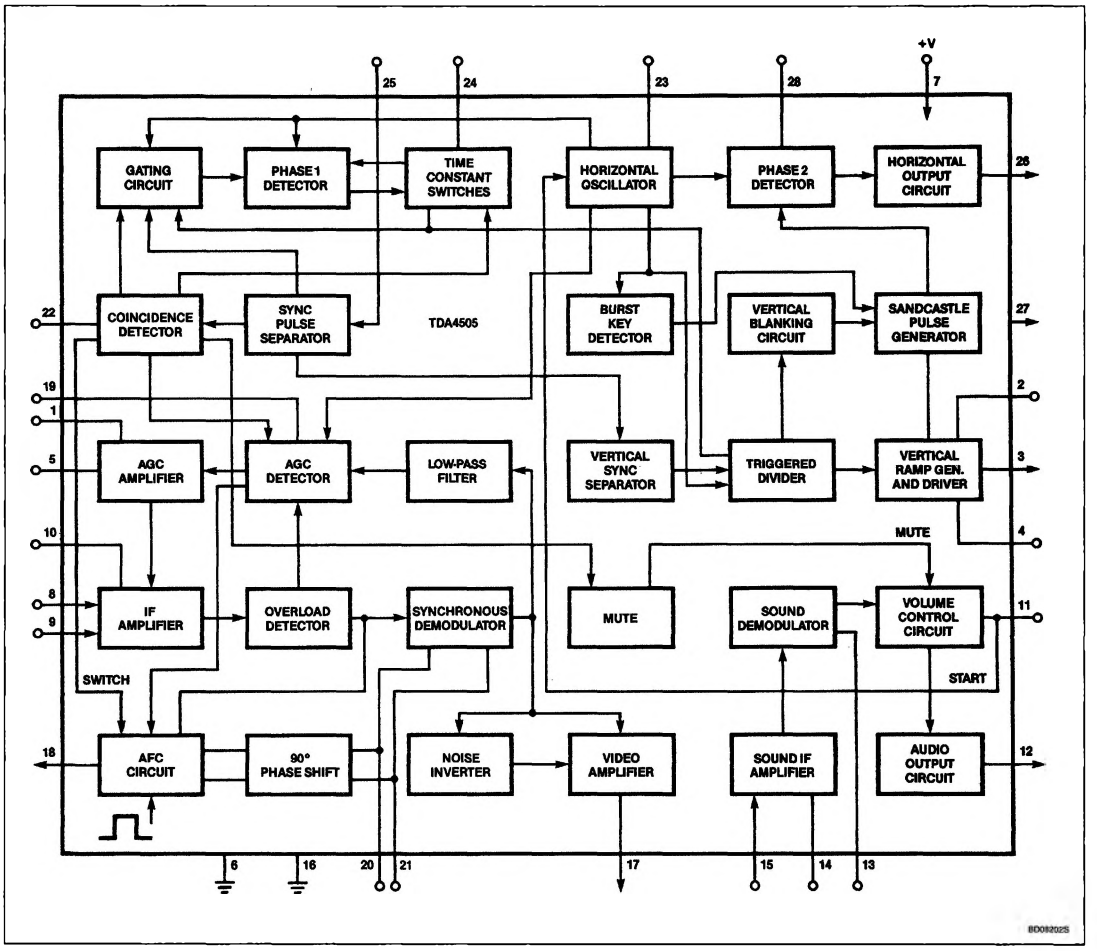
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4505N
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4505AN
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4505BN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 7)	13.2	V
P_{TOT}	Total power dissipation	2.3	W
T_A	Operating ambient temperature range	−25 to +65	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
V_{7-6}	Supply voltage (Pin 7)	9.5	12	13.2	V
I_7	Supply current (Pin 7)		135		mA
V_{11-6}	Supply voltage (Pin 11)[1]		8.6		V
I_{11}	Supply current (Pin 11) for horizontal oscillator start		6	8	mA
Vision IF amplifier (Pins 8 and 9)					
V_{8-9}	Input sensitivity 38.9MHz on set AGC	60	100	140	μV
V_{8-9}	45.75MHz on set AGC		120		μV
R_{8-9}	Differential input resistance (Pin 8 to 9)	800	1300	1800	Ω
C_{8-9}	Differential input capacitance (Pin 8 to 9)		5		pF
G_{8-9}	Gain control range	56	60		dB
V_{8-9}	Maximum input signal	50	100		mV
ΔV_{17-6}	Expansion of output signal for 50dB variation of input signal with V_{8-9} at 150μV (0dB)		1		dB
Video amplifier measured at top sync input signal voltage (RMS value) of 10mV					
V_{17-6}	Output level for zero signal input (zero point of switched demodulator)		5.8		V
V_{17-6}	Output signal top sync level[2]	2.7	2.9	3.1	V
$V_{17-6(P-P)}$	Amplitude of video output signal (peak-to-peak value)		2.6		V
$I_{17(INT)}$	Internal bias current of output transistor (NPN emitter-follower)	1.4	2.0		mA
BW	Bandwidth of demodulated output signal	5			MHz
G_{17}	Differential gain (Figure 3)[3]		4	10	%
φ	Differential phase (Figure 3)[3]		3	10	deg.
	Video non-linearity[4] complete video signal amplitude			10	%
	Intermodulation (Figure 4) at gain control = 45dB				
	f = 1.1MHz; blue	55	60		dB
	f = 1.1MHz; yellow	50	54		dB
	f = 3.3MHz; blue	60	66		dB
	f = 3.3MHz; yellow	55	59		dB
	Signal-to-noise ratio[5]				
S/N	$Z_S = 75Ω$; $V_I = 10mV$	50	54		dB
S/N	end of gain control range	50	56		dB
	Residual carrier signal		7	30	mV
	Residual 2nd harmonic of carrier signal		24	30	mV

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuner AGC[13]					
$V_{1-6(RMS)}$	Minimum starting point take-over			0.5	mV
$V_{1-6(RMS)}$	Maximum starting point take-over	50	100		mV
I_{5MAX}	Maximum output swing	6	8		mA
$V_{5-6(SAT)}$	Output saturation voltage I = 2mA			300	mV
I_5	Leakage current			1	μA
ΔV_I	Input signal variation complete tuner control (ΔI_5 = 2mA)	0.5	2	5	dB
AFC circuit (Pin 18)[6]					
$V_{18-6(P-P)}$	AFC output voltage swing	9.5	10.35	11	V
$\pm I_{18}$	Available output current		2.6		mA
	Control steepness		70		mV/kHz
V_{18-6}	Output voltage at nom. tuning of the reference-tuned circuit		6		V
I_{18}	Offset current AFC output (Pins 20 and 21 short-circuited)		TBD		μA
Sound circuit					
V_{15LIM}	Input limiting voltage $V_O = V_{O\ MAX} - 3dB$; $Q_L = 16$; $f_{AF} = 1kHz$; $f_C = 5.5MHz$		400	800	μV
R_{15-6}	Input resistance $V_{I(RMS)} = 1mV$		2.6		kΩ
C_{15-6}	Input capacitance $V_{I(RMS)} = 1mV$		6		pF
AMR AMR	AM rejection (Figures 7 and 8) $V_I = 10mV$ $V_I = 50mV$		46 50		dB dB
$V_{12-6(RMS)}$	AF output signal $\Delta f = 7.5kHz$; minimum distortion	400	600	800	mV
$V_{12-6(RMS)}$	AF output signal; $\Delta f \approx 50kHz$ Pin 11 used as starting pin	300	700	1200	mV
Z_{12-6}	AF output impedance		25	100	Ω
THD	Total harmonic distortion volume control 20dB, $\Delta f = 27.5kHz$; weighted acc. CCIR 468		1	3	%
RR RR	Ripple rejection $f_k = 100Hz$, volume control 20dB when muted		35 30		dB dB
V_{12-6}	Output voltage in Mute condition		3.0		V
S/N	Signal-to-noise ratio; $\Delta f = 27.5kHz$ weighted noise (CCIR 468)		45		dB
Volume control (Figure 8)					
V_{11-6}	Voltage (Pin 11 disconnected)		5.0		V
I_{11}	Circuit (Pin 11 short circuited)		0.9		mA
R_{11-6}	External control resistor		5		kΩ
OSS	Suppression output signal during mute condition		66		dB

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sync separator and first control loop					
$V_{25-6(P-P)}$	Required sync pulse amplitude; $R_{17-25} = 2k\Omega$[7]	200	800		mV
	Input current				
I_{25}	$V_{25-6} > 5V$		10		μA
I_{25}	$V_{25-6} = 0V$		TBD		mA
$\pm \Delta f$	Holding range PLL		1100	1500	Hz
$\pm \Delta f$	Catching range PLL	600	1000		Hz
	Control sensitivity[8]				
	video to oscillator; at weak signal		2.5		kHz/μs
	at strong signal during scan		3.75		kHz/μs
	during vertical retrace and catching		7.5		kHz/μs
Second control loop (positive edge)					
$\Delta t_D/\Delta t_O$	Control sensitivity R_{28-6} = see Figure 1		50		
t_D	Control range		25		μs
Phase adjustment (via second control loop)					
	Control sensitivity		25		μA/μs
α	Maximum allowed phase shift		±2		μs
Horizontal oscillator (Pin 23)					
f_{FR}	Free-running frequency $R = 34k\Omega$; $C = 2.7nF$		15,625		Hz
Δf	Spread with fixed external components		0.4	4	%
Δf_{FR}	Frequency variation due to change of supply voltage from 9.5 to 13.2V		0	0.5	%
TC	Frequency variation with temperature			1×10^{-4}	$°C^{-1}$
Δf_{FR}	Maximum frequency shift			10	%
Δf_{FR}	Maximum frequency deviation at start H-out		8	10	%
Horizontal output (Pin 26)					
V_{26-6}	Output voltage high level			13.2	V
V_{26-6}	Output voltage at which protection commences			15.8	V
V_{26-6}	Output voltage low at $I_{26} = 10mA$		0.15	0.5	V
d	Duty cycle of horizontal output signal at $t_P = 10\mu s$		0.45		
t_R	Rise time of output pulse		260		ns
t_F	Fall time of output pulse		100		ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Flyback input and sandcastle output[9]					
I_{27}	Input current required during flyback pulse	0.1		2	mA
V_{27-6}	Output voltage during burst key pulse	8	9.0		V
V_{27-6}	Output voltage during horizontal blanking	4	4.35	5	V
V_{27-6}	Output voltage during vertical blanking	2.1	2.5	2.9	V
t_W	Width of burst key pulse (60Hz)	3.1	3.5	3.9	µs
t_W	Width of burst key pulse (50Hz)	3.6	4.0	4.4	µs
	Width of horizontal blanking pulse		flyback pulse width		
	Width of vertical blanking pulse 50Hz divider in search window 60Hz divider in search window 50Hz divider in narrow window 60Hz divider in narrow window		 21 17 25 21		 lines lines lines lines
	Delay between start of sync pulse at video output and rising edge of burst key pulse		5.2		µs
Coincidence detector mute output[10]					
V_{22-6}	Voltage for in-sync condition		10.3		V
V_{22-6}	Voltage for no-sync condition no signal		1.5		V
V_{22-6}	Switching level to switch off the AFC		6.4		V
V_{22-6}	Hysteresis AFC switch		0.4		V
V_{22-6}	Switching level to activate mute function (transmitter identification)		2.4		V
V_{22-6}	Hysteresis Mute function		0.5		V
$I_{22(P-P)}$	Charge current in sync condition 4.7µs	0.7	1.0		mA
$I_{22(P-P)}$	Discharge current in sync condition 1.3µs		0.5		mA
Vertical ramp generator[11]					
I_2	Input current during scan		0.5	2	µA
I_2	Discharge current during retrace		0.4		mA
$V_{2-6(P-P)}$	Sawtooth amplitude		0.8	1.1	V
Vertical output (Pin 3)					
I_3	Output current			7	mA
V_{3-6}	Maximum output voltage		5.7		V
Feedback input (Pin 4)					
 V_{4-6} $V_{4-6(P-P)}$	Input voltage DC component AC component (peak-to-peak value)		 3.3 1.2		 V V
I_4	Input current			12	µA
Δt_P	Internal precorrection to sawtooth		5		%
	Deviation amplitude 50/60Hz		0	2	%
Vertical guard[12]					
 ΔV_{4-6} ΔV_{4-6}	Active at a deviation with respect to the DC feedback level; $V_{27-6} = 2.5V$; at switching level low at switching level high		 1.3 1.9		 V V

NOTES:

1. Pin 11 has a double function. When during switch-on a current of 6mA is supplied to this pin, this current is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as volume control. The indicated maximum value is the current at which all ICs will start. Higher currents are allowed: the excess current is bypassed to ground.
2. Signal with negative-going sync top white 10% of the top sync amplitude (Figure 2).
3. Measured according to the test line given in Figure 3.
   — The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   — The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
4. This figure is valid for the complete video signal amplitude (peak white to black).
5. The $S/N = 20 \log \frac{V_{OUT\ BLACK\text{-}TO\text{-}WHITE}}{V_{N(RMS)}}$ at B = 5MHz.
6. The AFC control voltage is obtained by multiplying the IF-output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90° phase shift network. The IF-output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal, the AFC circuit is gated by means of an internally generated gating pulse. As a result the detector is operative only during black level at a constant carrier amplitude which contains no additional side bands. As a result the AFC output voltage contains no video information.
   At very weak input signals, the driver signal for the AFC circuit will contain a lot of noise. This noise signal has again an asymmetrical frequency spectrum and this will cause an offset of the AFC output voltage. To avoid problems due to this effect, the AFC is switched off when the AGC is controlled to maximum gain.
   The measured figures are obtained at an input sign RMS voltage of 10mV and the AFC output loaded with 2 times 220kΩ between $+V_S$ and ground. The unloaded Q-factor of the reference tuned circuit is 70. The AFC is switched off when no signal is detected by the coincidence detector or when the voltage at Pin 22 is between 1.2V and 6.4V. This can be realized by a resistor of 68kΩ connected between Pin 22 and ground.
7. The slicing level can be varied by changing the value of R_{17-25}. A higher resistor value results in a larger value of the minimum sync pulse amplitude. The slicing level is independent of the video information.
8. Frequency control is obtained by supplying a correction current to the oscillator RC-network via a resistor, connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the right frequency in one of the two following ways:
   a) Interrupt R_{23-24}.
   b) Short circuit the sync separator bias network (Pin 25) to $+V_{CC}$.
   To avoid the need of a VCR switch, the time constant of phase detector at strong input signal is sufficient short to get a stable picture during VCR playback. During the vertical retrace period, the time constant is even shorter so that the head errors of the VCR are compensated at the beginning of the scan. Only at weak signal conditions (information derived from the AGC circuit) is the time constant increased to obtain a good noise immunity.
9. The flyback input and sandcastle output have been combined on one pin.
   The flyback pulse is clamped to a level of 4.5V. The minimum current to drive the second control loop is 0.1mA.
10. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
11. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60Hz and corrects the vertical amplitude.
12. To avoid screenburn due to a collapse of the vertical deflection, a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
13. Starting point tuner takeover at 1 = 0.2mA. Takeover to be adjusted with a potentiometer of 47kΩ.

FUNCTIONAL DESCRIPTION

IF Amplifier, Demodulator, and AFC

The IF amplifier has a symmetrical input (Pins 8 and 9). The synchronous demodulator and the AFC circuit share an external reference tuned circuit (Pins 20 and 21). An internal RC-network provides the necessary phase-shifting for AFC operation. The AFC circuit is gated by means of an internally generated gating pulse. As a result, the AFC output voltage contains no video information. The AFC circuit provides a control voltage output with a swing greater than 10V from Pin 18.

AGC Circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC circuit connected to Pin 19. The point of tuner take-over is preset by the voltage level at Pin 1.

Video Amplifier

The signal through the video amplifier comprises video and sound information.

Sound Circuit and Horizontal Oscillator Starting Function

The input to the sound IF amplifier is obtained by a band-pass filter coupling from the video output (Pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (5kΩ) between Pin 11 and ground, or by supplying Pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

DC Volume Control/Horizontal Oscillator Start

The circuit can be used with a DC volume control or with a starting possibility of the horizontal oscillator. The operation depends on the application. When during switch-on no current is supplied to Pin 11, this pin will act as volume control. When a current of 6mA is supplied to Pin 11, the volume control is set to a fixed output signal and the IC will generate drive pulses for the horizontal deflection. The main supply of the IC can then be derived from the horizontal deflection.

Horizontal Synchronization

The video input signal (positive video) is connected to Pin 25.

The horizontal synchronization has two control loops. This has been introduced because a sandcastle pulse had to be generated. An accurate timing of the burstkey pulse can be made in an easy way when the oscillator sawtooth is used. Therefore, the phase of this sawtooth must have a fixed relation with respect to the sync pulse. That can only be realized when a second loop is used.

Horizontal Phase Detector

The circuit has the following operating conditions:

a. Strong input signal, synchronized or not synchronized. (The input signal condition is obtained from the AGC-circuit, the in-sync/out-of-sync from the coincidence detector). In this condition the time constant is optimal for VCR playback; i.e., fast time constant during the vertical retrace (to be able to correct head-errors of the VCR) and such a time constant during scan that fluctuations of the sync are corrected. In this condition the phase detector is not gated.

b. Weak signal. In this condition the time constant is doubled compared with the previous condition. Furthermore, the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by the noise in the video signal.

c. Not synchronized (weak signal). In this condition the time constant during scan and vertical retrace are the same as during scan in condition a.

Vertical Sync Pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of only 10μs with a separation of 22μs. This type of vertical sync pulses are generated by certain video tapes with anti-copy guard.

Vertical Ramp Generator

To avoid problems during VCR-playback in the so-called feature modes (fast or slow), the vertical ramp generator is not coupled to the horizontal oscillator when such signals are received. For normal signals the coupling between vertical ramp generator and horizontal oscillator is maintained. This ensures a reliable interface.

Vertical Divider System

The IC embodies a synchronized divider system for generating the vertical sawtooth at Pin 2. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency; one line period equals 2 clock pulses.

Due to the divider system no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60Hz to 50Hz system. When the trigger pulse comes before line 576 the system works in the 60Hz mode, otherwise 50Hz mode is chosen. The divider system operates with 2 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter.

The counter increases its counter value with 1 for each time the separated vertical sync. pulse is within the search window. When it is not, the counter value is lowered with 1.

The different working modes of the divider system are specified below.

a. Large (search) window: divider ratio between 488 and 722.

This mode is valid for the following conditions:

1. Divider is locking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Non-standard TV signal condition detected while a double or enlarged vertical sync pulse is still found after the internally-generated anti-topflutter pulse has ended. This means a vertical sync pulse width larger than 10 clock pulses (50Hz) viz. 12 clock pulses (60Hz).

   In general this mode is activated for video tape recorders operating in the feature trick mode. When the wide vertical sync. pulses are detected, the vertical ramp generator is decoupled from the horizontal oscillator. As a consequence, the retrace time of this ramp generator is now determined by the external capacitor and the discharge current. This decoupling prevents instability of the picture due to irregular incoming signals (variable number of lines per field).

4. Up/down counter value of the divider system operating in the narrow window mode drops below count 6.

b. Narrow window: divider ratio between 522 - 528 (60Hz) or 622 - 628 (50Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is lowered with 1. At a counter value below 6, the divider system switches over the large window mode. The divider system also generates the so-called anti-topflutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the divider mode a the start is generated at the reset of the divider. In mode b the anti-topflutter pulse starts at the beginning of the first equalizing pulse.

The anti-topflutter pulse ends at count 10 for 50Hz and count 12 for 60Hz. The vertical

blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse width is 34 (17 lines) for 60Hz and at count 42 (21 lines) for 50Hz systems.

The vertical blanking pulse generated at the sandcastle output Pin 27 is made by adding the anti-topflutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b mode. The total length of the vertical blanking in this condition is 21 lines in the 60Hz mode and 25 lines in the 50Hz mode.

Application When External Video Signals Have to Be Synchronized

The input of the sync separator is externally available. For the normal application, the video output signal (Pin 17) is AC-coupled to this input (see Figure 2). It is possible to interrupt this connection and to drive the sync separator from another source; e.g., a teletext decoder in serial mode or a signal coming from the PT-plug. When a teletext decoder is applied, the IF-amplifier and synchronization circuit are running in the same phase so that the various connections between the two parts (like AGC gating) can remain active. When external signals are applied to the sync separator, the connections between the two parts must be interrupted. This can be obtained by connecting Pin 22 to ground.

This results in the following condition:

- AGC detector is not gated.
- AFC circuit is active.
- Mute circuit not active so that the sound channel remains switched-on.
- The first phase detector has an optimal time constant for external video sources.

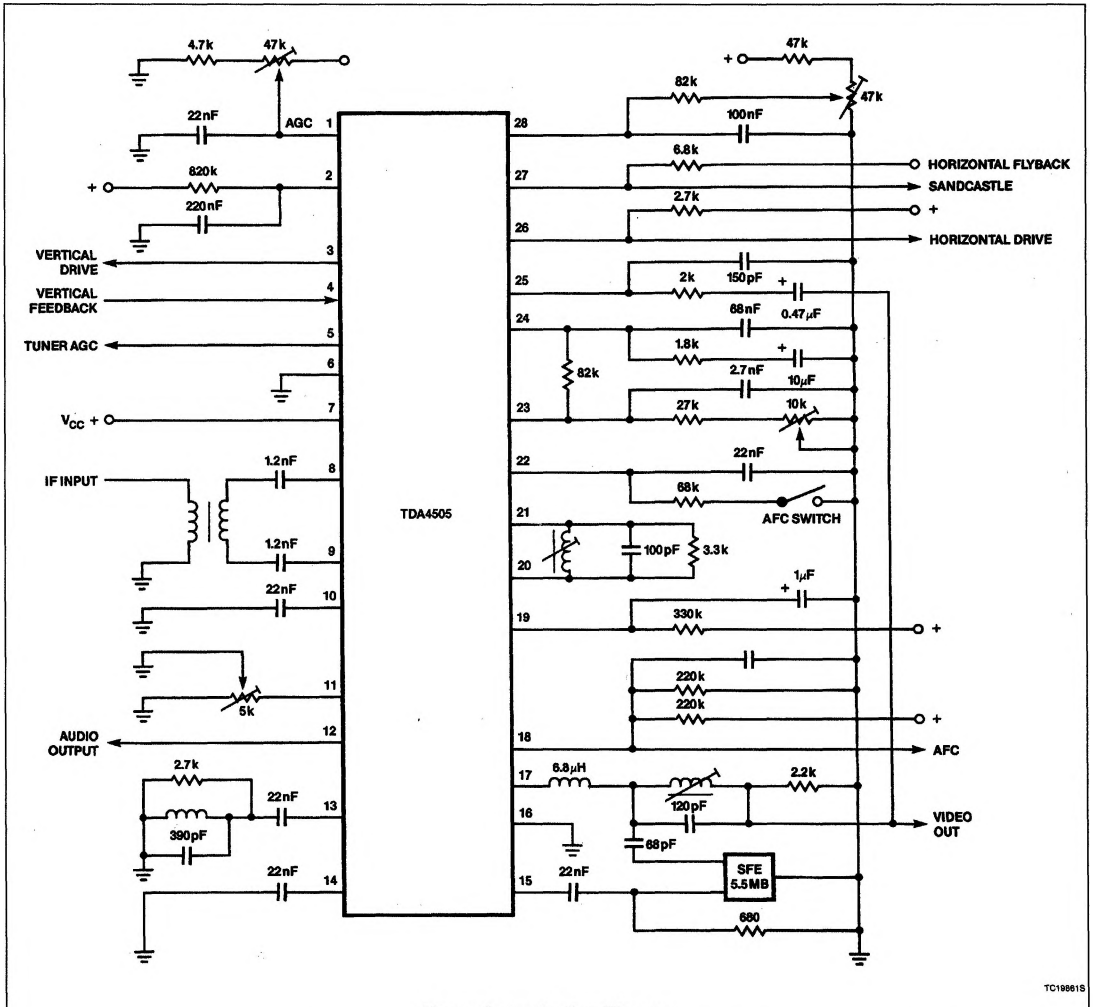


Figure 1. Application Diagram

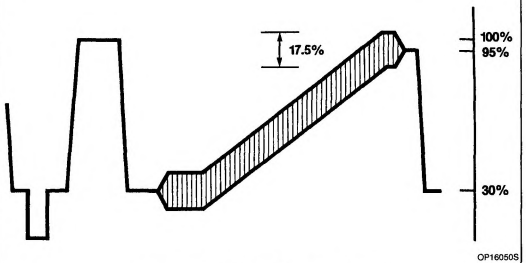


Figure 2. Video Output Signal

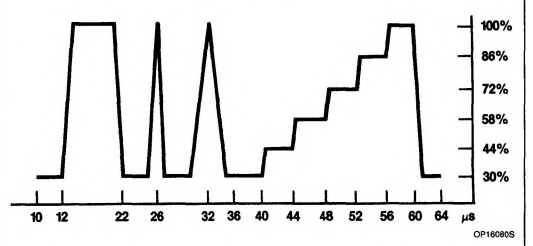
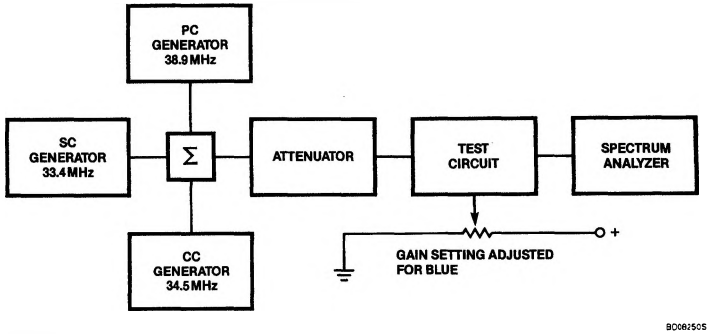


Figure 3. E.B.U. Test Signal Waveform (Line 330)



NOTES:
Value at 1.1MHz; $20\log\frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 1.1MHz} + 3.6dB$.

Value at 3.3MHz; $20\log\frac{V_O \text{ at } 4.4 \text{ MHz}}{V_O \text{ at } 3.3MHz}$.

Figure 4. Test Setup Intermodulation

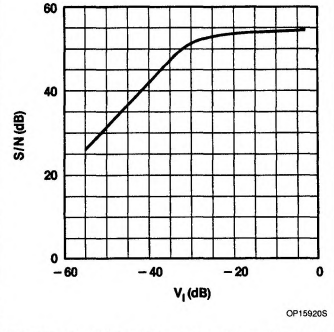


Figure 5. S/N Ratio as a Function of the Input Voltage

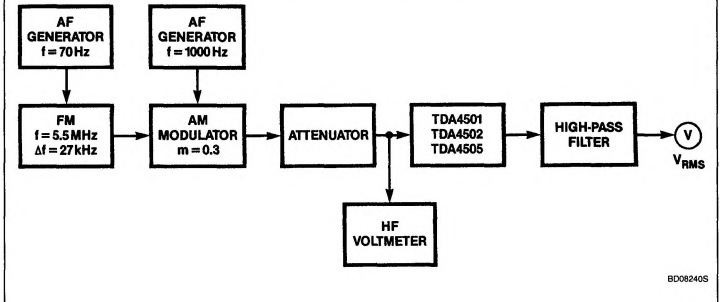


Figure 6. Test Setup AM Suppression

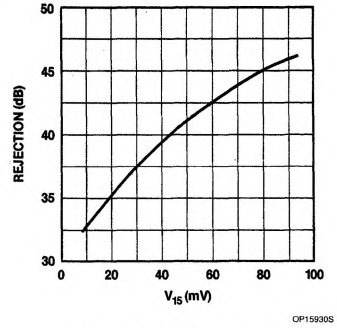


Figure 7. AM Rejection

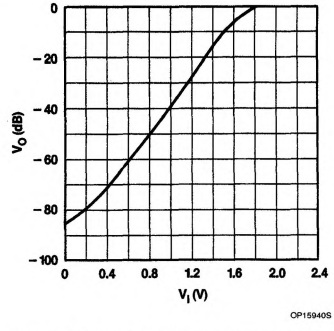


Figure 8. Volume Control Characteristics