COLOR TRANSIENT IMPROVEMENT CIRCUIT — TDA4560

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	typ.	12	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0	dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150	ns
Adjustable Y-delay time	t_d	720 to	1035	ns
Y-attenuation	α_y	typ.	7	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

COLOR TRANSIENT IMPROVEMENT CIRCUIT — TDA4560

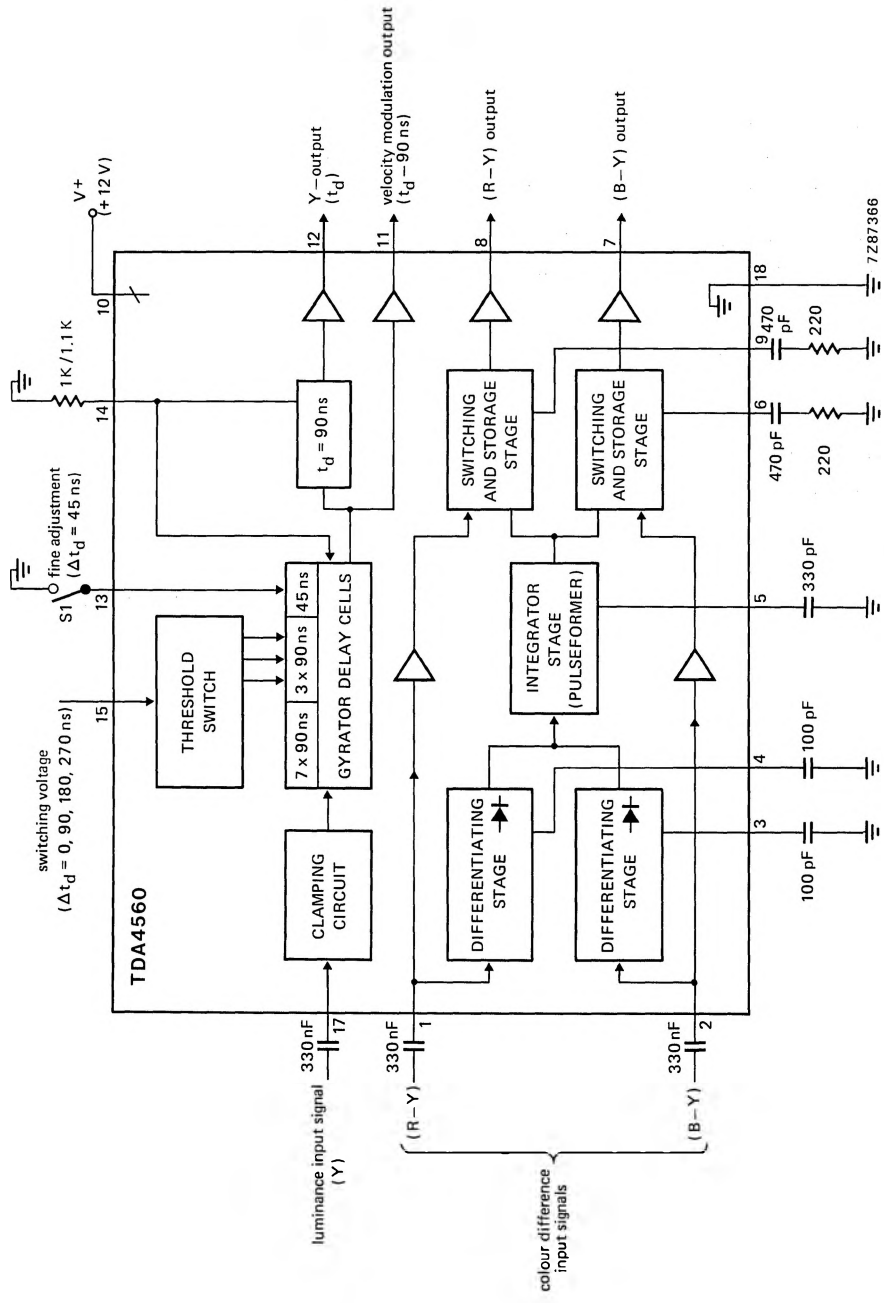


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	max.	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12, 15	$V_{n\text{-}18}$	0 to	V_P	V
at pin 11	$V_{11\text{-}18}$	0 to	$V_P - 3$	V
at pin 17	$V_{17\text{-}18}$	0 to	7	V
Voltages ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$	0 to	5	V
at pin 8 to pin 9	$V_{8\text{-}9}$	0 to	5	V
Currents				
at pins 6, 9	$\pm I_{6,9}$	max.	15	mA
Total power dissipation	P_{tot}	max.	1.1	W
Storage temperature range	T_{stg}	−25 to +	150	°C
Operating ambient temperature range	T_{amb}	0 to +	70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

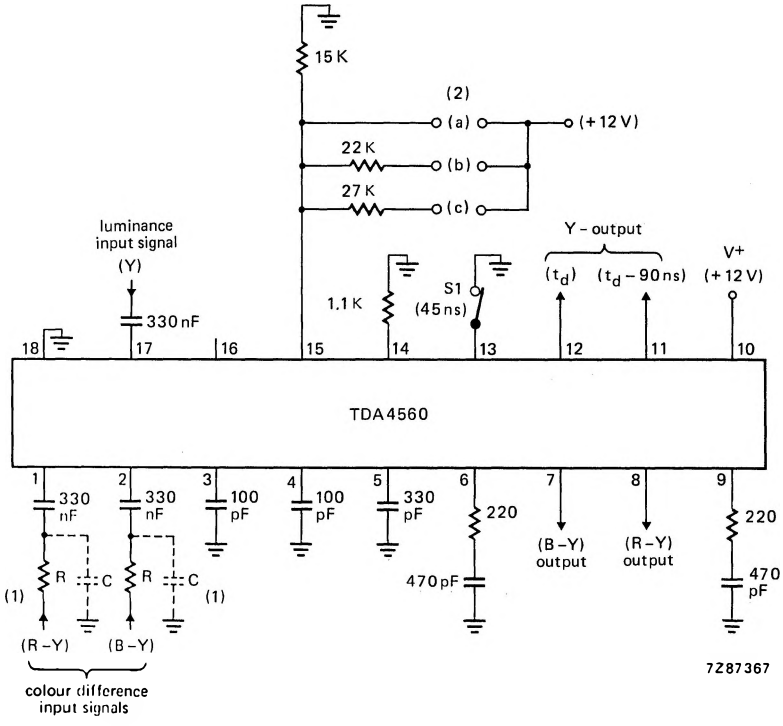
CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	–	12	13.2	V
Supply current	$I_P = I_{10}$	–	35	–	mA
Colour difference channels (pins 1 and 2)					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{1-18}	–	1.05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{2-18}	–	1.33	–	V
Input resistance	$R_{1,\ 2-18}$	–	12	–	kΩ
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output current (emitter follower with constant current source 0.5 mA)	$-I_{7,\ 8}$	–	1.2	–	mA
(R-Y) and (B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Input resistance	R_{17-18}	–	20	–	kΩ
Internal bias voltage	V_{17-18}	–	2.3	–	V
Input current during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}, \frac{V_{12}}{V_{17}}$	α_y	–	7	–	dB
Output current (emitter follower with constant current source 0.4 mA)	$-I_{11,\ 12}$	–	1.2	–	mA
Frequency response ($V_{15-18} = 0$ V) at $R_{14-18} = 1$ kΩ	f_{12-17}	–	6	–	MHz
at $R_{14-18} = 1.1$ kΩ	f_{12-17}	–	4.5	–	MHz

parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17) (continued)					
Adjustable delay (switch S1 open)					
at $V_{15\text{-}18}$ = 0 to 2.5 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	640	–	ns
at $V_{15\text{-}18}$ = 0 to 2.5 V; $R_{14\text{-}18}$ = 1.1 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3.5 to 5.5 V; $R_{14\text{-}18}$ = 1.1 kΩ	t_d	–	810	–	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	800	–	ns
at $V_{15\text{-}18}$ = 6.5 to 8.5 V; $R_{14\text{-}18}$ = 1.1 kΩ	t_d	–	900	–	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	880	–	ns
at $V_{15\text{-}18}$ = 9.5 to 12 V; $R_{14\text{-}18}$ = 1.1 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at $V_{13\text{-}18}$ = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)					
with $R_{14\text{-}18}$ = 1 kΩ	t		t_d – 80 ns		
with $R_{14\text{-}18}$ = 1.1 kΩ	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	–	–	70	K/W

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
X	X	X	0 to 2.5 V	720
X	X	O	3.5 to 5.5 V	810
X	O	O	6.5 to 8.5 V	900
O	O	O	9.5 to 12 V	990

Where: X = connection closed; O = connection open.

* When switch (S1) is closed the delay time is increased by 45 ns.