Signetics

TDA8442
Quad DAC With I²C Interface

Product Specification

Linear Products

DESCRIPTION

The TDA8442 consists of four 6-bit D/A converters and 3 output ports. This IC was designed to provide I²C control, by replacing the potentiometers, for the TDA3560-series single-chip color decoders. Control of the IC is performed via the two-line, bidirectional I²C bus.

FEATURES

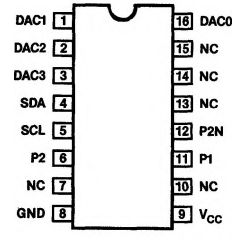
- **6-bit resolution**
- **3 output ports**
- **I²C control**

APPLICATIONS

- **I²C interface control**
- **System control**
- **Switching**

PIN CONFIGURATION

N Package



TOP VIEW

CD12850S

PIN NO.	SYMBOL	DESCRIPTION
1	DAC1	Analog output 1
2	DAC2	Analog output 2
3	DAC3	Analog output 3
4	SDA	Serial data line } I²C bus
5	SCL	Serial clock line } I²C bus
6	P2	Port 2 NPN collector output with internal pull-up resistor
7	NC	Not connected
8	GND	Supply return (ground)
9	V_{CC}	Positive supply voltage
10	NC	Not connected
11	P1	Port 1 open NPN emitter output
12	P2N	Inverted P2 output
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	DAC0	Analog output 0

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−20°C to +70°C	TDA8442N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range (Pin 9)	−0.3 to +13.2	V
	Input/output voltage ranges		
V_{SDA}	(Pin 4)	−0.3 to +13.2	V
V_{SCL}	(Pin 5)	−0.3 to +13.2	V
V_{CC2}	(Pin 6)	−0.3 to V_{CC}[1]	V
V_{CC2N}	(Pin 12)	−0.3 to V_{CC}[1]	V
V_{CC1}	(Pin 11)	−0.3 to V_{CC}[1]	V
V_{DAX}	(Pins 1 to 3 and Pin 16)	−0.3 to V_{CC}[1]	V
P_{TOT}	Total power dissipation	1	W
T_A	Operating ambient temperature range	−20 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Pin voltage may exceed V_{CC} if the current in that pin is limited to 10mA.

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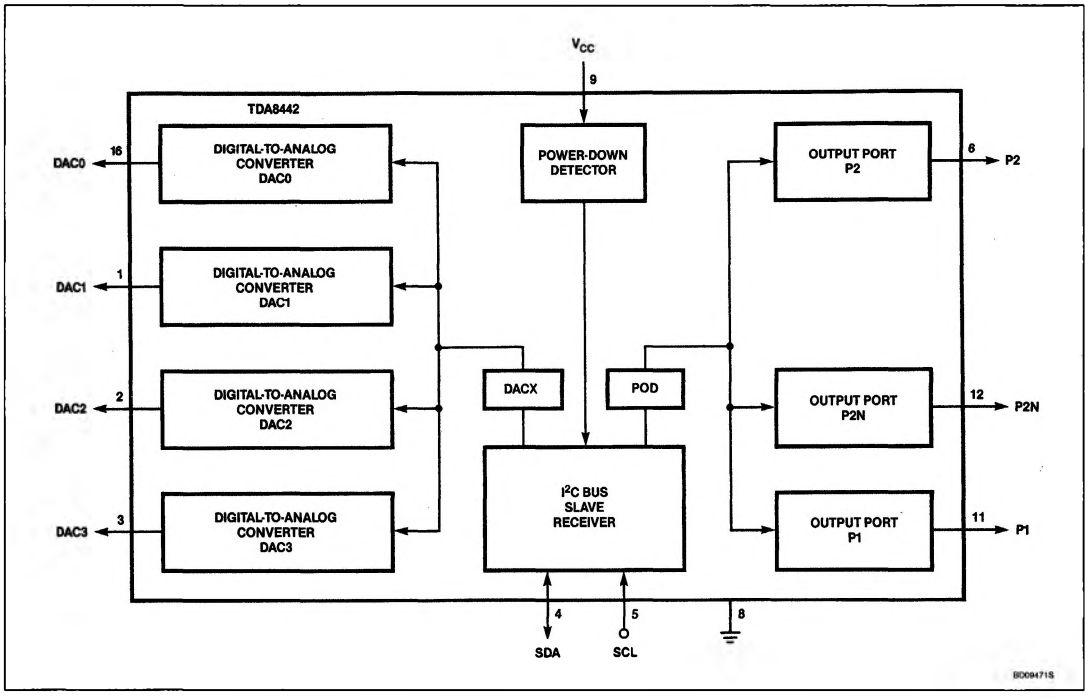
BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
V_{CC}	Supply voltage (Pin 9)	10.8	12	13.2	V
I_{CC}	Supply currents (no outputs loaded) (Pin 9)		12		mA
I²C bus inputs SDA (Pin 4) and SCL (Pin 5)					
V_{IH}	Input voltage High[1]	3		$V_{CC} - 1$	V
V_{IL}	Input voltage Low	−0.3		1.5	V
I_{IH}	Input current High[1]			10	μA
I_{IL}	Input current Low[1]			10	μA
I²C bus output SDA (Pin 4) (open-collector)					
V_{OL}	Output voltage Low at $I_{OL} = 3.0mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
Ports P2 and P2N (Pins 6 and 12) (NPN collector output with pull-up resistor to V_{CC})					
R_O	Internal pull-up resistor to V_{CC}	5	10	15	kΩ
V_{OL}	Output voltage Low at $I_{OL} = 2mA$			0.4	V
I_{OL}	Maximum output sink current	2	5		mA
Port P1 (Pin 11) (open NPN emitter output)					
I_{OH}	Output current High at $0 < V_O < V_{CC} - 1.5V$	14			mA
I_{OL}	Output leakage current at $0 < V_O < V_{CC}V$			100	μA
Digital-to-analog outputs Output DAC0 (Pin 16)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	3			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		100	mV
	Deviation from linearity			150	mV
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA
Output DAC1 (Pin 1)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	4			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1.7	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		120	mV
	Deviation from linearity			170	mV
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Output DAC2 (Pin 2)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	4			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1.7	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		120	mV
	Deviation from linearity			170	mV
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA
Output DAC3 (Pin 3)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	10			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		350	mV
	Deviation from linearity			0.50	V
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA
Power-down reset					
V_{CCD}	Maximum value of V_{CC} at which power-down reset is active	6		10	V
t_R	Rise time of V_{CC} during power-on (V_{CC} rising from 0V to V_{CCD})	5			μs

NOTES:
1. If $V_{CC} < 1V$, the input current is limited to 10μA at input voltages up to 13.2V.
2. Values are proportional to V_{CC}.

FUNCTIONAL DESCRIPTION

Control

Analog control is facilitated by four 6-bit digital-to-analog converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I²C bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open NPN emitter output capable of sourcing 14mA (minimum).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are NPN collector outputs with internal pull-up resistors of 10kΩ (typical). Both outputs are capable of sinking up to 2mA with a voltage drop of less than 400mV. If one output is programmed to be Low, the other output will be High, and vice versa.

Reset

The power-down reset mode occurs whenever the positive supply voltage falls below 8.5V (typical) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C bus. Programming of the TDA8442 is performed using the format shown in Figure 1.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down reset mode (V_{CC} > 8.5V (typ)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analog converter control), and the corresponding data/control bytes (see Figure 2).

POD Bit P1 — If a '1' is programmed, the P1 output is forced High. If a '0' is programmed, or after a power-down reset, the P1 output is Low (high-impedance state).

POD Bit P2/P2N — If a '1' is programmed, the P2 output goes High and the P2N output goes Low. If a '0' is programmed, and after a power-down reset, the P2 output is Low and the P2N output is High.

DAX Bits AX5 to AX0 — The digital-to-analog converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using Bits AX5 to AX0, the lowest value being all AX5 to AX0 data at '0', or when power-down reset has been activated.

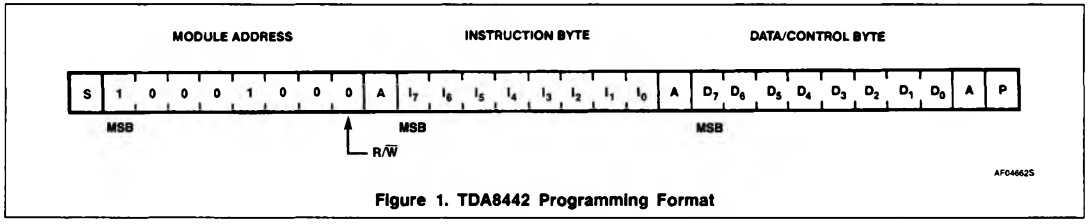


Figure 1. TDA8442 Programming Format

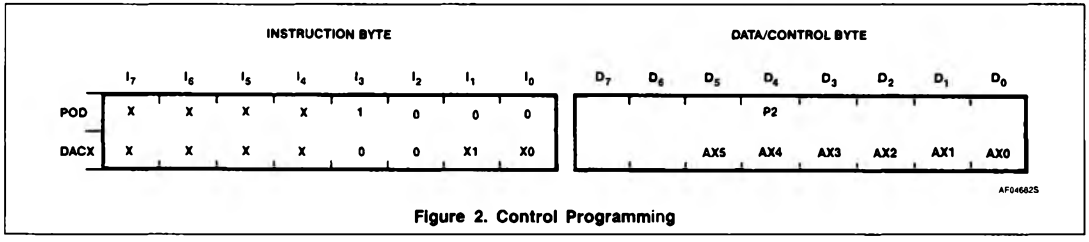
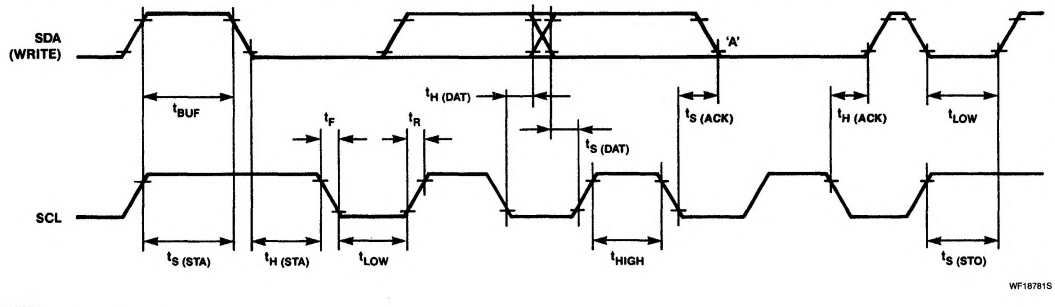


Figure 2. Control Programming

I²C BUS TIMING

Bus loading conditions: 4kΩ pull-up resistor to +5V; 200pF capacitor to GND.
All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			µs
t_{SU}, t_{STA}	Start condition setup time	4			µs
t_{HD}, t_{STA}	Start condition hold time	4			µs
t_{LOW}	Low period SCL, SDA	4			µs
t_{HIGH}	High period SCL	4			µs
t_R	Rise time SCL, SDA			1	µs
t_F	Fall time SCL, SDA			0.30	µs
t_{SU}, t_{DAT}	Data setup time (write)	0.25			µs
t_{HD}, t_{DAT}	Data hold time (write)	0			µs
t_{SU}, t_{ACK}	Acknowledge (from TDA8442) setup time			2	µs
t_{HD}, t_{ACK}	Acknowledge (from TDA8442) hold time	0			µs
t_{SU}, t_{STO}	Stop condition setup time	4			µs



NOTE:
Reference levels are 10 and 90%.

Figure 3. I²C Bus Timing, TDA8442