CMOS 8-Bit Microcontroller

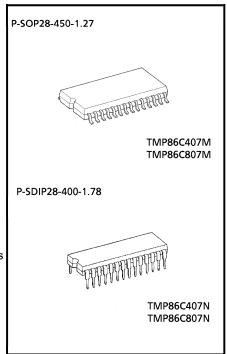
TMP86C407M/N, TMP86C807M/N

The TMP86C407/807 are high speed and high performance 8-bit single chip microcomputers with small package. The MCU contain CPU core, ROM, RAM, multirole timer counter, SEI and UART, 8-bit AD converter, and two clock generators on a chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86C407M	4 Kbytes		D COD20 450 4 27	TN 4D0CD007N4
TMP86C807M	8 Kbytes	2561-1	P-SOP28-450-1.27	TMP86P807M
TMP86C407N	4 Kbytes	256 bytes	D CD ID00 400 4 70	TN 4D0CD007N
TMP86C807N	8 Kbytes		P-SDIP28-400-1.78	TMP86P807N

Features

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- ♦ Instruction execution time: $0.25 \mu s$ (fc = 16 MHz) $122 \,\mu s \, (fs = 32.768 \, kHz)$
- ◆ 132 types and 731 basic instructions
- ◆ Interrupt sources: 18 factors (External: 5, Internal: 13)
- ◆ Input/Output ports: 22 pins
- 16-bit timer/counter: 1 ch
 - Timer, PPG output, Pulse width measurement, Pulse duty measurement, Event counter
- ▶ 8-bit timer/counter: 2 ch
 - Timer, PDO output, Event counter, PWM output, PPG modes
- Time Base Timer
- Divider output function
- Watchdog Timer
 - Interrupt source/Internal Reset (programmable)



- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter
- entitled Quality and Reliability Assurance / Handling Precautions.
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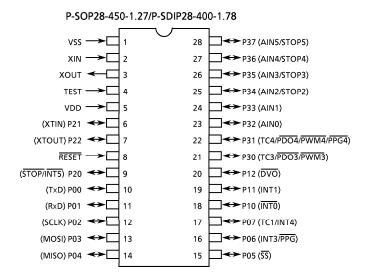
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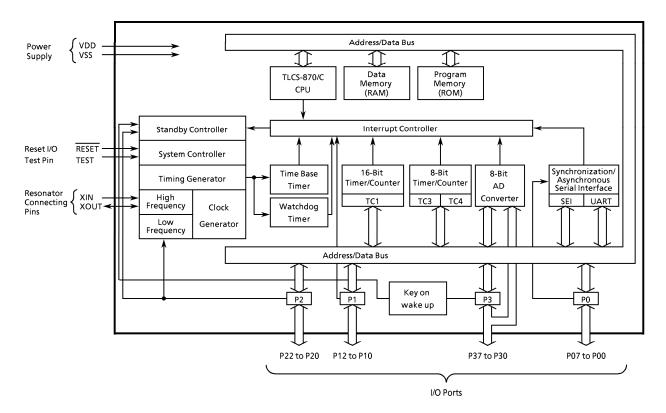
86C407-1 2002-11-27

- ◆ Serial interface
 - SEI (MSB/LSB Max: 4 Mbps at 16 MHz)
 - 8-bit UART: 1ch
- ◆ 8-bit successive approximate type AD converter
 - Analog input: 6 ch
- ♦ Key On Wake Up: 4 ch
- ◆ Power saving operating modes (9 modes)
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW 1 mode: Low power consumption operation using low-frequency clock (High-frequency stop)
 - SLOW 2 mode: Low power consumption operation using low-frequency clock (High-frequency run)
 - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer.
 - Release by INTTBT interrupt.
 - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock.
 - Release by interrupts.
 - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock.
 - Release by interrupts.
 - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer.
 - Release by INTTBT interrupt.
 - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock.
 - Release by interrupts.
 - SLEEP 2 mode: CPU stops, and peripherals operate using high and low-frequency clock.
 - Release by interrupts.
- ◆ Dual clock operation
- ◆ Wide operating voltage: 2.7 to 5.5 V at 8 MHz/32.768 kHz,
 - 4.5 to 5.5 V at 16 MHz/32.768 kHz

Pin Assignments (Top View)



Block Diagram



Pin Functions

Pin Name	Input/Output	F	unction		
P07 (TC1, INT4)	I/O (I/O)		Timer/Counter 1 input/External interrupt input 4		
P06 (INT3, PPG)	I/O (I/O)		External interrupt input 3/PPG output		
P05 (SS)	I/O (Input)	8-bit programmable input/output ports. Each bit of these ports can be	SEI master slave change input		
P04 (MISO)	I/O (I/O)	individually configured as an input or	SEI master input, slave output		
P03 (MOSI)	I/O (I/O)	output under software control. When used as function, the latch must be	SEI master output, slave input		
P02 (SCLK)	I/O (I/O)	set to 1.	SEI serial clock input/output pin		
P01 (RxD)	I/O (Input)	Nch O.D output function.	UART data input		
P00 (TxD)	I/O (Output)		UART data output		
P12 (DVO)	I/O (Output)	3-bit programmable input/output ports (tri-state). Each bit of these ports	Divider output		
P11 (INT1)	I/O (Input)	can be individually configured as an input or output under software control.	External interrupt input 1		
P10 (ĪNTO)	I/O (Input)	When used as function, the latch must be set to 1.	External interrupt input 0		
P22 (XTOUT)	I/O (Output)		Resonator connecting pins (32.768 kHz)		
P21 (XTIN)	I/O (Input)	3-bit programmable input/output ports. When used as input port and function,	For inputting external clock, XTIN is used and XTOUT is opened.		
P20 (INT5, STOP5)	I/O (Input)	the latch must be set to 1.	External interrupt input 5 or STOP mode release signal input		
P37 (AIN5, STOP5)	I/O (Input)		STOP mode release signal input 5		
P36 (AIN4, STOP4)	I/O (Input)		STOP mode release signal input 4		
P35 (AIN3, STOP3)	I/O (Input)	8-bit programmable input/output ports	STOP mode release signal input 3 AD converter		
P34 (AIN2, STOP2)	I/O (Input)	(tri-state). Each bit of these ports can be	STOP mode release signal input 2 analog input		
P33 (AIN1)	I/O (Input)	individually configured as an input or output under software control.			
P32 (AIN0)	I/O (Input)	When used as function and analog			
P31 (TC4, PDO4, PWM4, PPG4)	1/0 (1/0)	inputted latch must be set to 1.	Timer/Counter 4 input, PDO, PWM, PPG output		
P30 (TC3, PDO3, PWM3)	I/O (I/O)		Timer/Counter 3 input, PDO, PWM output		
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequused and XOUT is opened.	ency clock. For inputting external clock, XIN is		
RESET	Input	RESET signal input			
TEST	Input	TEST pin for out-going test. Be fixed to low			
VDD, VSS	Power Supply	+ 5 V, 0 (GND)			

Under Development

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C407/807 memory consist of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C407/807 memory address map. The general-purpose register banks are not assigned to the RAM address space.

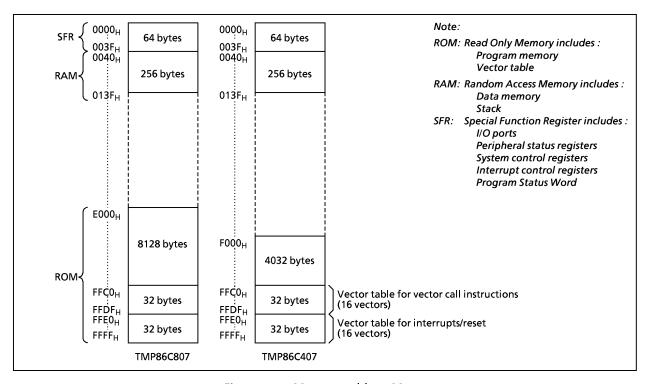


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86C407 has a 4 K×8 bits (address $F000_H$ to $FFFF_H$), TMP86C807 has a 8 K×8 bits (address $E000_H$ to $FFFF_H$) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Electrical Characteristics

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	
Output Valtage	V _{OUT1}	P21, P22, RESET, Tri-state Port	– 0.3 to V _{DD} + 0.3	V
Output Voltage	V_{OUT2}	P20, Sink Open Drain Port	– 0.3 to 5.5	
	I _{OUT1} I _{OH}	P0, P1, P3 Port	- 1.8	
Output Current (Per 1 pin)	I _{OUT2} I _{OL}	P1, P2, P3 Port	3.2	
	I _{OUT3} I _{OL}	P0 Port	30	mΑ
	Σ I _{OUT1}	P0, P1, P3 Port	- 30	ША
Output Current (Total)	Σ I _{OUT2}	P1, P2, P3 Port	60	
	Σ I _{OUT3}	P0 Port	80	
Power Dissipation [T _{opr} = 85°C]	PD		145	mW
Soldering Temperature (time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 150	°C
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins		Condition	Min	Max	Unit
				NORMAL1, 2 mode	4.5		
			fc = 16 MHz	IDLE0, 1, 2 mode	4.5		
				NORMAL1, 2 mode			
Supply Voltage	V_{DD}		fc = 8 MHz	IDLE0, 1, 2 mode		5.5	
			fs =	SLOW1, 2 mode	2.7		
			32.768 kHz	SLEEP0, 1, 2 mode			
				STOP mode			V
	V _{IH1}	Except Hysteresis input	$V_{DD} \ge 4.5 \text{ V}$ $V_{DD} < 4.5 \text{ V}$		$V_{DD} \times 0.70$		
Input high Level	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$	V_{DD}	
	V _{IH3}				$V_{DD} \times 0.90$		
	V_{IL1}	Except Hysteresis input		, > A E V		$V_{DD} \times 0.30$	
Input low Level	V_{IL2}	Hysteresis input	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	_{DD} ≥ 4.5 V	0	$V_{DD} \times 0.25$	
	V_{IL3}		V	_{'DD} < 4.5 V		$V_{DD} \times 0.10$	
	fc XIN, XOUT		V _{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
Clock Frequency			V _{DD} = 4.5 to 5.5 V		1.0	16.0	IVITZ
	fs	XTIN, XTOUT	V _{DD}	= 2.7 to 5.5 V	30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Standard

DC Characteristics $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		_	0.9	-	٧
Input Current	I _{IN1}	TEST Sink Open Drain, Tri-state Port	V _{DD} = 5.5 V, V _{IN} = 5.5 V/0 V	_	_	± 2	μΑ
	I _{IN3}	RESET, STOP					
Input Resistance	R _{IN1}	TEST Pull-Down		_	70	_	kΩ
input resistance	R _{IN2}	RESET Pull-Up		100	220	450	KAZ
Output Leakage Current	I _{LO}	Sink Open Drain, Tri-state Port	$V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V/0 V}$	-	-	± 2	μΑ
Output High Voltage	V_{OH}	P0, P1, P3 Port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	_	-	_
Output Low Voltage	V_{OL}	P1, P2, P3 Port	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	_	0.4	\ \
Output Low Current	I_{OL}	High Current Port (P0 Port)	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	_	20	-	
Supply Current in			V _{DD} = 5.5 V	_	7.5	9.0	mA
NORMAL 1, 2 mode			V _{IN} = 5.3/0.2 V		7.5	9.0	'''^
Supply Current in IDLE 0, 1, 2 mode			fc = 16.0 MHz fs = 32.768 kHz	-	5.5	6.5	
Supply Current in SLOW 1 mode				-	14.0	25.0	
Supply Current in SLEEP 1 mode	l _{DD}		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$ $fs = 32.768 \text{ kHz}$	_	7.0	15.0	
Supply Current in SLEEP 0 mode			15 = 32.700 KMZ		6.0	15.0	μΑ
Supply Current in STOP mode			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	_	0.5	10.0	

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 \text{ V}$

Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The power supply current in STOP2 and SLEEP2 modes each are the same as in IDLE0, 1, and 2 modes.

AD Conversion Characteristics

 $(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V} \le V_{DD} \le 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Input Voltage	V _{AIN}		V _{SS}	_	V_{DD}	٧
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = 5.5 V$ $V_{SS} = 0.0 V$	_	0.6	1.0	mA
Non linearity Error			-	_	± 1	
Zero Point Error		$V_{DD} = 5.0 V$,	-	_	± 1	LSB
Full Scale Error		$V_{DD} = 5.0 \text{ V},$ $V_{SS} = 0.0 \text{ V}$	-	_	± 1	"35
Total Error			-	_	± 2	

 $(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V} \le V_{DD} < 4.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Input Voltage	V _{AIN}		V _{SS}	-	V_{DD}	٧
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = 4.5 V$ $V_{SS} = 0.0 V$	-	0.5	0.8	mA
Non linearity Error			-	-	± 1	
Zero Point Error		$V_{DD} = 2.7 \text{ V},$ $V_{SS} = 0.0 \text{ V}$	-	-	± 1	LSB
Full Scale Error		$V_{SS} = 0.0 V$	-	-	± 1	"35
Total Error			-	-	± 2	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.
 About conversion time, please refer to "2.10.2 Register Configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of V_{DD} V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: The relevant pin for I_{REF} is V_{DD} , so that the current flowing into V_{DD} is the power supply current $I_{DD} + I_{REF}$.

SEI Operating Conditions (Slave mode)

(V_{SS} = 0.0 V, 2.7 V \leq V_{DD} \leq 5.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Transfer Rate			15.625 k	1	fc/4	bps

AC Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode				
Machine Cycle Time	4.00	IDLE 0, 1, 2 mode	0.25	_	4	_
	tcy	SLOW 1, 2 mode	447.6	-	133.3	μS
		SLEEP 0, 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	_			ns
Low Level Clock Pulse Width	twcL	fc = 16 MHz	25	-	_	''3
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	147			
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz	14.7	_	_	μS

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode			4	
Machine Cycle Time	tou	IDLE 0, 1, 2 mode	0.5	_		
	ιcy	SLOW 1, 2 mode			422.2	μS
		SLEEP 0, 1, 2 mode	117.6	_	133.3	
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz	50	_	_	''3
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	14.7	_	-	
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz				μS

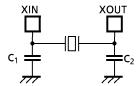
Recommended Oscillation Conditions-1

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_{ODT} = -40 \text{ to } 85^{\circ}\text{C})$$

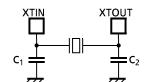
Doromotor	Resonator	Oscillating	Pocomr	nended Resonator	Recommended Constant		
Parameter	Resortator	Frequency	Kecomi	iended Resonator	C ₁	c ₂	
		16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF	
High frameson		0.0411-	MURATA	CSA8.00MTZ	30 pF	30 pF	
High-frequency oscillation	Ceramic resonator	8 MHz		CST8.00MTW	30 pF (built-in)	30 pF (built-in)	
oscillation			MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)	
Low-frequency oscillation	Crystal resonator	32.768 kHz	SII	VT-200	6 pF	6 pF	

Recommended Oscillation Conditions-2
$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, T_{opr} = -40 \text{ to } 85^{\circ}\text{C})$$

Darameter	Parameter Resonator		Recomn	Recommended Resonator		ed Constant
Parameter	Resortator	Frequency	Recommended Resonator		c ₁	C ₂
	0.8411	MURATA	CSA8.00MTZ	30 pF	30 pF	
High-frequency	C	8 MHz		CST8.00MTW	30 pF (built-in)	30 pF (built-in)
oscillation Ceramic resonator		MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.
- Note 2: To ensure stable oscillation, the resonator position, load capacitance, etc. must be appropriate. Because there factors are greatly affected by board patterns, please be sure to evaluate operation on the board on which the device will actually be mounted.
- Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html