CMOS 8-Bit Microcontroller

TMP86C845U

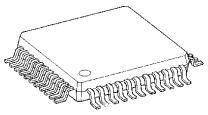
The TMP86C845 is the high-speed, high-performance and low-power consumption 8-bit microcomputer, including ROM, RAM, multi-function timer/counter, serial interface and 10-bit AD converter on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86C845U	8 K × 8 bits	256 × 8 bits	P-LQFP44-1010-0.80A	TMP86PM47U

Features

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.5 μs (at 8 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 15 interrupt sources (External: 6, Internal: 9)
- Input/Output ports (35 pins)
- 8-bit timer counter: 2 ch
  - Timer, PWM, PPG, PDO, Event counter modes
- Time base timer
- Watchdog timer
- Serial interface
  - 8-bit SIO: 1 ch
- 10-bit successive approximation type AD converter
  - Analog input: 8 ch

P-LQFP44-1010-0.80A



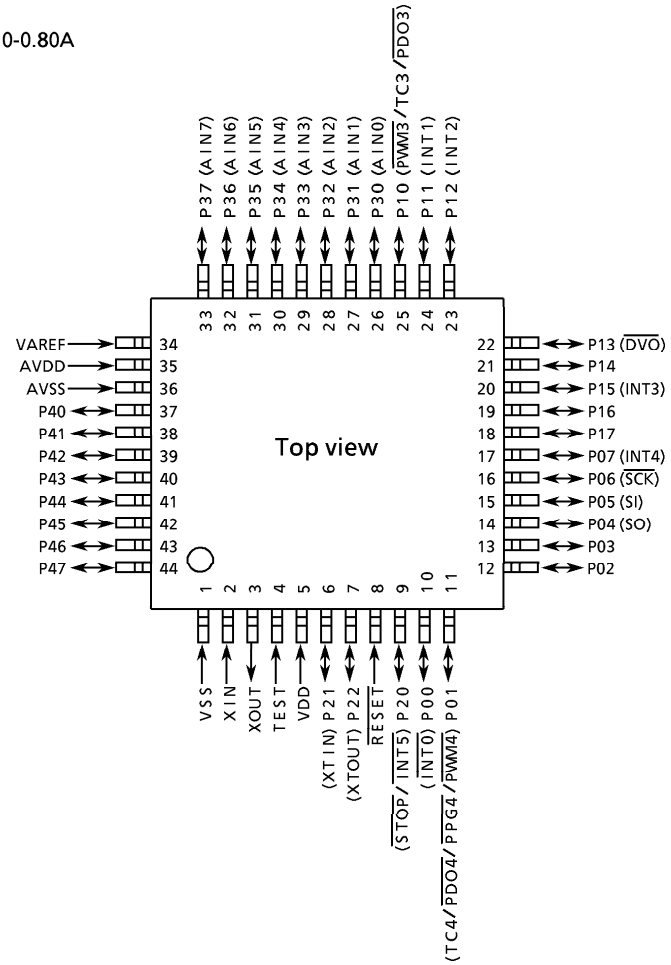
TMP86C845U

Note: There are some difference between TMP86C845U and TMP86PM47U.
Please refer to these data sheet about them.

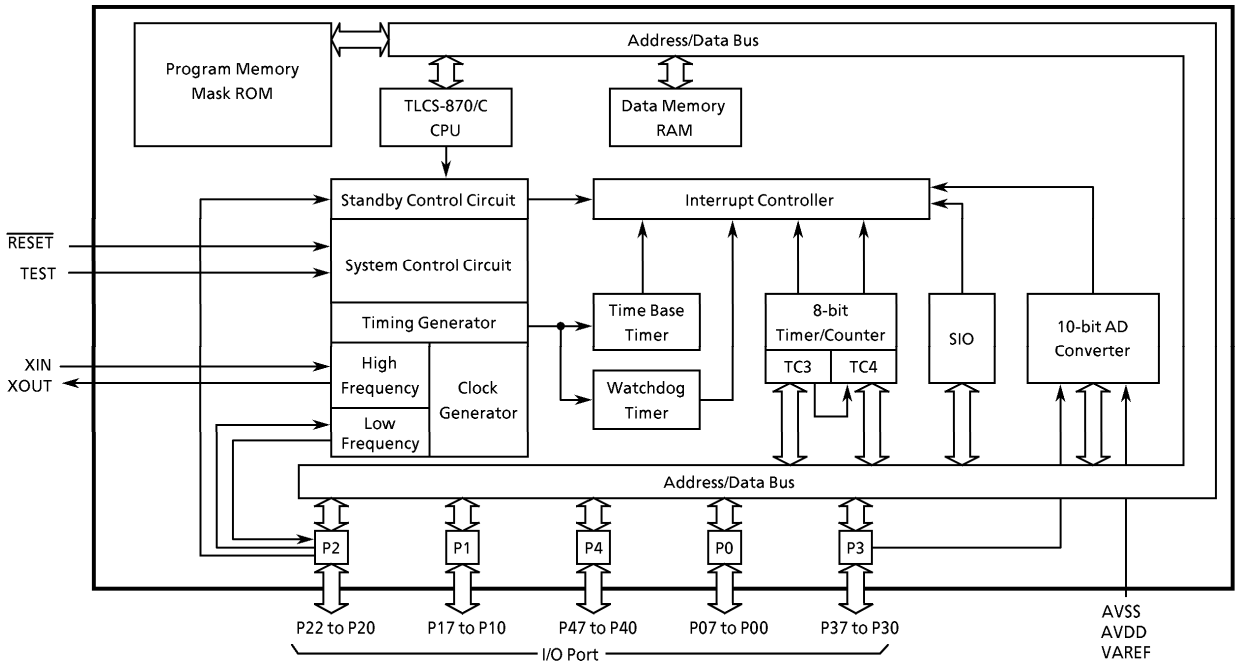
- Dual clock operation
  - Single/Dual-clock mode
- Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
  - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock. (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by INTTBT interruput.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interruputs.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interruputs.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by INTTBT interruput.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interruputs.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interruputs.
- Wide operating voltage: 2.7 to 5.5 V at 8 MHz/32.768 kHz

Pin Assignments (Top View)

P-LQFP44-1010-0.80A



Block Diagram



Pin Functions

Pin Name	I/O	Functions	
P07 (INT4)	I/O (Input)	8-bit I/O port. When used as input port, external interrupt input, serial clock input/output, serial data input/output and timer/counter 4 input/output, the latch must be set to "1".	External interrupt input
P06 ($\overline{SCK}$)	I/O (Input/Output)		SIO input/output
P05 (SI)	I/O (Input)		
P04 (SO)	I/O (Output)		
P03	I/O		
P02	I/O		
P01 ($\overline{PWM4}$/TC4/$\overline{PDO4}$/$\overline{PPG4}$)	I/O (Input/Output)		Timer/Counter input PPG output, PWM output, PDO output
P00 ($\overline{INT0}$)	I/O (Input)		External interrupt input
P17	I/O	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control. An output latch is set to "1" when using it as a functional terminal.	—
P16	I/O		
P15 (INT3)	I/O (Input)		External interrupt input
P14 ($\overline{PPG}$)	I/O (Output)		PPG output
P13 ($\overline{DVO}$)	I/O (Output)		Divider output
P12 (INT2/TC1)	I/O (Input)		External interrupt input
P11 (INT1)	I/O (Input)		External interrupt input.
P10 ($\overline{PWM3}$/TC3/$\overline{PDO3}$)	I/O (Input/Output)		Timer/Counter input PWM output, PDO output
P20 ($\overline{INT5}$/$\overline{STOP1}$)	I/O (Input)	3-bit I/O port with latch. When used as input port, external interrupt input, and STOP mode release signal input, the latch must be set to"1".	External interrupt input STOP mode release signal input
P21 (XTIN)	I/O (Input)		Resonator connecting pins for low-frequency clock. For inputting external clock, XTIN is used and XTOUT is opened.
P22 (XTOUT)	I/O (Output)		
P37 (AIN7)	I/O (Input)	8-bit I/O port. Each bit of these ports can be individually configured as an input or output under software control. When used as analog input, then must be set to "1".	AD converter analog inputs
P36 (AIN6)			
P35 (AIN5)			
P34 (AIN4)			
P33 (AIN3)			
P32 (AIN2)			
P31 (AIN1)			
P30 (AIN0)			
P47	I/O	8-bit I/O port with latch. Each bit of these ports can be individually configured as an input or an output under software control.	—
P46			
P45			
P44			
P43			
P42			
P41			
P40			
TEST	Input	Test pin for out-going test. Be fixed to Low.	
$\overline{RESET}$	Input	Reset signal input	
XIN	Input	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
VSS	Power Supply	0.0 [V] (GND)	
VDD		+ 5 V	
AVSS		0.0 [V] (GND)	
AVDD		AD circuit power supply	
VAREF		Analog reference voltage inputs (High, Low)	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C845 memory consist of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C845 memory address map. The general-purpose registers are not assigned to the RAM address space.

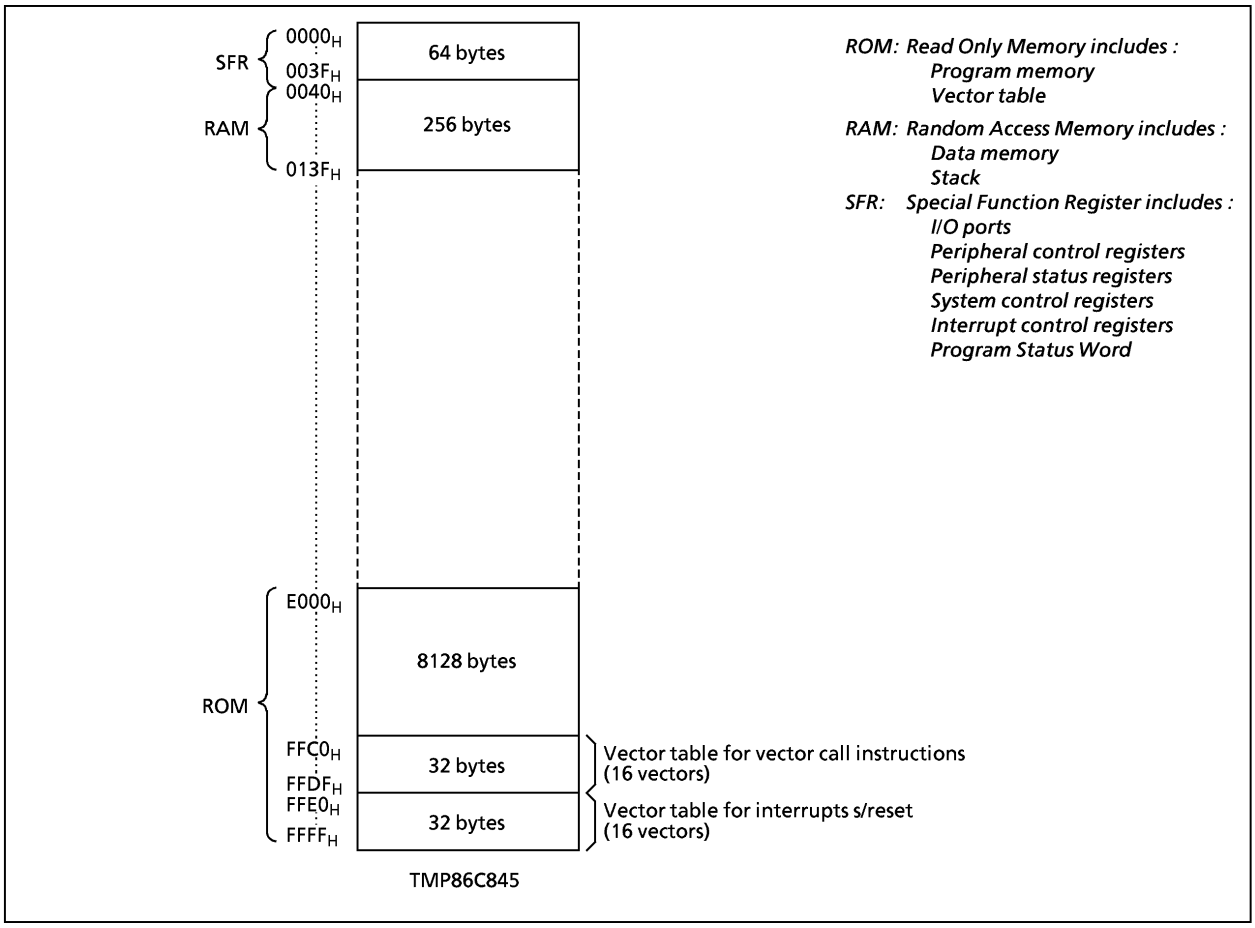


Figure 1-1. Memory Address Maps

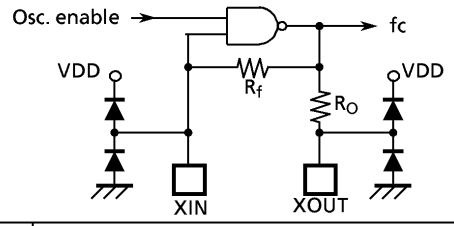
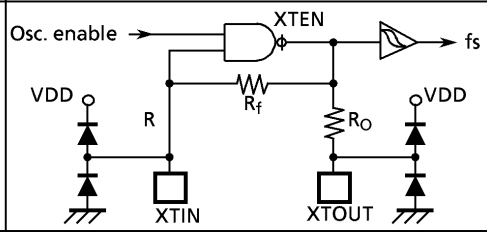
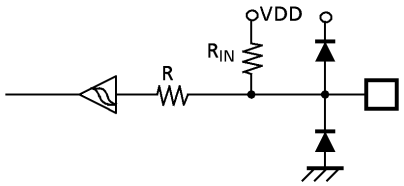
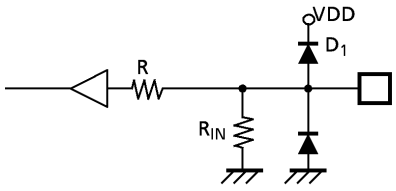
1.2 Program Memory (ROM)

The TMP86C845 has a 8 K×8 bits (Address $E000_H$ to $FFFF_H$), of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Input/Output Circuitry

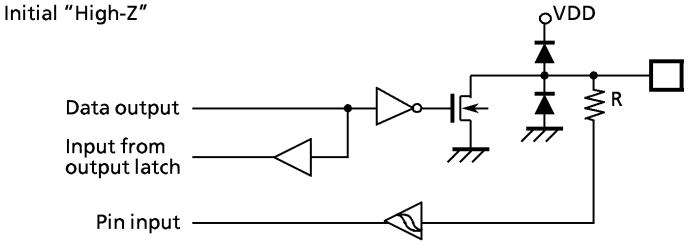
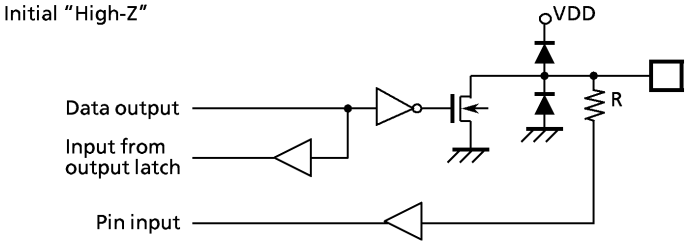
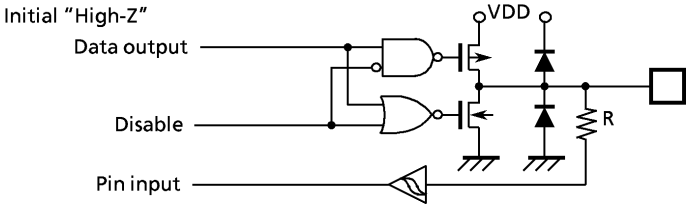
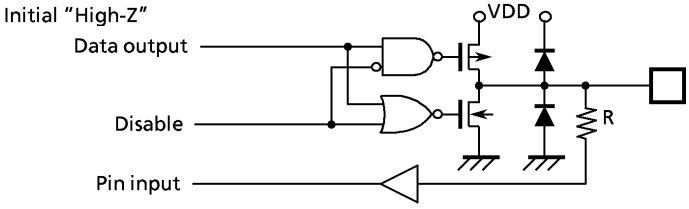
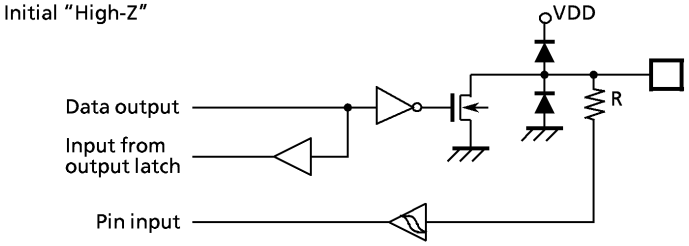
(1) Control Pins

The input/output circuitries of the TMP86C847/H47/M47 control pins are shown below.

Control Pin	I/O	Input/Output Circuitry	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency) R_f = 1.2 MΩ (typ.) R_O = 1.5 kΩ (typ.)
XTIN XTOUT	Input Output	NM1: Refer to port P2 NM2: 	Resonator connecting pins (Low-frequency) R_f = 6 MΩ (typ.) R_O = 220 kΩ (typ.)
$\overline{\text{RESET}}$	Input Output		Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 100 Ω (typ.)
TEST	Input		Pull-down resistor R_{IN} = 70 kΩ (typ.) R = 100 Ω (typ.)

Note 1: The TEST pin of the TMP86PM47 does not have a pull-down resistor and protect diode (D1). Fix the TEST pin at low-level.
Note 2: The input circuitry of $\overline{\text{RESET}}$ pin of TMP86C845 is diffeernt from TMP86PM47's one.

(2) Input/Output Ports

Port	I/O	Input/Output Circuitry	Remarks
P07 to P05 P00	I/O	Initial "High-Z" 	Sink open drain output High current output Hysteresis input R = 100 Ω (typ.)
P04 to P01	I/O	Initial "High-Z" 	Sink open drain output High current output R = 100 Ω (typ.)
P15 P12 to P10	I/O	Initial "High-Z" 	Tri-state I/O Hysteresis input R = 100 Ω (typ.)
P17, P16 P14, P13	I/O	Initial "High-Z" 	Tri-state I/O R = 100 Ω (typ.)
P2	I/O	Initial "High-Z" 	Sink open drain output High current output Hysteresis input R = 100 Ω (typ.)

Note: In TMP87PM47, P04 to P01, P17, 16, P14 and P13 are hysteresis input.

Port	I/O	Input/Output Circuitry	Remarks
P3	I/O	Initial "High-Z" Data output Disable Pin input VDD R	Tri-state I/O R = 100 Ω (typ.)
P4	I/O	Initial "High-Z" Data output Disable Pin input VDD R	Tri-state I/O High current output (Nch) R = 100 Ω (typ.)

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1} I_{OH}	P1, P3, P4 port	– 1.8	
	I_{OUT2} I_{OL}	P1, P3 port	3.2	mA
	I_{OUT3} I_{OL}	P0, P2, P4 port	30	
Output Current (Total)	ΣI_{OUT1}	P1, P3 port	60	
	ΣI_{OUT2}	P0, P2, P4 port	80	
Power Dissipation [T_{opr} = 85°C]	PD		250	mW
Soldering Temperature (Time)	Tsld		260 (10 sec)	°C
Storage Temperature	Tstg		– 55 to 125	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values, which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	2.7	5.5	V
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		V_{DD} × 0.70	V_{DD}	
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		$V_{DD} < 4.5$ V		V_{DD} × 0.90		
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V		0	V_{DD} × 0.30	
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}		$V_{DD} < 4.5$ V			V_{DD} × 0.10	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note : The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN1}	TEST Pull-Down		–	70	–	kΩ
	R_{IN2}	$\overline{RESET}$ Pull-Up		100	200	450	
Output Leakage Current	I_{LO1}	Sink Open Drain	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	
Output High Voltage	V_{OH}	Tri-state Port	V_{DD} = 4.5 V, V_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Current	V_{OL}	Except XOUT, XTOUT, P0, P4, P2 Port	V_{DD} = 4.5 V, V_{OL} = 1.6 mA	–	–	0.4	mA
	I_{OL}	High Current Port (P0, P2, P4 Port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	
Supply Current in NORMAL1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V fc = 8 MHz fs = 32.768 kHz	–	4.0	6.2	
Supply Current in IDLE0, 1, 2 mode				–	2.8	4.5	
Supply Current in SLOW1 mode			V_{DD} = 3.0 V V_{IN} = 2.8/0.2 V fs = 32.768 kHz	–	6	18	μA
Supply Current in SLEEP1 mode				–	4	15	
Supply Current in SLEEP0 mode				–	4	13	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V	–	0.5	10	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V

Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

AD Conversion Characteristics

(V_{SS} = 0.0 V, 4.5 V to 5.5 V , Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			
Analog Reference Voltage Range	$\triangle V_{AREF}$		3.5	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 5.5 V V_{SS} = AVSS = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = A_{VDD} = 5.0 V, V_{SS} = AVSS = 0.0 V V_{AREF} = 5.0 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.7 V to 4.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			
Analog Reference Voltage Range	$\triangle V_{AREF}$		2.5	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 4.5 V V_{SS} = AVSS = 0.0 V	–	0.5	0.8	mA
Non linearity Error		V_{DD} = A_{VDD} = 2.7 V, V_{SS} = AVSS = 0.0 V V_{AREF} = 2.7 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.8.2 Register Configuration".
Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} - V_{SS}$

AC Characteristics

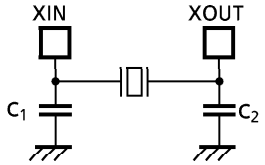
(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL1, 2 mode	0.5	–	4	μs
		IDLE0, 1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP0, 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twsH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low Level Clock Pulse Width	twsL					

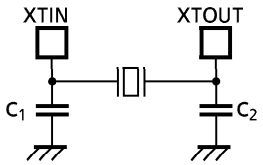
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html