CMOS 8-Bit Microcontroller TMP86FM48U/F

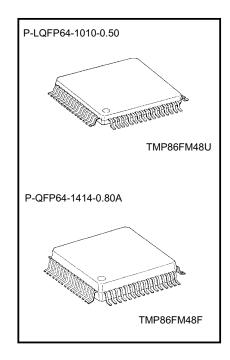
The TMP86FM48 is the high-speed, high-performance and low power consumption 8-bit microcomputer, including FLASH, RAM, multi-function timer/counter, serial interface (UART, HSIO, I2C), a 10-bit AD converter and two clock generators on chip.

	Product No.	FLASH (Program Area)	FLASH (Data Area)	RAM	Package	Emulation Chip
I	TMP86FM48U	32256 × 8 bits 512 × 8 bi		2.0 K × 8 bits	P-LQFP64-1010-0.50	*TMP86C948XB
I	TMP86FM48F	32230 × 6 DIIS	512 × 6 DIIS	2.0 K × 6 DILS	P-QFP64-1414-0.80A	*TIVIPOOC940AD

*: Under development

Feautures

- ♦ 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
 122 μs (at 32.768 kHz)
- ♦ 132 types and 731 basic instructions
- ♦ 20 interrupt sources (External: 5, Internal: 15)
- ♦ Input/Output ports (54 pins)
- ♦ 16-bit timer counter: 2 ch
 - Timer, Event counter,
 Pulse width measurement, External trigger timer,
 Window, PPG output modes
- ♦ 8-bit timer counter: 2 ch
 - Timer, Event counter, PWM output, Programmable divider output, Capture modes
- ♦ Time Base Timer
- ♦ Divider output function



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 damage to property.

damage to property.

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86FM48-1 2003-04-08

- Watchdog Timer
 - Interrupt source/internal reset generate (programmable)
- Serial interface
 - UART: 1ch (The function port for UART is also used as SIO function.)
 - SIO: 2ch
 - I2C bus: 1ch
- ♦ 10-bit successive approximation type AD converter
 - Analog input: 16 ch
- Four Key-On Wake-Up pins
- ♦ Dual clock operation
 - Single/Dual-clock mode
- Nine power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up.

Port output hold/High-impedance.

- SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
- IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of

Time-Base-Timer. Release by falling edge of TBTCR <TBTCK> setting.

• IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock.

Release by interruputs.

• IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock.

Release by interruputs.

• SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of

Time-Base-Timer. Release by falling edge of TBTCR <TBTCK> setting.

• SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock.

Release by interrupts.

• SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock.

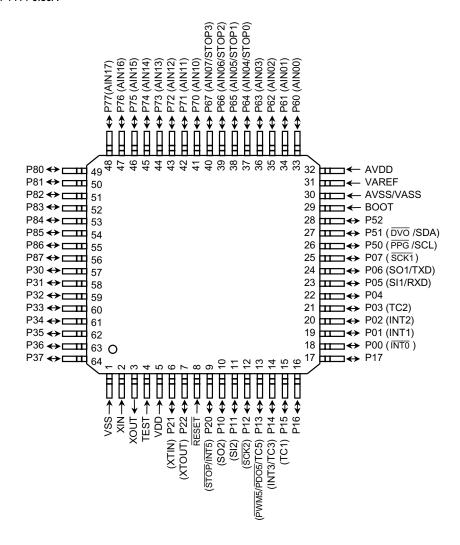
Release by interrupts.

♦ Wide operating voltage: 1.8 to 3.6 V at 8 MHz/32.768 kHz

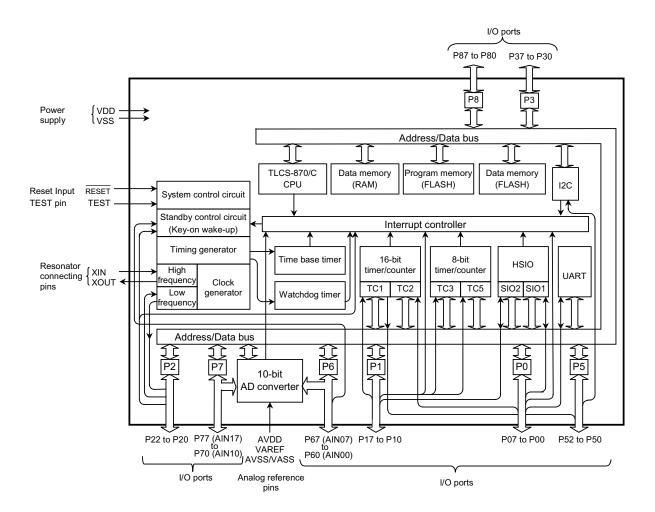
 $2.7\ \text{to}\ 3.6\ \text{V}$ at $16\ \text{MHz}/32.768\ \text{kHz}$

Pin Assignments (Top View)

P-LQFP64-1010-0.50 P-QFP64-1414-0.80A



Block Diagram



Pin Functions (1/2)

Pin Name	Input/Output	Fund	ctions		
P07 (SCK1)	I/O (I/O)	8-bit input/output port with latch.	Serial clock input/output 1		
P06 (TXD, SO1)	I/O (Output)	When used as a serial interface output	UART data output, Serial data output 1		
P05 (RXD, SI1)	I/O (Input)	or UART output, respective output latch (P0DR) should be set to "1".	UART data input, Serial data input 1		
P04	I/O	When used as an input port, an serial			
P03 (TC2)	I/O (Input)	interface input, UART input, timer	Timer counter 2 input		
P02 (INT2)	I/O (Input)	counter input or an external interrupt input, respective output control	External interrupt 2 input		
P01 (INT1)	I/O (Input)	(P00UTCR) should be cleared to "0"	External interrupt 1 input		
P00 (INT0)	I/O (Input)	after setting P0DR to "1".	External interrupt 0 input		
P17	I/O	8-bit input/output port with latch.			
P16	I/O	When used as a timer/counter output or serial interface output, respective			
P15 (TC1)	I/O (Input)	output latch (P1DR) should be set to	Timer counter 1 input		
P14 (TC3,INT3)	I/O (Input)	"1". When used as an input port, a timer counter input, an external interrupt input	Timer counter 3 input, External interrupt 3 input		
P13	1/0 (1/0)	or serial interface input, respective	PWM5 output, PDO5 output,		
(PWM5 , PDO5 , TC5)	I/O (I/O)	output control (P10UTCR) should be cleared to "0" after setting P1DR to "1".	Timer/counter 5 input		
P12 (SCK2)	I/O (I/O)	ologiod to a ditor octang i ibit to i i	Serial clock input/output 2		
P11 (SI2)	I/O (Input)		Serial data input 2		
P10 (SO2)	I/O (Output)		Serial data output 2		
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port or an	Resonator connecting pins (32.768 kHz For inputting external clock, XTIN is use		
P21 (XTIN)	I/O (Input)	external interrupt input, respective output control (P2OUTCR) should be	and XTOUT is opened.		
P20 (INT5, STOP)	I/O (Input)	cleared to "0" after setting output latch (P2DR) to "1".	External interrupt input 5 or STOP mode release signal input		
P37 to P30	I/O	8-bit input/output port with latch (Nch high current output). When used as an input port, respective output control (P3OUTCR) should be cleared to "0" after setting output latch (P3DR) to "1".			
P52	I/O	3-bit input/output port with latch (Nch high current output). When used as an input port or I2C-bus interface			
P51 (DVO , SDA)	I/O (Output,I/O)	input/output, respective output control (P5OUTCR) should be cleared to "0" after setting output latch (P5DR) to "1".	Divider Output/I ² C bus serial data input/output		
P50 (PPG, SCL)	I/O (Output,I/O)	When used as a PPG output or divider output, respective P5DR should be set to "1".	PPG Output/I ² C bus serial clock input/output		
P67 (AIN07, STOP3)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of this port can be	STOP 3 input		
P66 (AIN06, STOP2)	I/O (Input)	individually configured as an input or an output under software control. When	STOP 2 input		
P65 (AIN05, STOP1)	I/O (Input)	used as an input port, respective	STOP 1 input		
P64 (AIN04, STOP0)	I/O (Input)	input/output control (P6CR1) should be cleared to "0" after setting input control	STOP 0 input AD converter		
P63 (AIN03)	I/O (Input)	(P6CR2) to "1". When used as an analog input or key on wake up input,	analog inputs		
`/		2 h : : : : : : : : : : : : : : : : : :	i (
P62 (AIN02)	I/O (Input)	respective P6CR1 should be cleared to			
, ,	I/O (Input) I/O (Input)	respective P6CR1 should be cleared to "0" after clearing P6CR2 to "0". When used as a key on wake up input, STOPCR <stopien> should be set to</stopien>			

Pin Functions (2/2)

Pin Name	Input/Output	Functions	Pin Name		
P77 (AIN17)	I/O (Input)	8-bit programmable input/output port			
P76 (AIN16)	I/O (Input)	(tri-state). Each bit of this port can be individually configured as an input or an			
P75 (AIN15)	I/O (Input)	output under software control. When			
P74 (AIN14)	I/O (Input)	used as an input port, respective input/output control (P7CR1) should be cleared to "0" after setting input control	AD converter analog inputs		
P73 (AIN13)	I/O (Input)		AD converter analog inputs		
P72 (AIN12)	I/O (Input)	(P7CR2) to "1". When used as an analog input, respective P7CR1 should be			
P71 (AIN11)	I/O (Input)	cleared to "0" after clearing P7CR2 to			
P70 (AIN10)	I/O (Input)	"0".			
P87 to P80	I/O	8-bit input/output port with latch (Nch high current output). When used as an input port, respective output control (P8OUTCR) should be cleared to "0" after setting output latch (P8DR) to "1".			
XIN, XOUT	Input Output	Resonator connecting pins for high-freque For inputting external clock, XIN is used at	•		
RESET	Input	Reset signal input			
TEST	Input	Test pin for out-going test. Be fixed to low.			
воот	Input	Serial prom mode control input. When wribe fixed to High level.	ting to FLASH memory, BOOT pin should		
VDD, VSS		Power supply for operation			
VAREF	Power Supply	Analog reference voltage for AD conversion	on		
AVDD	Fower Supply	AD circuit power supply			
AVSS/VASS		AD circuit power supply/Analog reference GND for AD conversion			

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86FM48 memory consists of 5 blocks: FLASH memory, BOOT ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1.1.1 shows the TMP86FM48 memory address map. The general purpose registers are not assigned to the RAM address space.

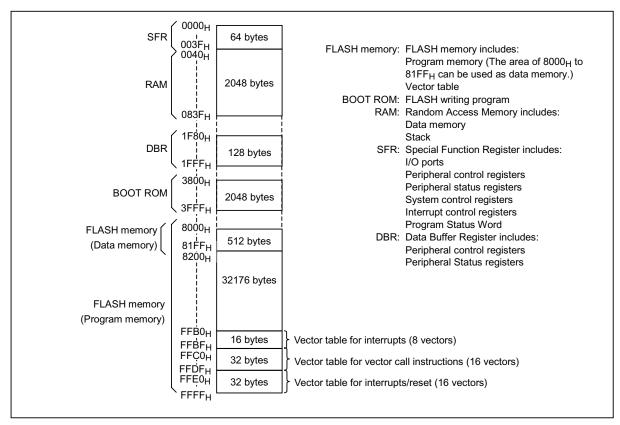


Figure 1.1.1 Memory Address Maps

1.2 Program Memory (FLASH)

The TMP86FM48 has a $32~\mathrm{K} \times 8$ bits (address $8000\mathrm{H}$ to FFFFH) of program memory (FLASH). The area of $8000\mathrm{H}$ to $81\mathrm{FFH}$ can be used as a 512×8 bits data memory of FLASH. However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See $2.4.5~\mathrm{Address}$ Trap). For details of FLASH memory, refer to section "2.16 FLASH memory".

Electrical Characteristics

Absolute Maximum Ratings $| (V_{SS} = 0 V) |$

Parameter	Symbol	Pins	Rating	Unit
Supply voltage	V_{DD}		-0.3 to 4.0	
Input voltage	V _{IN}		-0.3 to $V_{DD} + 0.3$	V
Output voltage	V _{OUT1}		-0.3 to $V_{DD} + 0.3$	
	I _{OUT1}	P0, P1, P20, P3, P5, P6, P7, P8 Ports	-2	
Output current (Per 1 pin)	I _{OUT2}	P0, P1, P2, P4, P6, P7, P8, Ports	2	
	I _{OUT3}	P3, P5 Ports	10	
	Σl _{OUT1}	P0, P1, P20, P3, P5, P6, P7, P8 Ports	-80	mA
Output current (Total)	ΣI_{OUT2}	P0, P1, P2, P4, P6, P7, P8, Ports	80	
	Σl _{OUT3}	P3, P5 Ports	30	
Power dissipation [Topr = 85°C]	PD		350	mW
Soldering temperature (time)	Tsld		260 (10 s)	
Storage temperature	Tstg		-55 to 125	°C
Operating temperature	Topr		-40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition-1 (MCU mode) (V_{SS} = 0 V, Topr = -40 to 85°C)

Parameter	Symbol	Pins	Co	ondition	Min	Max	Unit
			fc = 16 MHz	NORMAL1, 2 mode IDLE0, 1, 2 mode	2.7		
0 1 11	.,		fc = 8 MHz	NORMAL1, 2 mode	1.8	0.0	
Supply voltage	V_{DD}		fs =	IDLE0, 1, 2 mode SLOW1, 2 mode		3.6	
			32.768 kHz	SLEEP0, 1, 2 mode	1.8		
				STOP mode	•		V
	V _{IH1}	Except Hysteresis input	$V_{DD} \ge 2.7 \text{ V}$ $V_{DD} < 2.7 \text{ V}$		$V_{DD}\times 0.70$	V _{DD}	
Input high level	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V _{IH3}				$V_{DD} \times 0.90$		
	V _{IL1}	Except Hysteresis input	V _{DD} ≥ 2.7 V			$V_{DD} \times 0.30$	
Input low level	V _{IL2}	Hysteresis input	VDD ≥ 2.7 V		0	$V_{DD} \times 0.25$.]
	V _{IL3}		V_{DD} < 2.7 V			$V_{DD} \times 0.10$	
Clock frequency	fc	XIN, XOUT	$V_{DD} = 1.8 \text{ to } 3$.6 V	1.0	8.0	MHz
	10	λίιν, λου ί	V _{DD} = 2.7 to 3.6 V		1.0	16.0	IVII IZ
	fs	XTIN, XTOUT	$V_{DD} = 1.8 \text{ to } 3$.6 V	30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Recommended Operating Condition-2 (Serial PROM mode) $(V_{SS} = 0 \text{ V}, \text{Topr} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	VDD		2 MHz ≤ fc ≤16 MHz	2.7	3.6	٧
Clock frequency	fc	XIN, XOUT	VDD = 2.7 to 3.6 V	2.0	16.0	MHz

Note: The operating temperature area of serial PROM mode is 25° C \pm 5° C and the operating area of high frequency of serial PROM mode is different from MCU mode.

DC Characteristics $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol		Pir	าร	Cond	Condition		Тур.	Max	Unit
Hysteresis voltage	V _{HS}	Hyste	eresis inp	out	$V_{DD} = 3.3 \text{ V}$		-	0.4	-	V
	I _{IN1}	TEST	-		$V_{DD}=3.6\;V,\;V_{IN}$	= 0 V	-	_	-5	
Input current	I _{IN2}	Sink	Open Dr	ain, Tri-state	$V_{DD} = 3.6 \text{ V}, V_{IN}$	= 3.6 V/0 V	-	-	±5	μΑ
	I _{IN3}	RESE	RESET		$V_{DD} = 3.6 \text{ V}, V_{IN}$	= 3.6 V	_	_	+5	
	R _{IN1}	TEST	Pull-do	wn	$V_{DD} = 3.6 \text{ V}, V_{IN}$		_	70	_	
Input resistance	R _{IN2}	BOO	T Pull-do	own	$V_{DD} = 3.6 \text{ V}, V_{IN}$	= 3.6 V	-	70	_	kΩ
input resistance	R _{IN3}		RESET Pull-Up		$V_{DD} = 3.6 \text{ V}, V_{IN}$		100	220	450	K52
High frequency feedback resister	R _{FB}	XOU	Γ		$V_{DD} = 3.6 \text{ V}$		-	1.2	_	MΩ
Low frequency feedback resister	R _{FBT}	XTOL	JT		V _{DD} = 3.6 V		-	14	-	IVIS 2
Output leakage current	I _{LO}	Sink	Sink Open Drain Tri-state I		$V_{DD} = 3.6 \text{ V}$ $V_{OUT} = 3.4 \text{V} / 0.2 \text{ V}$		-	-	±10	μΑ
Output high voltage	V _{OH}	C-MC	C-MOS, Tri-state		$V_{DD} = 3.6 \text{ V}, I_{OH}$	= -0.6 mA	3.2	_	_	
Output low voltage	V _{OL}	Exce _l Ports		, P3 and P5	$V_{DD} = 3.6 \text{ V}, I_{OL}$	= 0.9 mA	-	-	0.4	V
Output low current	l _{OL}	P3, P	5 Ports		V _{DD} = 3.6 V, V _{OL} = 1.0 V		-	6	-	mA
				Flash Area		MNP = "1"	_	T.B.D.	T.B.D.	
Supply current in NORMAL 1, 2 mode			Fetch area	DAM A	$V_{DD} = 3.6 \text{ V}$	MNP = "0"	-	T.B.D.	T.B.D.	
NORWAL 1, 2 mode				RAM Area	V _{IN} = 3.4 V/0.2 V fc = 16 MHz	MNP = "1"	-	T.B.D.	T.B.D.	mA
Supply current in					fs = 32.768 kHz	MNP•ATP = "1"	_	T.B.D.	T.B.D.	
IDLE 0, 1, 2 mode					10 - 02.7 00 Ki iz	MNP•ATP = "0"	-	T.B.D.	T.B.D.	
0			F - 4 - 1-	Flash Area		MNP = "1"	-	T.B.D.	T.B.D.	
Supply current in SLOW 1 mode			Fetch area	DAM A ****		MNP = "0"	-	T.B.D.	T.B.D.	
SLOW Tillode	I _{DD}			RAM Area	$V_{DD} = 3.6 \text{ V}$	MNP = "1"	_	T.B.D.	T.B.D.	
Supply current in					$V_{IN} = 3.4 \ V/0.2 \ V$	MNP•ATP = "1"	-	T.B.D.	T.B.D.	
SLEEP 1 mode			1		$fs=32.768\;kHz$	MNP•ATP = "0"	-	T.B.D.	T.B.D.	μА
Supply current in					MNP•ATP = "1"	-	T.B.D.	T.B.D.		
SLEEP 0 mode						MNP•ATP = "0"	-	T.B.D.	T.B.D.	
Supply current in STOP mode					$V_{DD} = 3.6 \text{ V}$ $V_{IN} = 3.4 \text{ V}/0.2 \text{ V}$		-	T.B.D.	T.B.D.	

- Note 1: Typical values show those at Topr = 25° C.
- Note 2: Input current (I_{IN1} , I_{IN2}): The current through pull-up or pull-down resistor is not included.
- Note 3: I_{DD} does not include I_{REF} current.
- Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE 0, 1, 2.
- Note 5: MNP(MNPWDW) shows bit0 in EEPCR register and ATP(ATPWDW) shows bit1 in EEPCR register.
- Note 6: "Fetch" means reading operation of FLASH data as an instruction by CPU.

AD Conversion Characteristics

(VSS = 0.0 V, 2.7 V \leq VDD \leq 3.6 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog reference voltage	VAREF		A _{VDD} – 1.0	_	A _{VDD}	
Power supply voltage of analog control circuit	A _{VDD}			V_{DD}		V
Analog reference voltage range (Note 4)	ΔVAREF		2.5	-	-	V
Analog input voltage	V _{AIN}		V _{SS}	_	V _{AREF}	
Power supply current of analog reference voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 3.6 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	_	T.B.D.	T.B.D.	mA
Non linearity error		V _{DD} = A _{VDD} = 2.7 V	_	ı	±2	
Zero point error		155	_	ı	±2	LSB
Full scale error		$V_{SS} = 0.0 \text{ V}$	_	- 1	±2	LOB
Total error		$V_{AREF} = 2.7 V$	-	_	±2	•

$$(V_{SS} = 0.0 \text{ V}, 2.0 \text{ V} \le V_{DD} < 2.7 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog reference voltage	V _{AREF}		A _{VDD} - 0.6	-	A _{VDD}	
Power supply voltage of analog control circuit	A _{VDD}			V_{DD}		V
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.0	-	-	V
Analog input voltage	V _{AIN}		V _{SS}	_	V _{AREF}	
Power supply current of analog reference voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 2.0V$ $V_{SS} = 0.0 V$	_	T.B.D.	T.B.D.	mA
Non linearity error		V _{DD} = A _{VDD} = 2.0 V	_	-	±4	
Zero point error		35 155	_	ı	±4	LSB
Full scale error		$V_{SS} = 0.0 \text{ V}$	_	- 1	±4	LOD
Total error		V _{AREF} = 2.0 V	_	ı	±4	

$(V_{SS} = 0.0 \ V, \ 1.8 \ V \leq V_{DD} < 2.0 \ V, \ Topr = -10 \ to \ 85^{\circ}C) \ (Note \ 5)$

	-					
Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog reference voltage	V _{AREF}		A _{VDD} – 0.1	-	A _{VDD}	
Power supply voltage of analog control circuit	A _{VDD}			V_{DD}		V
Analog reference voltage range (Note 4)	ΔV_{AREF}		1.8	-	-	V
Analog input voltage	V _{AIN}		Vss	-	VAREF	
Power supply current of analog reference voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 1.8 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	T.B.D.	T.B.D.	mA
non linearity error		V _{DD} = A _{VDD} = 1.8 V	_	-	±4	
Zero point error		35 155	_	-	±4	LSB
Full scale error		V _{SS} = 0.0 V	_	-	±4	LOB
Total error		V _{AREF} = 1.8 V	_	-	±4	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.15.2 Register configration".
- Note 3: Please use input voltage to AIN input Pin in limit of VAREF VSS.

 When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range: ΔVAREF = VAREF VSS
- Note 5: When AD is used with VDD < 2.0 V, the guaranteed temperature range varies with the operating voltage.
- Note 6: When AD converter is not used, fix the AVDD pin and VAREFpin on the V_{DD} level.

AC Characteristics $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 3.6 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Mashina and time	4	NORMAL1, 2 mode IDLE1, 2 mode	0.25	- 4		
Machine cycle time	tcy	SLOW1, 2 mode SLEEP1, 2 mode	117.6	-	133.3	μS
High Level clock pulse width Low level clock pulse width	twcH twcL	For external clock operation (XIN input), fc = 16 MHz	-	31.25	-	ns
High level clock pulse width Low level clock pulse width	twcH twcL	For external clock operation (XTIN input), fs = 32.768 kHz	_	15.26	_	μs

$$(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 3.6 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL1, 2 mode	0.5	_	4	
Machine cycle time	tcy	IDLE1, 2 mode	0.0		·	
Machine Cycle time	icy	SLOW1, 2 mode	117.6		400.0	μS
		SLEEP1, 2 mode	117.0	ı	133.3	
High level clock pulse width	twcH	For external clock operation (XIN		60.5		
Low level clock pulse width	twcL	input), fc = 8 MHz	- 62.5	02.5	_	ns
High level clock pulse width twcH		For external clock operation (XTIN	45.00	45.00	-	
Low level clock pulse width	twcL	input), fs = 32.768 kHz	- 15.26	μS		

Flash Characteristics (V_{SS} = 0 V)

Parameter	Condition	Min	Тур.	Max	Unit
Number of guaranteed writes (page writing) to Flash memory in serial PROM mode	$_{\text{DD}} = 2.7 \text{ to } 3.6 \text{ V}, 2 \text{ MHz} \le \text{fc} \le 16 \text{ MHz}$ $_{\text{copr}} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C})$	T.B.D	Times		
Number of guaranteed writes (page writing) to Flash data memory in MCU mode	V_{DD} = 1.8 to 3.6 V at fc = 8 MHz V_{DD} = 2.7 to 3.6 V at fc = 16 MHz (Topr = -40 to 85°C)	1	1	T.B.D	Times
Writing time to Flash data memory for one page (64 bytes) in MCU mode		ı	T.B.D	ı	ms

Recommended Oscillating Conditions

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following http://www.murata.co.jp/search/index.html