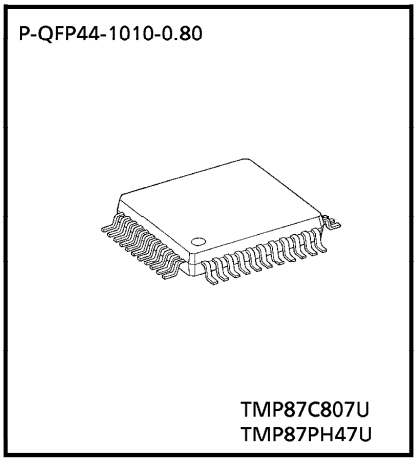
CMOS 8-Bit Microcontroller

TMP87C807U

87C807 is high speed and high performance 8-bit single chip microcomputers with small package. The MCU contain CPU core, ROM, RAM, input/output ports, six multi-function timer/counters, a serial interface, a high speed serial output, and two clock generators on a chip.
87C807 is compatibled with 87PH47 except for ROM size, RAM size and A/D converter.

Part No.	ROM	RAM	Package	OTP MCU
TMP87C807U	8 K × 8-bit	256 × 8-bit	P-QFP44-1010-0.80	TMP87PH47U

Features

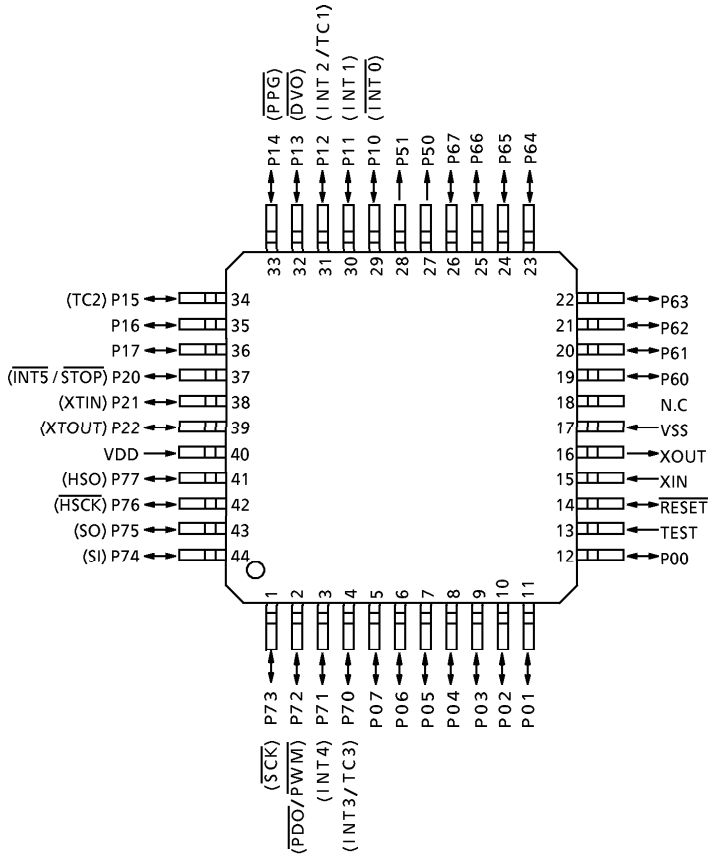


- ◆8-bit single chip microcomputer TLCS-870 Series
- ◆Instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
- ◆412 basic instructions
  - Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
  - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
  - 16-bit data operations
  - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆14 interrupt sources (External: 6, Internal: 8)
  - All sources have independent latches each, and nested interrupt control is available.
  - 4 edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆Input/Output ports (37 pins)
  - High current output: 8 pins (typ. 20 mA)
  - Output: 2 pins
- ◆Two 16-bit Timer/Counters
  - Timer, Event counter, Programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes
- ◆Two 8-bit Timer/Counters
  - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
- ◆Divider output function (frequency: 1 kHz to 8 kHz)
- ◆Watchdog Timer
- ◆8-bit Serial Interface
  - With 8 bytes transmit/receive data buffer
  - Internal/external serial clock, and 4/8-bit mode
- ◆8-bit High Speed Serial Output (rate: max. 1 bit/μs)
- ◆Dual clock operation
- ◆Five Power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
  - SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
  - IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE2 mode: CPU stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ◆Wide operating voltage: 2.7 to 5.5 V at 4.2 MHz/32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz
- ◆Emulation Pod: BM87CH47U0A

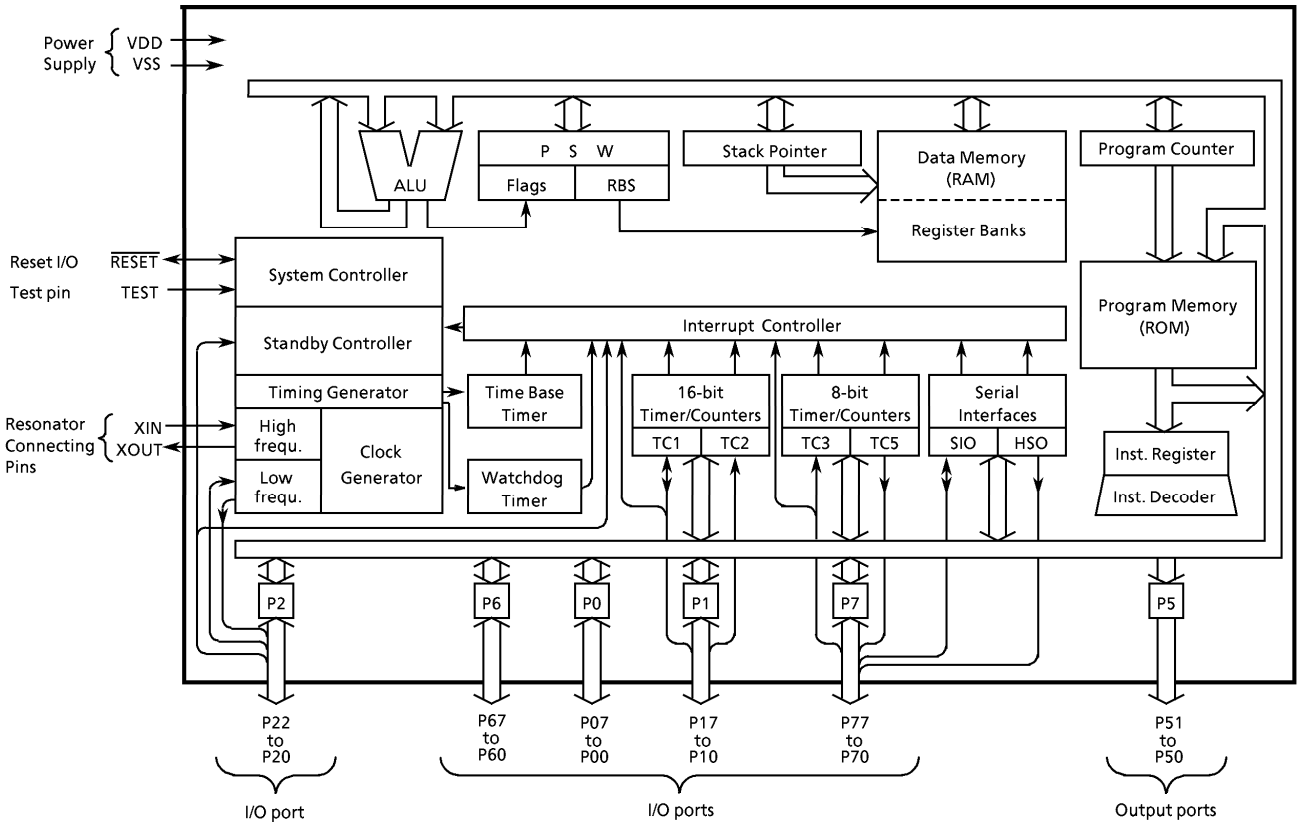
980910EBP2

Pin Assignments (Top View)

P-QFP44-1010-0.80



Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output or a PPG output, the latch must be set to "1".	
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer/Counter 2 input
P14 ($\overline{\text{PPG}}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{\text{DVO}}$)			Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{\text{INT0}}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{\text{INT5}}$ / $\overline{\text{STOP}}$)			External interrupt input 5 or STOP mode release signal input
P51, P50	Output	2-bit output port with latch	
P67 to P60	I/O (Output)	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control.	
P77 (HSO)	I/O (Output)	8-bit programable input/output port (tri-state). When used as an input port, a SIO input/output, an external interrupt input or a $\overline{\text{PWM}}$/$\overline{\text{PDO}}$ output, the latch must be set to "1".	HSO serial data output
P76 ($\overline{\text{HSCK}}$)			HSO serial clock output
P75 (SO)			SIO serial data output
P74 (SI)			SIO serial data input
P73 ($\overline{\text{SCK}}$)	I/O (I/O)		SIO serial clock input/output
P72 ($\overline{\text{PWM}}$ / $\overline{\text{PDO}}$)	I/O (Output)		8-bit PWM output or 8-bit programmable divider output
P71 (INT4)	I/O (Input)		External interrupt input 4
P70 (INT3 / TC3)			External interrupt input 3 or Timer/Counter 3 input
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be fixed at low level.	
VDD, VSS	Power Supply	2.7 to 5.5 V, 0V (GND)	
N.C		Be fixed at low level.	

Operational Description

1. CPU Core FUnctions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87C807. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

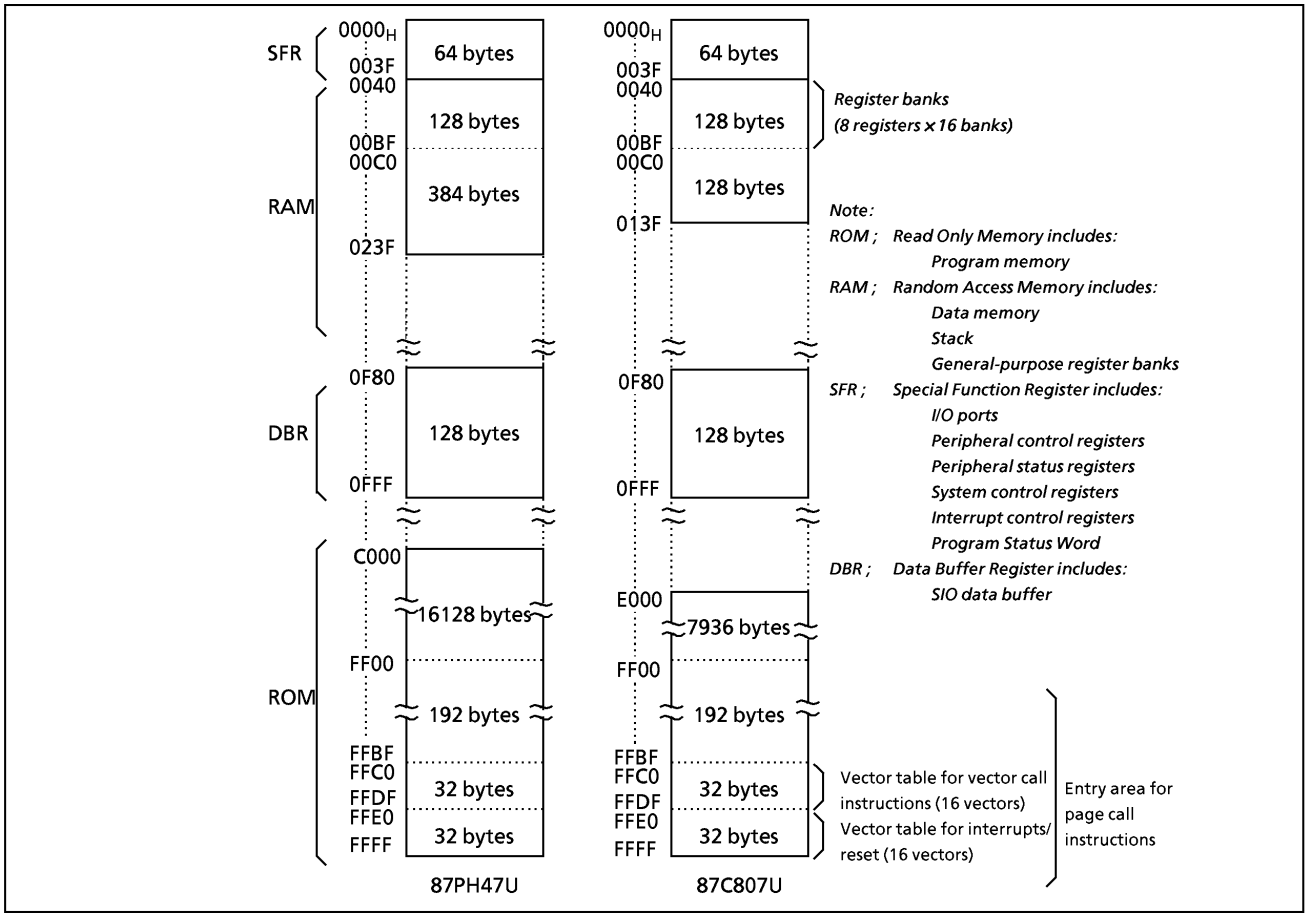


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2, P5, P6, P7	3.2	mA
	I_{OUT2}	Port P0	30	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2, P5, P6, P7	100	mA
	ΣI_{OUT2}	Port P0	120	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL 1/2 mode and IDLE 1/2 mode.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P0	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low current	I_{OL3}	P0	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V/0.2 V	–	6	9	mA
Supply Current in IDLE 1, 2 modes				–	3	4.5	
Supply Current in NORMAL 1, 2 modes			V_{DD} = 3.0 V fc = 4.19 MHz fs = 32.768 kHz V_{IN} = 2.8 V/0.2 V	–	2	3	mA
Supply Current in IDLE 1, 2 modes				–	1	1.5	
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V/0.2 V	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}, I_{IN3}; The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

A.C. Characteristics - 1

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	4	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

A.C. Characteristics - 2

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

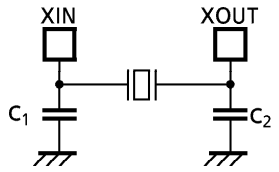
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 mode	0.95	–	10	μs
		In IDLE1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 4.2 MHz	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

Recommended Oscillating Conditions - 1 (V_{SS} = 0 V, T_{opr} = – 30 to 70°C)

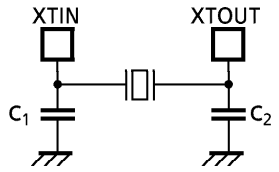
Parameter	Oscillator	Frequency	Recommended Oscillator		Recommended Condition	
					C_1	C_2
High-frequency	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ CSACS8.00MT CSTCS8.00MT	30 pF	30 pF
		4.19 MHz	MURATA	CSA4.19MGU CST4.19MGWU	built-in 30 pF	built-in 30 pF
	Crystal Oscillator	8 MHz	NDK	AT-51	16 pF	16 pF
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	12 pF	12 pF

Recommended Oscillating Conditions-2 (V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillator Frequency	Recommended Oscillator		Recommended Constant	
					C_1	C_2
High-frequency	Ceramic Resonator	4.19 MHz	MURATA	CSA4.19 MGU	30 pF	30 pF
			MURATA	CST4.19MGWU	built-in 30 pF	built-in 30 pF
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fiedstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.