CMOS 8-Bit Microcontroller

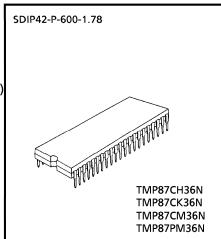
TMP87CH36N, TMP87CK36N, TMP87CM36N

The 87CH36/CK36/CM36 is high speed and high performance 8-bit single chip microcomputer. This MCU contains CPU core, ROM, RAM, input/output ports, six multi-function timer/counter, serial bus interface, on-screen display, PWM, 6-bit A/D conversion inputs and remote control signal preprocessor on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CH36N	16 Kbytes			
TMP87CK36N	24 Kbytes	1 Kbytes	SDIP42-P-600-1.78	TMP87PM36N
TMP87CM36N	32 Kbytes			

Features

- ◆8-bit single chip microcomputer TLCS-870 Series
- lacktriangle Instruction execution time : 0.5 μ s (at 8 MHz)
- ◆412 basic instructions
 - Multiplication and Division (8 bits × 8 bits, 16 bits ÷ 8 bits)
 - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive Or)
 - 16-bit data operations
 - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆12 interrupt sources (External: 3, Internal: 9)
 - All sources have independent latches each, and nested interrupt control is available.
 - Edge-selectable external interrupts with noise reject
 - High-speed task switching by register bank changeover
- ♦6 Input/Output ports (34 pins)
 - High current output: 4 pins (typ. 20 mA)
- ◆Two 16-bit Timers
- **◆**Two 8-bit Timer/Counters
 - Timer, Event counter, Capture (Pulse width/duty measurement) modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16384 Hz)
- ◆Watchdog Timer
 - Interrupt source/reset output (programmable)
- ◆Serial bus Interface
 - I²C-bus, 8-bit SIO modes



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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.
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◆On-screen display circuit

Character patterns
 Characters displayed
 128 characters
 24 columns x 12 lines

• Composition : 14 x 18 dots

• Size of character : 3 kinds (line by line)

• Color of character : 8 kinds (character by character)

• Variable display position : Horizontal 128 steps, Vertical 256 steps

• Fringing, Smoothing function

◆D/A conversion (Pulse Width Modulation) outputs

• 14-bit resolution (1 channel)

• 7-bit resolution (9 channels)

◆6-bit A/D conversion input (4 channels)

◆ Pulse output (Clock for PLL IC)

◆ Remote control signal preprocessor

◆Two Power saving operating modes

• STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.

• IDLE mode : CPU stops, and Peripherals operate. Release by interrupts.

◆Operating voltage: 4.5 to 5.5 V at 8 MHz

◆Emulation Pod : BM87CM37N0A

Pin Assignments (Top View) (PWM0) P40 ← 42 <u></u>VDD SDIP42-P-600-1.78 (PWM1) P41 < 2 41 □ → P36 (SCK) (PWM2) P42 < 3 40 □< →P35 (SDA/SO) (PWM3) P43 ≪ 4 →P34 (SCL / SI) 39 5 (PWM4) P44 ← →[38 P33 (TC4) (PWM5) P45 < →[6]< →P32 (INT4) 37 □< >P31 (TC3) (PWM6) P46 < → 7 36 (PWM7) P47 **← →**[8 35 □ ← → P30 (INT3 / RXIN) (PWM8) P50 ← 9 34 □ < > P20 (INT5 / STOP) (PWM9) P51 < → 10 33 □< →RESET (PULSE) P52 **← →** → XOUT 11 32 P53 < 12 31 ∐≺—XIN (CIN0) P54 < →[13 30 **□**←─TEST (CIN1) P55 < →[29 →OSC2 14 (CIN2) P56 < →[15 28 □<—osc1 (CIN3) P57 < → 16 27]< →P71 (VD) | ← →P70 (HD) P60 **≺** 17 26 P61 < → [] | < →P67 (Y / BL) 18 25 □< >P66 (B) P62 < → [] 19 24 I/O Ports |≺ →P65 (G) P63 < →[20 23 P71 to P70 →P64 (R) P67 VSS-21 22 **Block Diagram** to P60 Display Character Y/BL ROM Memory B,G,R VD HD Р6 Р7 Osc. connecting pins for ∫osc1 On-screen display circuit on-screen ે osc2 display VDD Stack Pointer **Program Counter** Data Memory Supply \ VSS (RAM) Flags RBS Register Banks Reset I/O RESET System Controller Test Pin TEST Interrupt Controller Program Memory (ROM) Standby Controller 16-bit Time Base 8-bit **Timing Generator** Timer Timer/Counter Timer TC1 TC2 TC3 TC4 XIN: Resonator Connecting \XOUT High Clock Watchdog Inst.Register frequ. Generator Timer Pins Inst. Decoder Serial Bus D/A Converter 6-bit A/D Pulse Remote control P2 Р4 P5 Р3 Interface-ver.A Converter Generator signal preprocessor (SIO/I2C) P57 to P50 P20 P47 P36

I/O Ports

Pin Function

Pin Name	Input/Output	Function					
P20 (INT5/STOP)	I/O (Input)	1-bit input / output port with latch. When used as an input port, the latch must be set to "1".	External interrupt input 5 or STOP mode release signal input				
P36 (SCK)	I/O (I/O)		SIO serial clock input/output				
P35 (SDA/SO)	I/O (I/O/Output)	7-bit input/output port with latch.	l ² Cbus serial data input/output or SIO serial data output				
P34 (SCL/SI)	I/O (I/O/Input)	When used as an input port, a serial bus interface input/output, a timer/counter	I ² Cbus serial clock input/output or SIO serial data input				
P33 (TC4)		input, a remote control signal preprocessor input, or an external	Timer/Counter 4 input				
P32 (INT4)	I/O (Input)	interrupt input, the latch must be set to	External interrupt input 4				
P31 (TC3)]"1".	Timer/Counter 3 input				
P30 (INT3/RXIN)	I/O (Input/Input)		External interrupt input 3 or remote control signal preprocessor input				
P47 (PWM7) to P41 (PWM1)	140 (0	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an activity of the configured as an input or an activity of the configured as an input or an activity of the configuration.	7-bit D/A conversion (PWM) outputs				
P40 (PWM0)	1/O (Output)	output under software control. During reset, all bits are configured as inputs. When used as a PWM output, the latch must be set to "1".					
P57 (CIN3) to P54 (CIN0)	I/O (Input)	8-bit input/output port with latch.	6-bit A/D conversion (Comparator) inputs				
P53	I/O	When used as an input port, a					
P52 (PULSE)		comparator input, a PWM output, or a pulse output, the latch must be set to	Pulse output (Clock for PLL IC)				
P51 (PWM9)	I/O (Output)	"1".	7-bit D/A conversion (PWM) outputs				
P50 (PWM8)			/ Sit DIA conversion (1 vvivi) outputs				
P67 (Y/BL)		8-bit programmable input/output port (P67 to P64 : tri-state, P63 to P60 : High	Focus signal output or Background blanking control signal output				
P66 (B) P65 (G) P64 (R)	· I/O (Output)	current output). Each bit of this port can be individually configured as an input or an output under software control. During reset, all bits are configured as	RGB output				
P63 P62 P61 P60	. I/O	inputs. When used as the R, G, B, Y / BL outputs of on-screen display circuit, each bit of the P6 port data selection register (bits 7 to 4 in address 0F91 _H) must be set to "1".	High current output.				
P71 (VD)	I/O (Input)	2-bit input/output port with latch. When used as an input ports, or a vertical synchronous signal input and horizontal	Vertical synchronous signal input				
P70 (HD)		synchronous signal input, the latch must be set to "1".	Horizontal synchronous signal input				
OSC1, OSC2	Innut Output	Resonator connecting pins for on-screen di	splay circuitry.				
XIN, XOUT	Input, Output	Resonator connecting pins. For inputting e	external clock, XIN is used and XOUT is opened.				
RESET	I/O	Reset signal input or watchdog timer output output.	ut/address-trap- reset output/system-clock-reset				
TEST	Input	Test pin for out-going test. Be tied to low.					
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)					

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1 shows the memory address maps of the 87CH36/K36/M36. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR / DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

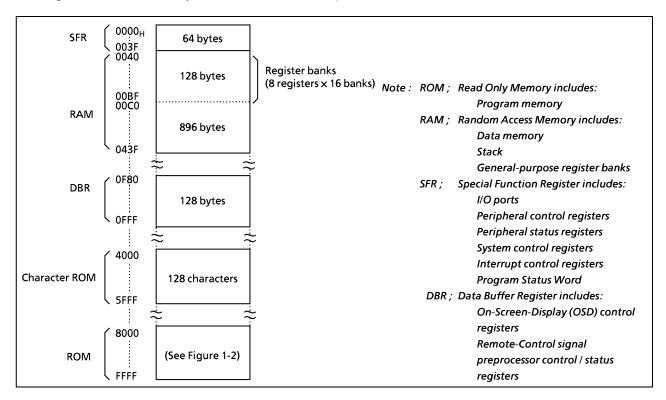


Figure 1-1. Memory Address Map

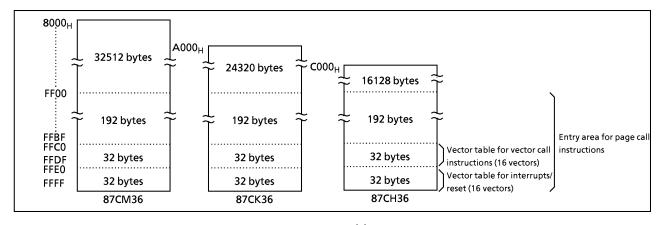


Figure 1-2. ROM Address Maps

Electrical Characteristics

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Ratings	Unit	
Supply Voltage	V _{DD}		- 0.3 to 6.5	V	
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	V	
Output Voltage	V _{OUT1}		- 0.3 to V _{DD} + 0.3	٧	
	I _{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	3.2		
Output Current (Per 1 pin)	I _{OUT2}	Ports P60 to P63	30	mA	
0 + +6 +/T + 1)	Σl _{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	120		
Output Current (Total)	Σl _{OUT2}	Ports P60 to P63	120	mA	
Power Dissipation [Topr = 70°C]	PD		600	mW	
Soldering Temperature (time)	Tsld		260 (10 s)	°C	
Storage Temperature	Tstg		– 55 to 125	°C	
Operating Temperature	Topr		– 30 to 70	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = -30 to 70°C)

Parameter	Symbol	Pins		Conditions		Max	Unit	
Supply Voltage	V _{DD}		fc = 8 MHz			5.5	V	
				STOP mode	2.0			
La casada Librala Marida a ca	V _{IH1}	Except hysteresis input		V _{DD} ≧ 4.5 V		V _{DD}	v	
Input High Voltage	V _{IH2}	Hysteresis input				V DD		
	V _{IL1}	Except hysteresis input		- V _{DD} ≥4.5 V		$V_{DD} \times 0.30$		
Input Low Voltage	V _{IL2}	Hysteresis input				$V_{DD} \times 0.25$	V	
	fc	XIN, XOUT	V _D	V _{DD} = 4.5 to 5.5 V		8.0		
Clock Frequency		0.01 0.03	Normal frequency mode (FORS = 0, V _{DD} = 4.5 to 5.5 V)		4.0	$f_{OSC} \le f_C \times 1$ $.2 \le 8.0$	MHz	
	losc	f _{OSC} OSC1, OSC2		Double frequency mode (FORS = 1, V_{DD} = 4.5 to 5.5 V)		$f_{OSC} \le f_C \times 0.6 \le 4.0$		

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock Frequency fc; The condition of supply voltage range is the value in NORMAL and IDLE modes.

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D.C. Characteristics

 $(V_{SS} = 0 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit	
Hysteresis Voltage	V _{HS}	Hysteresis inputs		-	0.9	_	٧	
	I _{IN1}	TEST	V _{DD} = 5.5 V, V _{IN} = 5.5 V / 0 V	_	_	± 2		
In most Commont	I _{IN2}	Open drain ports	V _{DD} = 5.5 V, V _{IN} = 5.5 V	-	_	2		
Input Current	I _{IN3}	Tri-state ports	V _{DD} = 5.5 V, V _{IN} = 5.5 V / 0 V	-	_	± 2	<u>μ</u> Α	
	I _{IN4}	RESET, STOP	V _{DD} = 5.5 V, V _{IN} = 5.5 V / 0 V	_	_	± 2		
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ	
Output Leakage Current	I _{LO1}	Sink open drain ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	-	_	2	_	
	I _{LO2}	Tri-state ports	$V_{DD} = 5.5 \text{ V}, \ V_{OUT} = 5.5 \text{ V} / 0 \text{ V}$	_	_	± 2	μΑ	
Output High Voltage	V _{OH2}	Tri- state port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	_	_	٧	
Output Low Voltage	V _{OL}	Except XOUT, OSC2 and ports P60 to P63	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	-	_	0.4	V	
Output Low Current	I _{OL3}	Ports P60 to P63	V _{DD} = 4.5 V, V _{OL} = 1.0 V	_	20	_	mA	
Supply Current in NORMAL mode			V _{DD} = 5.5 V fc = 8 MHz	_	10	16	mA	
Supply Current in IDLE mode	I _{DD}		$V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$	-	6	8	mA	
Supply Current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V / 0.2 V	_	0.5	10	μΑ	

Note 1 : Typical values show those at $T_{opr} = 25$ °C , $V_{DD} = 5$ V.

Note 2 : Input Current I_{IN1} , I_{IN4} ; The current through pull-up or pull-down resistor is not included.

Note 3: Typical current consumption during A/D conversion is 1.2 mA.

A/D Conversion Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Analog Input Voltage Range	V _{AIN}	CIN3 to CIN0		V _{SS}	-	V_{DD}	٧
Conversion Error			V _{DD} = 5.0 V	-	-	± 1.5	LSB

TMP87CH36/K36/M36

A.C. Characteristics

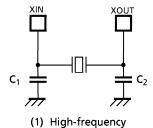
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$

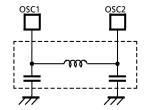
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Machine Cuele Time	tcy	In NORMAL mode	0.5	-	1.0	
Machine Cycle Time	tcy	In IDLE mode	0.3			μS
High-Level Clock Pulse Width	t _{WCH}	For external clock operation	62.5	_	_	
Low-Level Clock Pulse Width	t_{WCL}	(XIN input) , fc = 8MHz	02.3			ns

Recommended Oscillating Condition

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, T_{opr} = -30 \text{ to } 70^{\circ}\text{C})$$

Parameter	Oscillator	Frequency	Recommended	Recomm Condi	
Tarameter	Oscillator	rrequericy	Oscillator	C ₁	C ₂
	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	7g 08	30 pF
	Ceramic Nesonator	4 MHz	KYOCERA KBR4.0MS	30 pi	30 pi
High-frequency		4 101112	MURATA CSA4.00MG		
Oscillation	Crystal Oscillator	8 MHz	TOYOCOM 210B 8.0000	20. 5	20. 5
		4 MHz	TOYOCOM 204B 4.0000	20 pF	20 pF
OSD	LC Resonator	8 MHz	TOKO A285TNIS-11695		
		7 MHz	TOKO TBEKSES-30375FBY	_	_





(2) LC Resonator for OSD

Note: On our OSD circuit, the horizontal display start position is determined by counting the clock from LC oscillator. So, the unstable start of oscillation after the rising edge of Horizontal Sync. Signal will be cause the OSD distortion.

Generally, smaller C and larger L make clearer wave form at the beginning of oscillation. We recommend that the value of LC oscillator should be equal and bigger than $33 \mu H$.

Note: To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, by CRT (Cathode Ray Tube).