CMOS 8-Bit Microcontroller

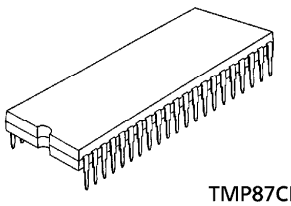
TMP87CH36N, TMP87CK36N, TMP87CM36N

The 87CH36/CK36/CM36 is high speed and high performance 8-bit single chip microcomputer. This MCU contains CPU core, ROM, RAM, input/output ports, six multi-function timer/counter, serial bus interface, on-screen display, PWM, 6-bit A/D conversion inputs and remote control signal preprocessor on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CH36N	16 Kbytes	1 Kbytes	SDIP42-P-600-1.78	TMP87PM36N
TMP87CK36N	24 Kbytes			
TMP87CM36N	32 Kbytes			

Features

SDIP42-P-600-1.78



TMP87CH36N
TMP87CK36N
TMP87CM36N
TMP87PM36N

- ◆8-bit single chip microcomputer TLCS-870 Series
- ◆Instruction execution time : 0.5 μs (at 8 MHz)
- ◆412 basic instructions
  - Multiplication and Division (8 bits × 8 bits, 16 bits ÷ 8 bits)
  - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive Or)
  - 16-bit data operations
  - 1-byte jump/subroutine-call (Short relative jump / Vector call)
- ◆12 interrupt sources (External : 3, Internal : 9)
  - All sources have independent latches each, and nested interrupt control is available.
  - Edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆6 Input/Output ports (34 pins)
  - High current output : 4 pins (typ. 20 mA)
- ◆Two 16-bit Timers
- ◆Two 8-bit Timer/Counters
  - Timer, Event counter, Capture (Pulse width/duty measurement) modes
- ◆Time Base Timer (Interrupt frequency : 1 Hz to 16384 Hz)
- ◆Watchdog Timer
  - Interrupt source/reset output (programmable)
- ◆Serial bus Interface
  - I2C-bus, 8-bit SIO modes

980910EBP1

◆On-screen display circuit
- Character patterns : 128 characters
- Characters displayed : 24 columns × 12 lines
- Composition : 14 × 18 dots
- Size of character : 3 kinds (line by line)
- Color of character : 8 kinds (character by character)
- Variable display position : Horizontal 128 steps, Vertical 256 steps
- Fringing, Smoothing function

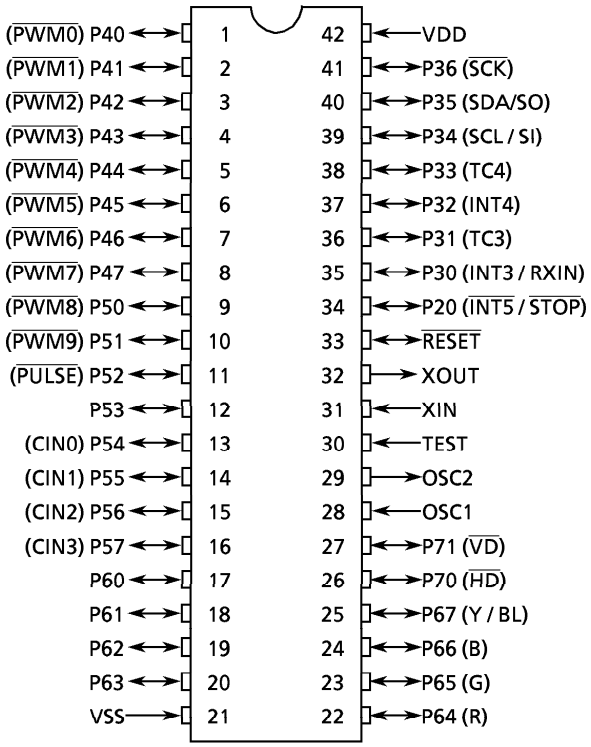
◆D/A conversion (Pulse Width Modulation) outputs
- 14-bit resolution (1 channel)
- 7-bit resolution (9 channels)

◆6-bit A/D conversion input (4 channels)
◆Pulse output (Clock for PLL IC)
◆Remote control signal preprocessor
◆Two Power saving operating modes
- STOP mode : Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
- IDLE mode : CPU stops, and Peripherals operate. Release by interrupts.

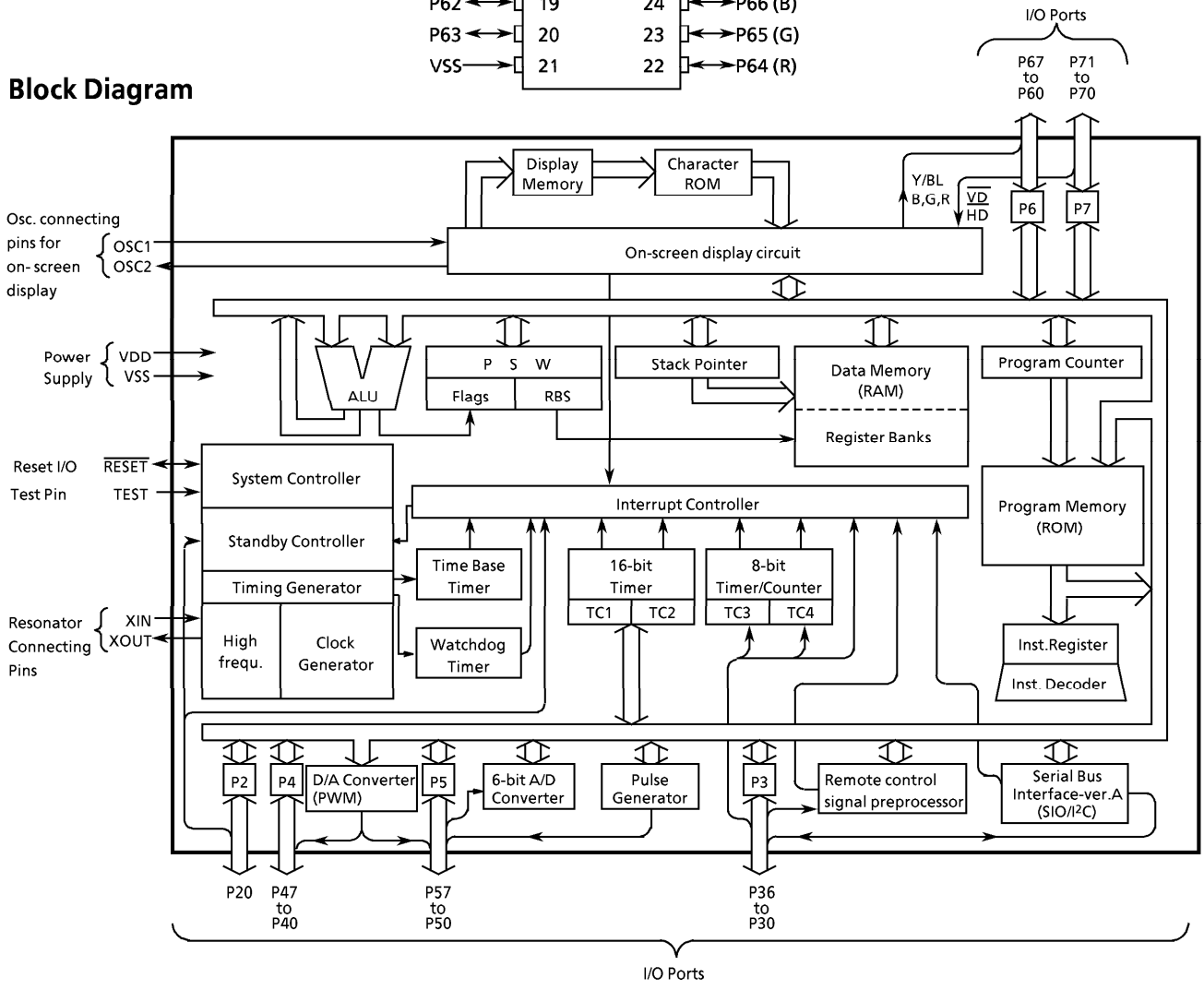
◆Operating voltage : 4.5 to 5.5 V at 8 MHz
◆Emulation Pod : BM87CM37N0A

Pin Assignments (Top View)

SDIP42-P-600-1.78



Block Diagram



Pin Function

Pin Name	Input/Output	Function	
P20 ($\overline{INT5}$/$\overline{STOP}$)	I/O (Input)	1-bit input / output port with latch. When used as an input port, the latch must be set to "1".	External interrupt input 5 or STOP mode release signal input
P36 ($\overline{SCK}$)	I/O (I/O)	7-bit input/output port with latch. When used as an input port, a serial bus interface input/output, a timer/counter input, a remote control signal preprocessor input, or an external interrupt input, the latch must be set to "1".	SIO serial clock input/output
P35 (SDA/SO)	I/O (I/O/Output)		I²Cbus serial data input/output or SIO serial data output
P34 (SCL/SI)	I/O (I/O/Input)		I²Cbus serial clock input/output or SIO serial data input
P33 (TC4)	I/O (Input)		Timer/Counter 4 input
P32 (INT4)			External interrupt input 4
P31 (TC3)			Timer/Counter 3 input
P30 (INT3/RXIN)	I/O (Input/Input)		External interrupt input 3 or remote control signal preprocessor input
P47 ($\overline{PWM7}$) to P41 ($\overline{PWM1}$)	I/O (Output)	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a PWM output, the latch must be set to "1".	7-bit D/A conversion (PWM) outputs
P40 ($\overline{PWM0}$)			14-bit D/A conversion (PWM) output
P57 (CIN3) to P54 (CIN0)	I/O (Input)	8-bit input/output port with latch. When used as an input port, a comparator input, a PWM output, or a pulse output, the latch must be set to "1".	6-bit A/D conversion (Comparator) inputs
P53	I/O		
P52 ($\overline{PULSE}$)	I/O (Output)		Pulse output (Clock for PLL IC)
P51 ($\overline{PWM9}$)			7-bit D/A conversion (PWM) outputs
P50 ($\overline{PWM8}$)			
P67 (Y/$\overline{BL}$)	I/O (Output)	8-bit programmable input/output port (P67 to P64 : tri-state, P63 to P60 : High current output). Each bit of this port can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as the R, G, B, Y / $\overline{BL}$ outputs of on-screen display circuit, each bit of the P6 port data selection register (bits 7 to 4 in address $0F91_H$) must be set to "1".	Focus signal output or Background blanking control signal output
P66 (B)			RGB output
P65 (G)			
P64 (R)			
P63	I/O		High current output.
P62			
P61			
P60			
P71 ($\overline{VD}$)	I/O (Input)	2-bit input/output port with latch. When used as an input ports, or a vertical synchronous signal input and horizontal synchronous signal input, the latch must be set to "1".	Vertical synchronous signal input
P70 ($\overline{HD}$)			Horizontal synchronous signal input
OSC1, OSC2	Input, Output	Resonator connecting pins for on-screen display circuitry.	
XIN, XOUT		Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap- reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1 shows the memory address maps of the 87CH36/K36/M36. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR / DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

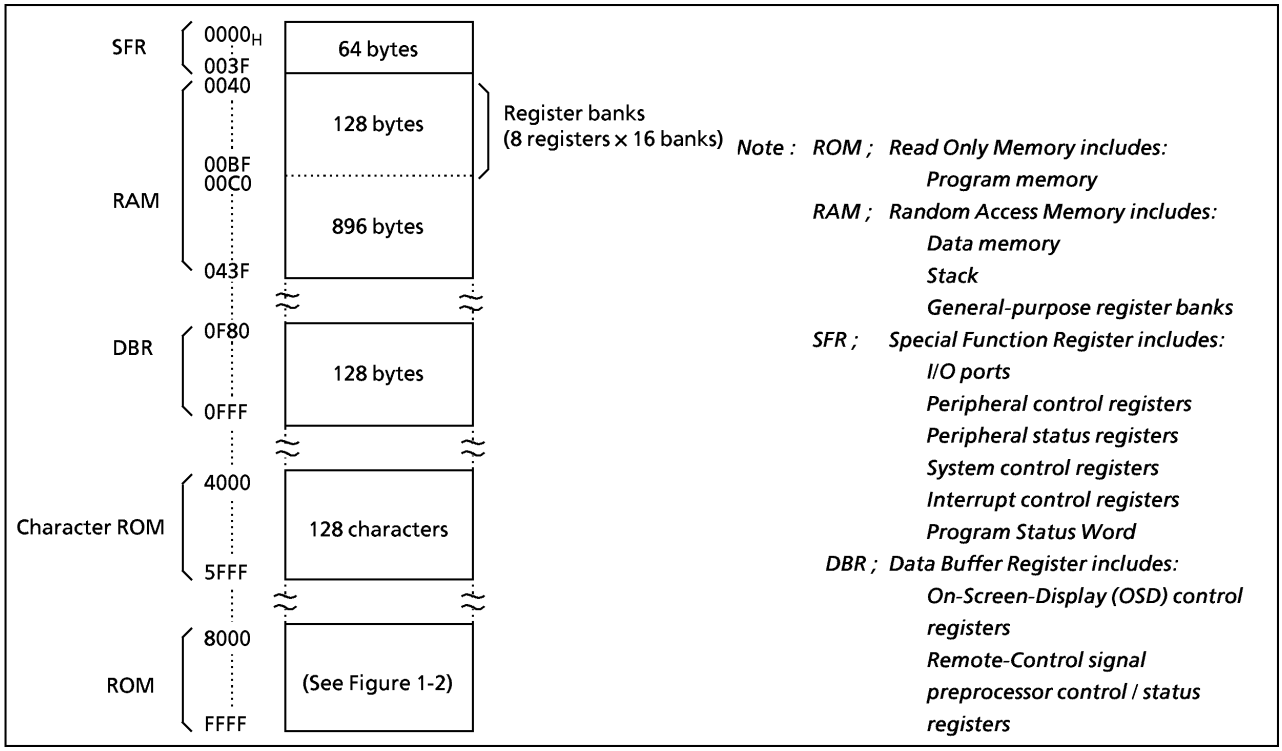


Figure 1-1. Memory Address Map

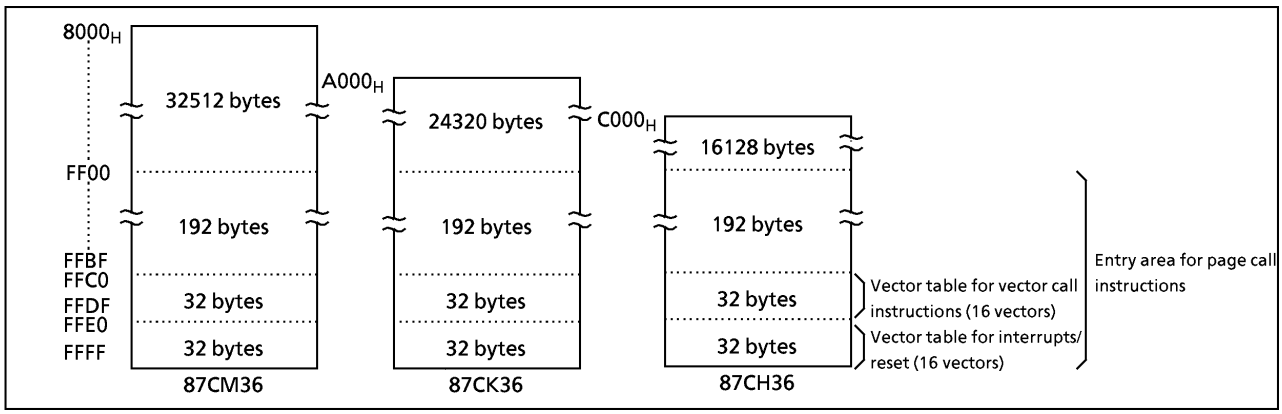


Figure 1-2. ROM Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	3.2	mA
	I_{OUT2}	Ports P60 to P63	30	
Output Current (Total)	ΣI_{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	120	mA
	ΣI_{OUT2}	Ports P60 to P63	120	
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL mode	4.5	5.5	V
				IDLE mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		4.0	8.0	MHz
	f_{OSC}	OSC1, OSC2	Normal frequency mode (FORS = 0, V_{DD} = 4.5 to 5.5 V)		4.0	$f_{OSC} \leqq f_C \times 1.2 \leqq 8.0$	
			Double frequency mode (FORS = 1, V_{DD} = 4.5 to 5.5 V)		2.0	$f_{OSC} \leqq f_C \times 0.6 \leqq 4.0$	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock Frequency fc ; The condition of supply voltage range is the value in NORMAL and IDLE modes.

D.C. Characteristics

(V_{SS} = 0 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports	V_{DD} = 5.5 V, V_{IN} = 5.5 V	–	–	2	
	I_{IN3}	Tri-state ports	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	–	–	± 2	
	I_{IN4}	$\overline{RESET}$, $\overline{STOP}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	–	–	± 2	
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri- state port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT, OSC2 and ports P60 to P63	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low Current	I_{OL3}	Ports P60 to P63	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL mode	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz V_{IN} = 5.3 V / 0.2 V	–	10	16	mA
Supply Current in IDLE mode				–	6	8	mA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1 : Typical values show those at T_{opr} = 25°C , V_{DD} = 5 V.
Note 2 : Input Current I_{IN1}, I_{IN4} ; The current through pull-up or pull-down resistor is not included.
Note 3 : Typical current consumption during A/D conversion is 1.2 mA.

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Analog Input Voltage Range	V_{AIN}	CIN3 to CIN0		V_{SS}	–	V_{DD}	V
Conversion Error			V_{DD} = 5.0 V	–	–	± 1.5	LSB

A.C. Characteristics

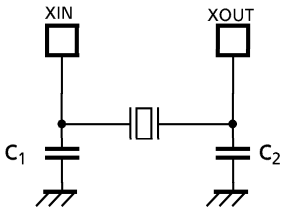
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL mode	0.5	–	1.0	μs
		In IDLE mode				
High-Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) , fc = 8MHz	62.5	–	–	ns
Low-Level Clock Pulse Width	t_{WCL}					

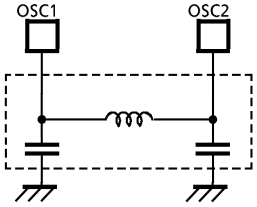
Recommended Oscillating Condition

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Oscillator	Frequency	Recommended Oscillator	Recommended Conditions	
				C_1	C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA KBR4.0MS		
			MURATA CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM 210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM 204B 4.0000		
OSD	LC Resonator	8 MHz	TOKO A285TNIS-11695	–	–
		7 MHz	TOKO TBEKSES-30375FBY		



(1) High-frequency



(2) LC Resonator for OSD

Note : On our OSD circuit, the horizontal display start position is determined by counting the clock from LC oscillator. So, the unstable start of oscillation after the rising edge of Horizontal Sync. Signal will be cause the OSD distortion.
Generally, smaller C and larger L make clearer wave form at the beginning of oscillation.
We recommend that the value of LC oscillator should be equal and bigger than 33μH.

Note : To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, by CRT (Cathode Ray Tube).