CMOS 8-Bit Microcomputer

TMP88C060F

The 88C060 is the high-speed and high-performance 8-bit microcomputer, including eight multiple timer / counters, a 10-bit A/D converter, serial interfaces (UART, I²C bus, and SIO). It can externally expand large program memory / data memory (up to 1 Mbytes linear address space).

Part No.	ROM	RAM	Package
TMP88C060F	ROM less	512 × 8 bit	P-LQFP80-1212-0.50A

Features

◆8-bit microcomputer TLCS-870 / X Series.

◆Minimum instruction execution time : 0.32 μs (at 12.5 MHz)
- Instruction execution time can be changed to reduce power consumption.
  min. 0.32 μs, 0.64 μs,1.28 μs, 2.56 μs, 5.12 μs, 122 μs at 12.5 MHz / 32.768 kHz

◆External memory expansion
- Expanded up to 1M bytes (for both programs and data)
- Non-multiplexed bus (20 bits of address and 8 bits of data)
- Wait control
- Bus arbitration control

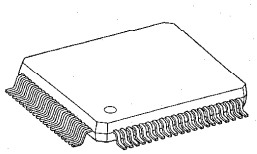
◆18 interrupt sources (External : 6, Internal : 12)

◆Input / Output ports (42 pins)
- High current output : 8 pins (typ. 20 mA), LED direct drive

◆Two 16-bit Timer / Counters
- TC1 : Timer, Event counter, Programmable pulse generator output, Pulse width measurement, External trigger timer, and Window modes.
- TC2 : Timer, Event counter, and Window modes.

◆Four 8-bit Timer / Counters
- TC3 : Timer, Event counter, and Capture for Remote control signal decoding (Pulse width / duty measurement) modes.
- TC4 : Timer, Event counter, PWM outputs, and programmable divider output modes.
- TC5 : Timer, PWM output, and programmable divider output modes
- TC6 : Timer and Baud-rate generation for UART modes

P-LQFP80-1212-0.50A



TMP88C060F

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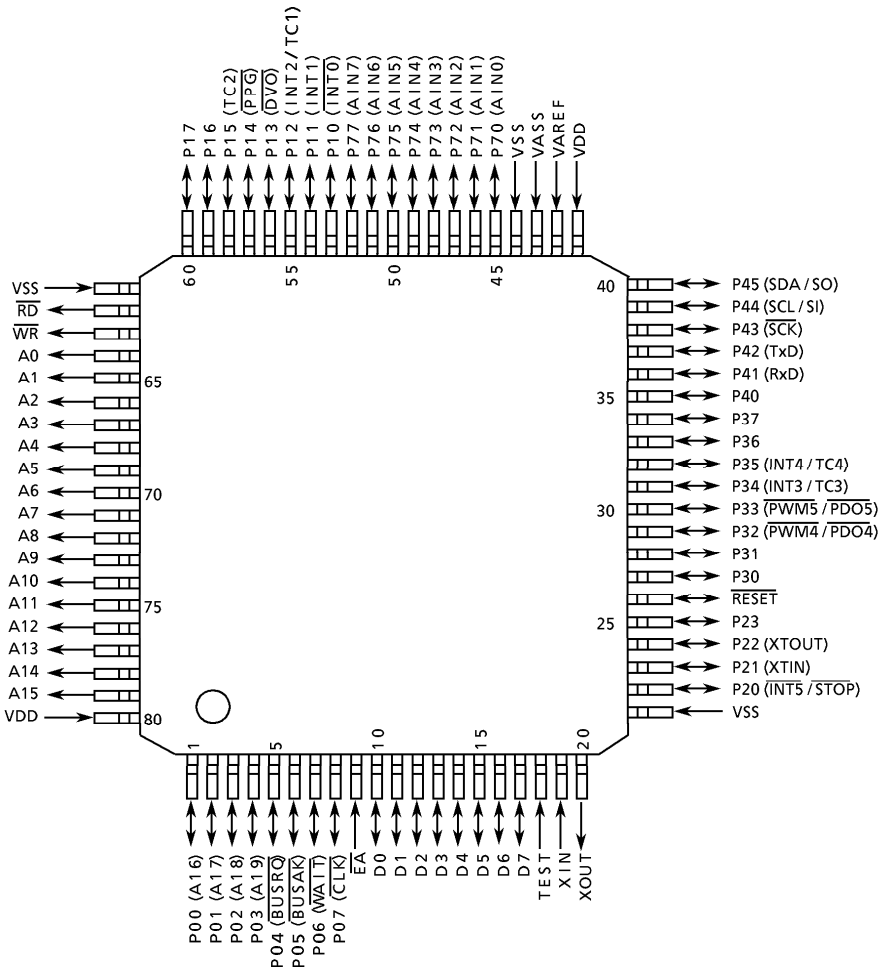
Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

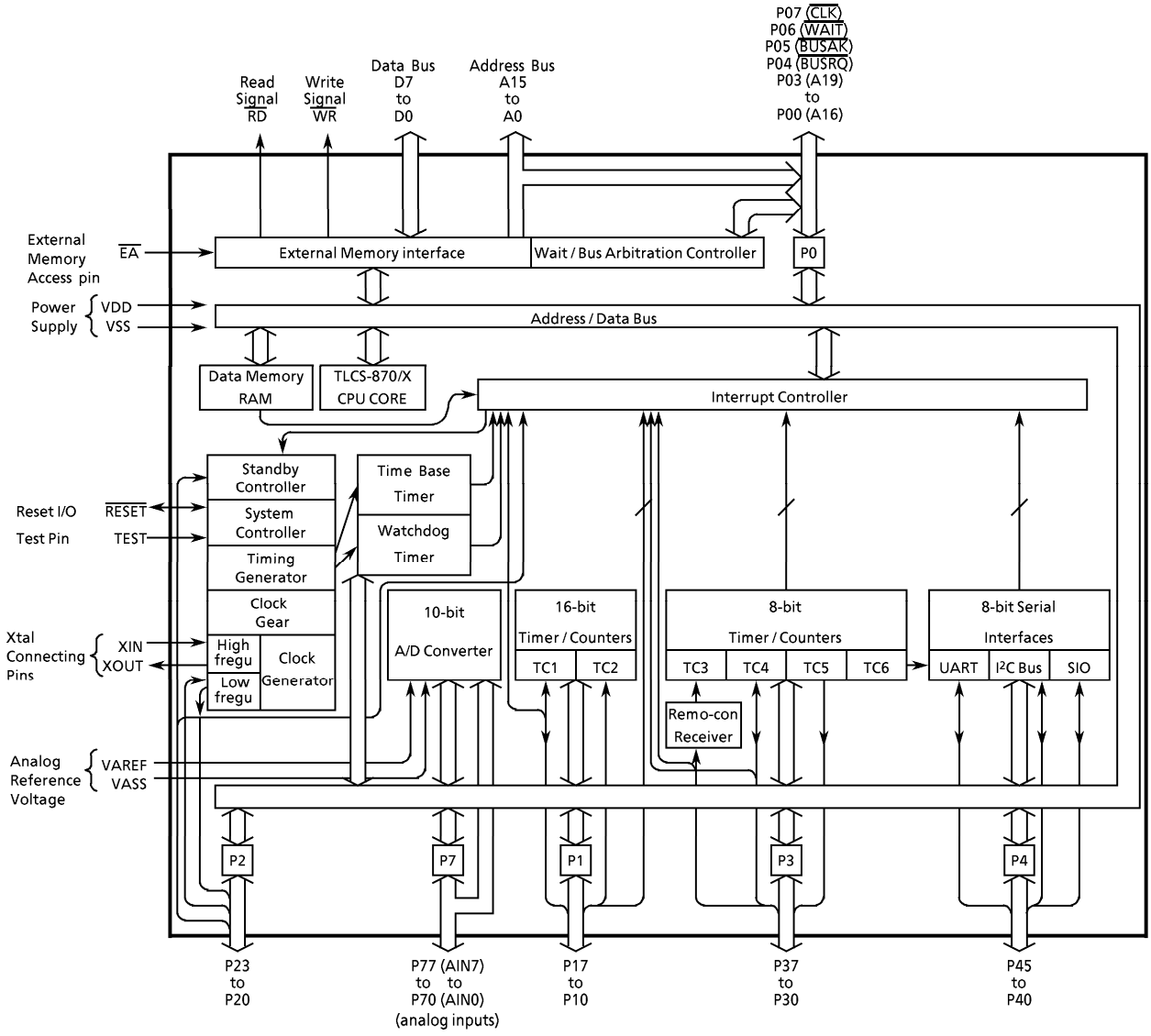
- ◆Time Base Timer (Interrupt frequency : 1 kHz to 16384 kHz)
- ◆Watchdog Timer
- ◆Divider output (frequency : 1 kHz to 8 kHz)
- ◆Two 8-bit Serial Interfaces
  - 8-bit UART (Parity. framing. overrun error detection)
  - 8-bit Serial Bus (I^2C-Bus for multi-master system and SIO)
- ◆10-bit successive approximate type A/D converter
  - 8 analog inputs
  - Conversion time : 59 μs at 12.5 MHz, 44 μs at 4.2 MHz
- ◆Dual clock operation
- ◆Five Power saving operating modes
  - STOP mode : Oscillation stops. Battery / Capacitor back-up. Release by stop pin input.
  - SLOW mode : Low power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE1 mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts. (CPU restarts)
  - IDLE2 mode : CPU stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP mode : CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ◆Wide operating voltage : 2.7 to 5.5 V at 4.2 MHz / 32.768 kHz, 4.5 to 5.5 V at 12.5 MHz / 32.768 kHz
- ◆Emulation Pod : BM88C060F0A

Pin Assignments (Top View)

P-LQFP80-1212-0.50A



Block Diagram



Pin Function

Pin name	Input / Output	Function	
P07 ($\overline{CLK}$)	I/O (Output)	8-bit programmable input / output ports (tri-state). Each bit of these ports can be individually configured as an input or an output. When used as a wait request input, a bus release request input, an external interrupt input, or a timer counter input, corresponding bit must be configured as input . When used as a divided-by-4 clock output, a bus acknowledge output, PPG output, or a divider output, the output latch must be set to "1" and corresponding bit must be configured as output. After reset, P03 to P00 are address buses. When used as a port, these ports must be set to the ports by EXPCR.	Divided-by-4 clock output
P06 ($\overline{WAIT}$)	I/O (Input)		Wait request input
P05 ($\overline{BUSAK}$)	I/O (Output)		Bus acknowledge output
P04 ($\overline{BUSRQ}$)	I/O (Input)		Bus request input
P03 (A19) to P00 (A16)	I/O (Output)		Upper address bus (external memory connect)
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer / Counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{DVO}$)			Divider output
P12 (INT2/TC1)	I/O (Input)		External interrupt input 2 or Timer / Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P23	I/O	4-bit input / output port with latch. When used as an input port, a resonator connecting pin, an external interrupt input, or a STOP mode release input, the output latch must be set to "1".	
P22 (XTOUT)	I/O (Output)		Xtal connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P37, P36	I/O	8-bit input / output port (large current output) with latch. When used as an input port, PWM output, an external interrupt input, or a timer counter input, the output latch must be set to "1".	
P35 (INT4 / TC4)	I/O (Input)		External interrupt input 4 or Timer / Counter 4 input
P34 (INT3 / TC3)			External interrupt input 3 or Timer / Counter 3 input
P33 ($\overline{PWM5}$ / $\overline{PDO5}$)	I/O (Output)		8-bit PWM output 5 or, 8-bit programmable divider output 5
P32 ($\overline{PWM4}$ / $\overline{PDO4}$)			8-bit PWM output 4 or, 8-bit programmable divider output 4
P31, P30	I/O		
P45 (SDA / SO)	I/O (I/O)	6-bit input / output port with latch. When used as an input port or a serial interface pin, the output latch must be set to "1".	SIO data output I^2C bus data I/O
P44 (SCL / SI)			SIO data input I^2C bus clock I/O
P43 ($\overline{SCK}$)			SIO clock input / output
P42 (TxD)			UART data output
P41 (RxD)			UART data input
P40			
P77 (AIN7) to P70 (AIN0)	I/O (Input)	8-bit programmable input / output port (tri-state). Each bit of these ports can be individually configured as an input or an output. When used as an analog input, these ports must be set to the analog input mode by P7CR and select the channel in ADCCR.	A/D converter analog input (ch 7 to ch 0)

Pin name	Input / Output	Function
A15 to A0	Output	Lower address bus (external memory connect)
D7 to D0	I/O	Data bus (external memory connect)
$\overline{RD}$	Output	Read strobe to an extrnal memory
$\overline{WR}$		Write strobe to an extrnal memory
$\overline{EA}$	Input	External memory access input. Be tied to low.
XIN, XOUT	Input, Output	Xtal connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output / address-trap-reset output / system-clock-reset output.
TEST	Input	Test pin for out-going test. Be tied to low.
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)
VAREF, VASS		Analog reference voltage for A/D converter (High, Low)

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.
This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TLCS-870 / X Series is capable of addressing 1M bytes of memory. Figure 1-1 shows the memory address map of the 88C060. The memory of the 88C060 is organized with 3 address spaces such as ROM, RAM SFR (Special Function Register). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR address space. There are 16 banks of the general-purpose register. The register banks are also assigned to the first 128 bytes of the RAM address space.

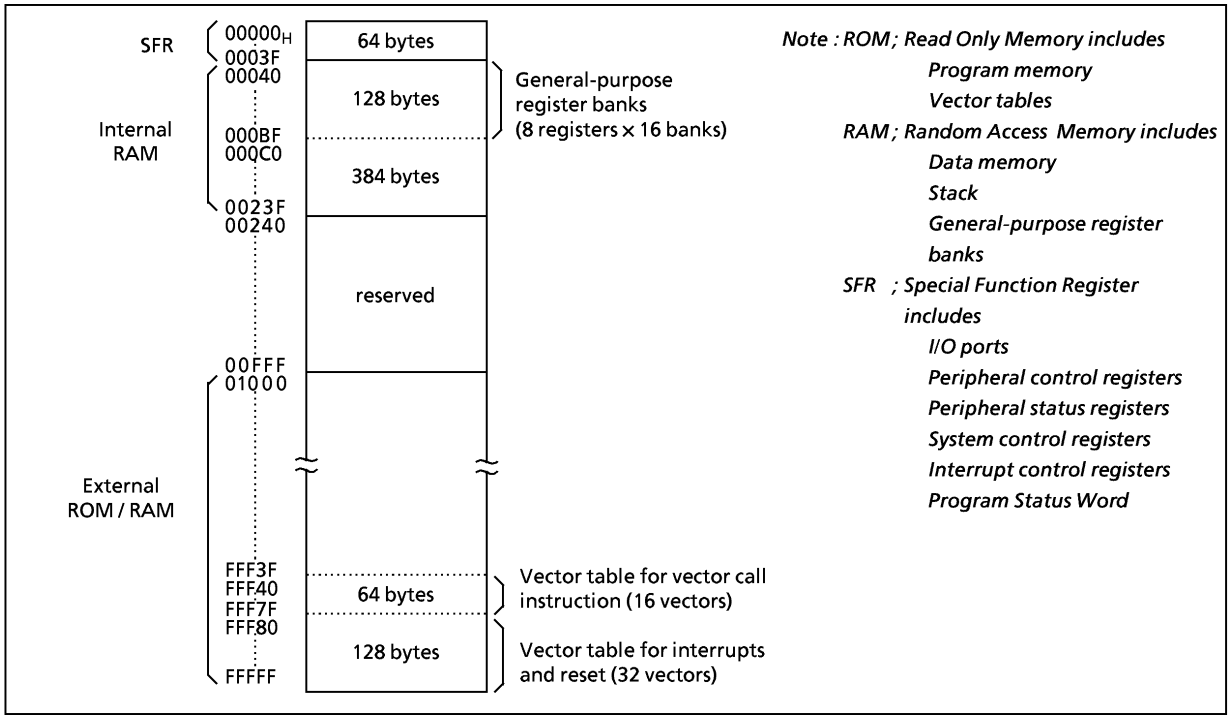


Figure 1-1. Memory address map

1.2 Program Memory (ROM)

The 88C060 can address up to 1M bytes of external program memory space except the first 4K bytes space (00000_H to $00FFF_H$).
The 88C060 does not have internal ROM. An external program memory must be connected.

1.3 Data Memory (ROM)

The 88C060 can address up to 1M bytes of data memory space. Data memory consists of internal data memory (on-chip RAM) and external data memory (RAM and / or ROM). The 88C060 has 512 bytes of static RAM. The first 128 bytes (00040_H to $000BF_H$) of the internal RAM are also used as general-purpose register banks.
The data memory contents become unstable when the power supply is turned on ; therefore, the data memory should be initialized by an initialization routine.

Electrical Characteristics

Absolute Maximum Rating

(V_{SS} = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}	P21, P22, $\overline{RESET}$, Tri-st	– 0.3 to V_{DD} + 0.3	
	V_{OUT2}	P20, P23, Sink Open Drain Port	– 0.3 to 5.5	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P4, P7 port	3.2	mA
	I_{OUT2}	A19-0, D7-0, $\overline{RD}$, $\overline{WR}$	12	
	I_{OUT3}	P3	30	
Output Current (Total)	ΣI_{OUT1}		80	
	ΣI_{OUT2}		120	
Power Dissipation (Topr = 70 °C)	PD		330	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 12.5 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode	2.7		
			fc = 4.2 MHz	NORMAL1, 2 mode			
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis and TTL input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}	Except TLL input	$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
	V_{IH4}	TTL input (Data bus)	V_{DD} = 5 V		2.2		
			V_{DD} = 3 V		V_{DD} – 0.2		
Input Low Voltage	V_{IL1}	Except hysteresis and TTL input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}	Except TTL input	$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
	V_{IL4}	TTL input (Data bus)	V_{DD} = 5 V			0.8	
			V_{DD} = 3 V			0.2	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 V to 5.5 V (Normal 1, 2 modes)		1.0	12.5	MHz
			V_{DD} = 2.7 V to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note2 : fc (Min.) are calculated at using clock Gear as follow :
(Minimum value of fc) = (pre-scaled ration) × 1 [MHz]

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST, $\overline{EA}$	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tir-state Port					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
	R_{IN3}	TEST		–	70	–	
Oscillator Feed-back Resistance	R_{fx}	XIN-XTOUT		–	1.2	–	MΩ
	R_{fxt}	XTIN-XTOUT		–	6	–	
Output Leakage Current	I_{LO1}	Sink Open Drain Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tir-st port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0V	–	–	± 2	
Output High Voltage	V_{OH2}	Tir-st port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
	V_{OH3}	A19-0, D7-0, $\overline{RD}$, $\overline{WR}$	V_{DD} = 4.5 V, I_{OH} = – 400 μs	2.4	–	–	
Output Low Voltage	V_{OL3}	A19-0, D7-0, $\overline{RD}$, $\overline{WR}$	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.45	V
Output Low Voltage	I_{OL1}	Except XOUT, P3, A19-0, D7-0, $\overline{RD}$, $\overline{WR}$	V_{DD} = 4.5 V, V_{OL} = 0.4 V	–	1.6	–	mA
	I_{OL3}	P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	
Supply Current in NORMAL1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 12.5 MHz fs = 32.768 kHz	–	15	20	mA
Supply Current in IDLE1, 2 mode				–	6	8	
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1 : Typical values show those at T_{opr} = 25 °C, V_{DD} = 5 V.
Note 2 : Input current I_{IN1}, I_{IN3} : The current through pull-up or pull-down resistor is not included.
Note 3 : IDD : Except for IREF.

A.C. Characteristics

(1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85 °C)

(1) - ① Clock

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL1, 2 mode	0.32	–	4	μs
		In IDLE1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) fc = 12.5 MHz	33.75	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XIN input) fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

(1) - ② External Memory Interface

Parameter	Symbol	Variable		12.5 MHz		Unit
		Min	Max	Min	Max	
Address Setup to $\overline{RD}$	t_{ARD}	0.5t – 30	–	10	–	ns
Address Setup to $\overline{WR}$	t_{AWR}	1.5t – 30	–	90	–	ns
Address Hold Time After $\overline{RD}$ / $\overline{WR}$	t_{RDA}	0.5t – 35	–	5	–	ns
	t_{WRA}					
Address to Valid Data In	t_{ADI}	–	3.5t – 95	–	185	ns
$\overline{RD}$ to Valid Data In	t_{RDDS}	–	3.0t – 100	–	140	ns
$\overline{RD}$ Low Pulse Width	t_{WRD}	0.3t – 40	–	200	–	ns
Input Data Hold After $\overline{RD}$	t_{RDDH}	0	–	0	–	ns
$\overline{WR}$ Low Pulse Width	t_{WWR}	2.0t – 40	–	120	–	ns
Data Setup to $\overline{WR}$	t_{DWR}	2.0t – 40	–	120	–	ns
Data Hold After $\overline{WR}$	t_{WRDH}	0.5t – 35	–	5	–	ns
XIN to Address Delay	t_{XINA}	–	140	–	140	ns
XTIN to Address Delay	t_{XTINA}	–	340	–	340	ns

Note : t = tcy / 4 (t = 80 ns @ fc = 12.5 MHz)

(1) - ③ Wait

Parameter	Symbol	Variable		12.5 MHz		Unit
		Min	Max	Min	Max	
Address Setup to $\overline{WAIT}$	t_{AWTF}	–	1.5t – 100	–	20	ns
Address Setup to $\overline{WAIT}$	t_{AWTR}	1.5t + 20	–	140	–	ns
$\overline{RD}$ Setup to $\overline{WAIT}$	t_{RDWTF}	–	1.0t – 100	–	– 20	ns
$\overline{RD}$ Setup to $\overline{WAIT}$	t_{RDWTR}	1.0t + 20	–	100	–	ns
$\overline{WR}$ Setup to $\overline{WAIT}$	t_{WRWTR}	20	–	20	–	ns
Address Valid to $\overline{CLK}$	t_{ACLK}	–	4.0t + 35	–	355	ns
$\overline{CLK}$ Pulse Width	t_{WCLKL} / t_{WCLKH}	2.0t – 50	–	110	–	ns
$\overline{CLK}$ Set up to WAIT	t_{CLKWT}	–	1.5t – 70	–	50	ns

Note: t = tcy / 4 (t = 80 ns @ fc = 12.5 MHz)

(1) - ④ Bus Arbitration

Parameter	Symbol	Variable		12.5 MHz		Unit
		Min	Max	Min	Max	
Bus Floating to $\overline{BUSAK}$	t_{BFAK}	0.5t – 30	–	10	–	ns
Period from $\overline{BUSRQ}$ to $\overline{BUSAK}$	t_{BACK}	–	5.5t + 30	–	470	ns

Note 1: t = tcy / 4 (t = 80 ns @ fc = 12.5 MHz)
Note 2: When the $\overline{BUSRQ}$ is set to "0" during "Wait Cycle", the Bus will be released after the completion of "Wait Cycle".
Note 3: When the $\overline{BUSRQ}$ is set to "0" just before interrupt request, the Bus will be released after the completion of current instruction execution and interrupt sequence.

A.C. Meaurement Condition

Output Level : High 2.2 V / Low 0.8 V, CL = 100pF

Input level : High 2.4 V / Low 0.4 V (D7 to D0)

High 0.7 V_{DD} / Low 0.3 V_{DD} ($\overline{WAIT}$)

High 0.8 V_{DD} / Low 0.2 V_{DD} (Except D7 to D0 and $\overline{WAIT}$)

A.C. Charactiristics (2) (V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85 °C)

(2) - ① Clock

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL1, 2 mode	0.95	–	4	μs
		In IDLE1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) fc = 4.2 MHz	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input) fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

(2) - ② External Memory Interface

Parameter	Symbol	Variable		4.2 MHz		Unit
		Min	Max	Min	Max	
Address Setup to $\overline{RD}$	t_{ARD}	0.5t – 110	–	9	–	ns
Address Setup to $\overline{WD}$	t_{AWR}	1.5t – 120	–	237	–	ns
Address Hold Time After $\overline{RD}$ / $\overline{WR}$	t_{RDA}	0.5t – 110	–	9	–	ns
	t_{WRA}					
Address to Valid Data In	t_{ADI}	–	3.5t – 270	–	563	ns
$\overline{RD}$ to Valid Data In	t_{RDDS}	–	3.0t – 205	–	509	ns
$\overline{RD}$ Low Pulse Width	t_{WRD}	3.0t – 40	–	674	–	ns
Input Data Hold After $\overline{RD}$	t_{RDDH}	0	–	0	–	ns
$\overline{WR}$ Low Pulse Width	t_{WWR}	2.0t – 85	–	391	–	ns
Data Setup to $\overline{WR}$	t_{DWR}	2.0t – 50	–	426	–	ns
Data Hold After $\overline{WR}$	t_{WRDH}	0.5t – 110	–	9	–	ns

Note : t = tcy / 4 (t = 238 ns @ fc = 4.2 MHz)

(2) - ③ Wait

Parameter	Symbol	Variable		4.2 MHz		Unit
		Min	Max	Min	Max	
Address Setup to $\overline{WAIT}$	t_{AWTF}	–	1.5t – 257	–	100	ns
Address Setup to $\overline{WAIT}$	t_{AWTR}	1.5t + 125	–	482	–	ns
$\overline{RD}$ Setup to $\overline{WAIT}$	t_{RDWTF}	–	1.0t – 165	–	73	ns
$\overline{RD}$ Setup to $\overline{WAIT}$	t_{RDWTR}	1.0t + 125	–	363	–	ns
$\overline{WR}$ Setup to $\overline{WAIT}$	t_{WRWTR}	50	–	50	–	ns
Address Valid to $\overline{CLK}$	t_{ACLK}	–	4.0t + 70	–	1022	ns
$\overline{CLK}$ Pulse Width	t_{WCLKL} / t_{WCLKH}	2.0t – 118	–	358	–	ns
$\overline{CLK}$ Set up to WAIT	t_{CLKWT}	–	1.5t – 170	–	187	ns

Note: t = tcy / 4 (t = 238 ns @ fc = 4.2 MHz)

(2) - ④ Bus Arbitration

Parameter	Symbol	Variable		4.2 MHz		Unit
		Min	Max	Min	Max	
Bus Floating to $\overline{BUSAK}$	t_{BFAK}	0.5t – 109	–	10	–	ns
Period from $\overline{BUSRQ}$ to $\overline{BUSAK}$	t_{BACK}	–	5.5t + 109	–	1200	ns

Note 1: t = tcy / 4 (t = 238 ns @ fc = 4.2 MHz)
Note 2 : When the $\overline{BUSRQ}$ is set to "0" during "Wait Cycle", the Bus will be released after the completion of "Wait Cycle".
Note 3 : When the $\overline{BUSRQ}$ is set to "0" just before interrupt request, the Bus will be released after the completion of current instruction execution and interrupt sequence.

A.C. Meaurement Condition

Output Level : High 0.7 V_{DD} / Low 0.3 V_{DD}, CL = 100 pF

Input level : High 0.9 V_{DD} / Low 0.1 V_{DD}

A / D Conversion Characteristics

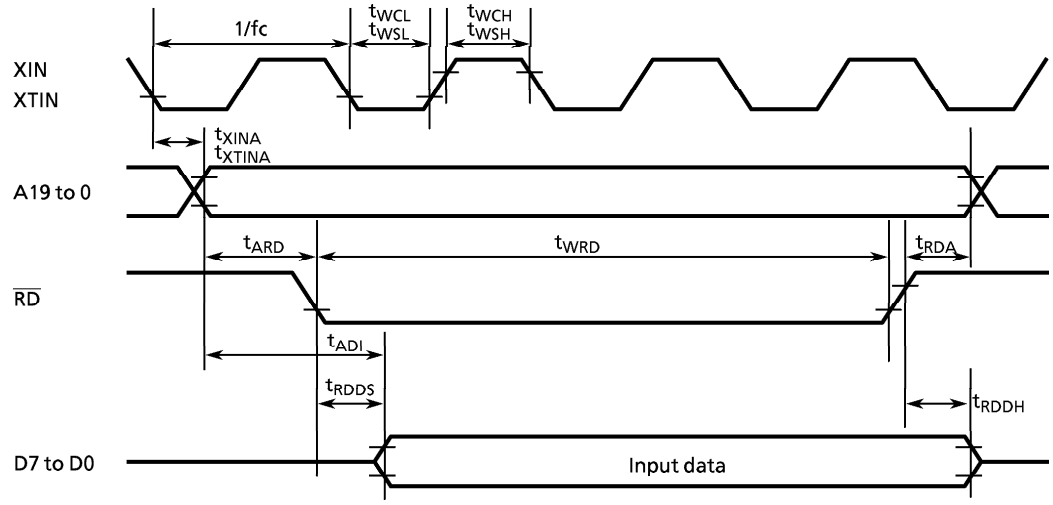
(Topr = – 40 to 85 °C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	V_{SS}	
Analog Reference Voltage Range	$\triangle V_{AREF}$		2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{DD} = AVDD = VAREF = 5.5 V VSS = AVSS = VASS = 0.0 V	–	0.5	1.0	mA
Non-Linearity Error		V_{DD} = 5.0 to 5.5 V, V_{SS} = 0.0V AVDD = VAREF = 5.000 V AVSS = VASS = 0.000 V low Speed Conversion (58.9 μs, @ 12.5 MHz)	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	
Non-Linearity Error		V_{DD} = 2.7 to 5.5 V, V_{SS} = 0.0V AVDD = VAREF = 2.700 V AVSS = VASS = 0.000 V Hihg speed conversion (43.7 μs, @ 4.2 MHz)	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

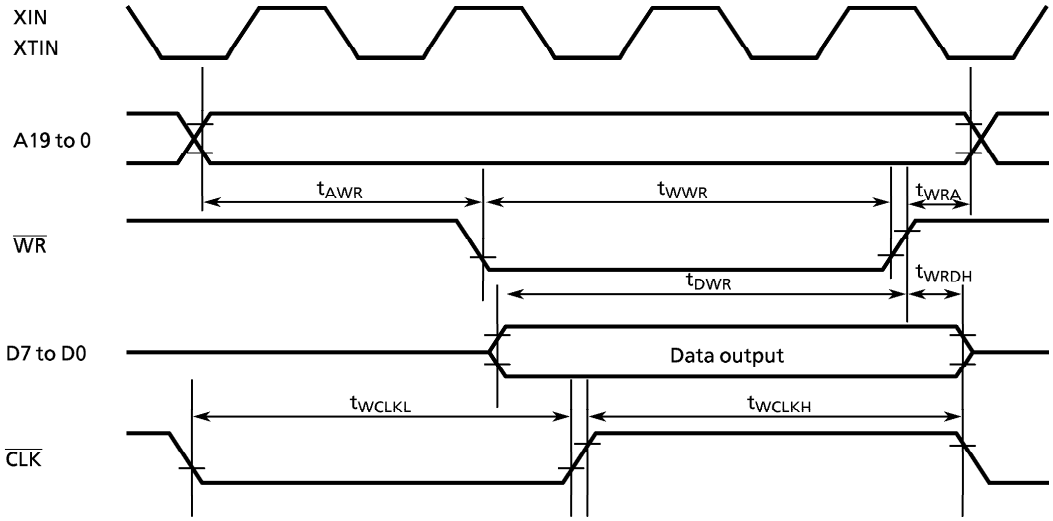
Note : $\triangle V_{AREF} = V_{AREF} - V_{ASS}$

Timing Chart

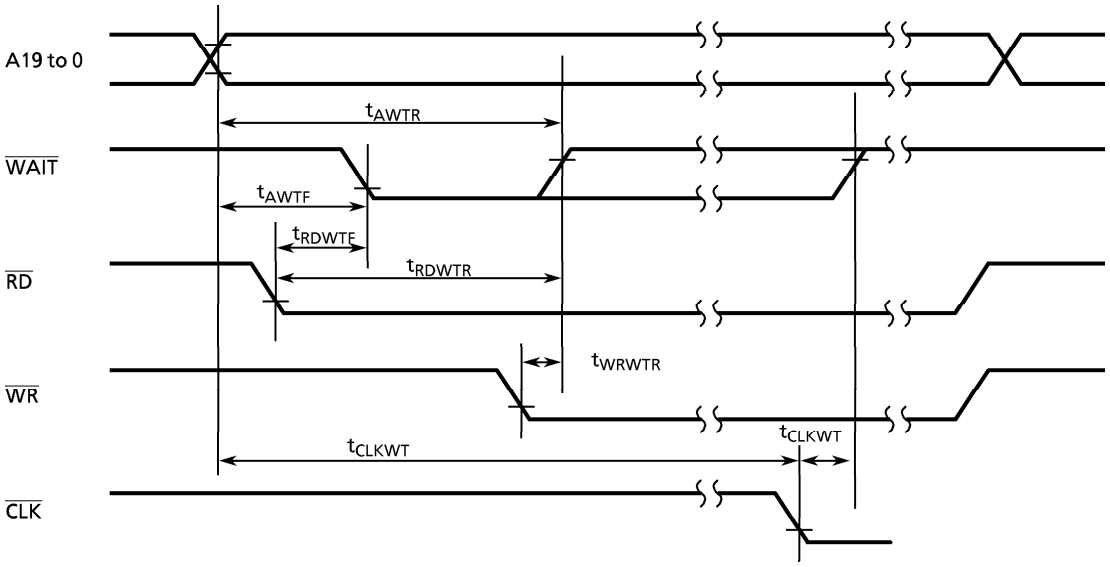
(1) Read Cycle



(2) Write Cycle



(3) Wait Timing



(4) Bus Arbitation