TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91CU10

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

****CAUTION****

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low-Voltage CMOS 16-Bit Microcontrollers

TMP91CU10F

1. Outline and Device Characteristics

The TMP91CU10 is an original Toshiba TLCS-900/L1 Series 16-bit microcontroller. The TMP91CU10 integrates a 16-bit CPU, ROM, RAM, multi-functional timer and event counter, general-purpose serial interface, an A/D converter and various other units in a single chip, and has been developed for controlling medium- to large-scale equipment.

The TMP91CU10 is housed in a 100-pin mini flat package.

The device characteristics are as follows:

(1) Original high-speed 16-bit CPU (900/H CPU)
- TLCS-90/900 instruction mnemonics (upwards compatible)
- 16-Mbyte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed μDMA: 4 channels (1.18 μs at 13.5 MHz) (1.0 μs at 16 MHz)

(2) Minimum instruction execution time
- 400 ns at 10 MHz (V_{CC} = 2.0 V) for mask ROM products only
- 296 ns at 13.5 MHz (VCC = 3.0 V)

(3) Internal RAM: 3 Kbytes
Internal ROM: 96 Kbytes

(4) External memory expansion
- Can be expanded up to 16 Mbytes (for both programs and data).
- AM8/$\overline{16}$ pin (selects the external data bus width)
- Can mix 8- and 16-bit external data buses (dynamic bus sizing).

(5) Chip Select and Wait controller: 3 blocks

(6) 8-bit timer: 8 channels
- Including event count function: 2 channels

(7) 16-bit timer and event counter: 2 channels

(8) General-purpose serial interface: 3 channels
- UART and Synchronous modes

(9) 10-bit A/D converter: 8 channels

(10) Watchdog timer

(11) Interrupt functions
- 2 CPU interrupts (SWI instruction and Illegal instruction)
- 26 internal interrupts 7-level priority can be set.
- 10 external interrupts 7-level priority can be set.

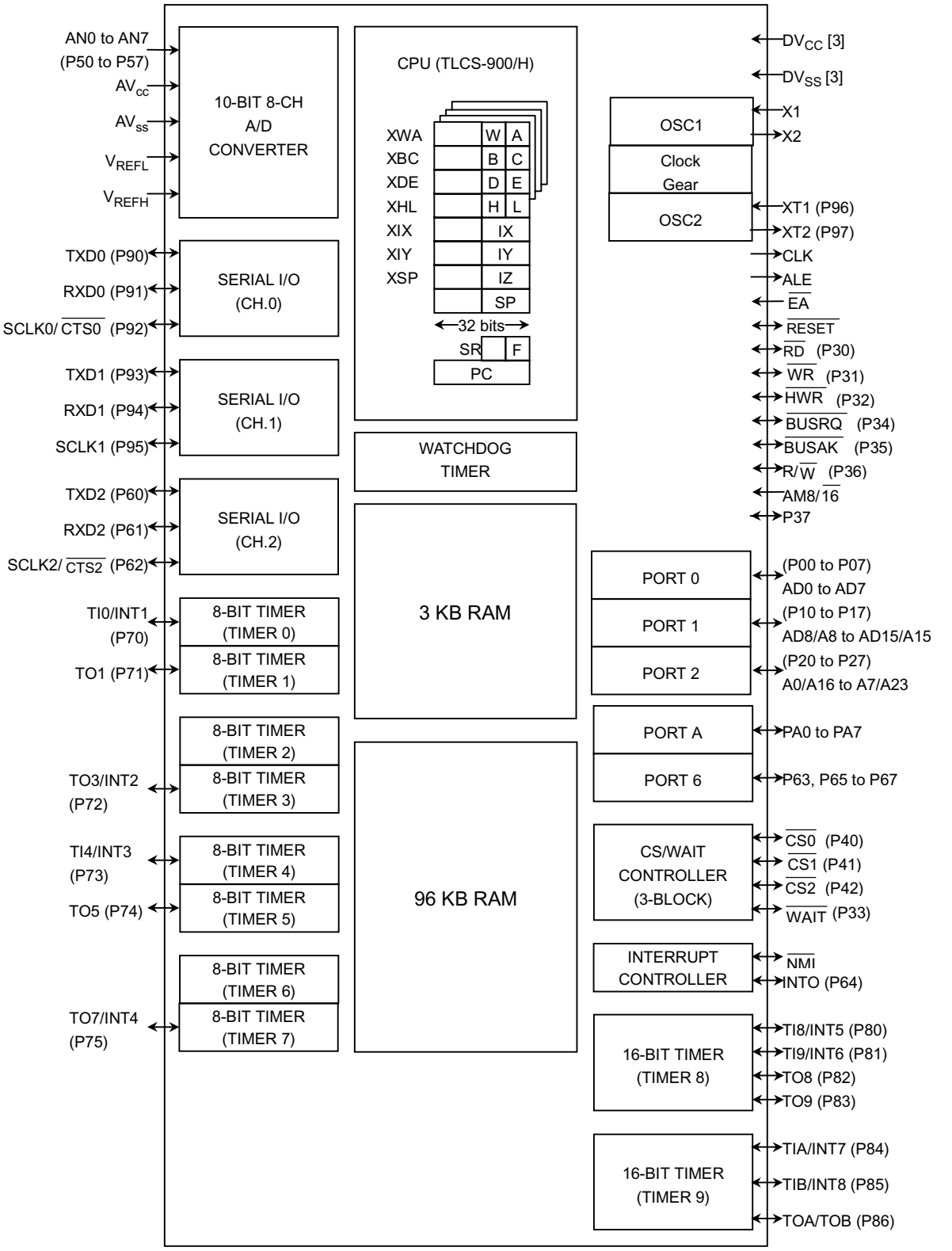
(12) I/O ports: 80 pins

(13) Standby function: 4 Halt modes (Run, Idle2, Idle1, Stop)

(14) Clock gear function
- Clock gear: High-frequency clock can be changed from fc to fc/16.
- Dual clock operation

(15) Low operating voltage
- 2.0 to 3.6 V

(16) Package
- Compact 14 mm × 14 mm × 1.4 mm (0.5 mm pitch)



( ): Default function after reset

Figure 1.1 TMP91CU10F Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP91CU10, their names and functions are described as follows:

2.1 Pin Assignment

Figure 2.1.1 shows the pin assignment of the TMP91CU10.

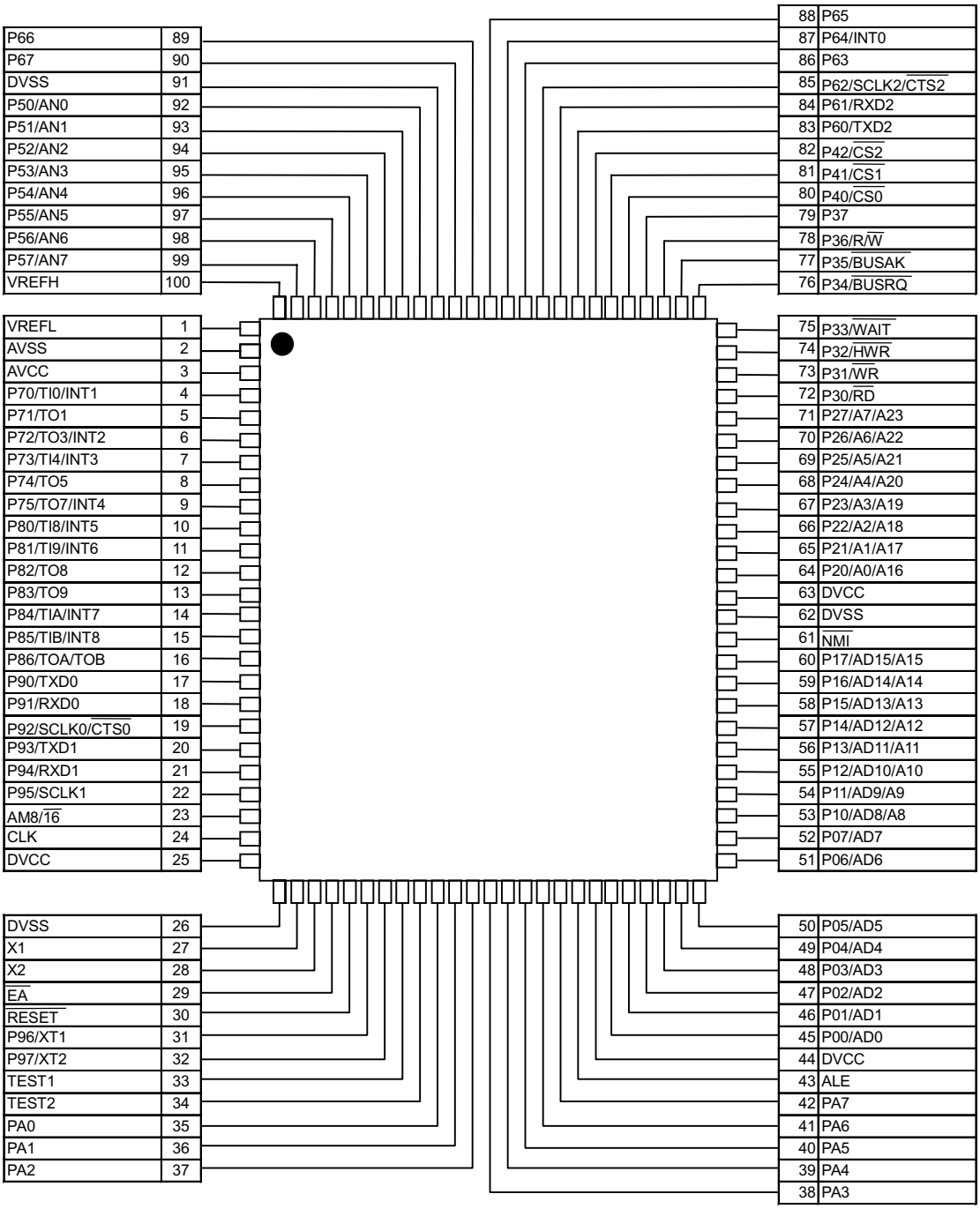


Figure 2.1.1 Pin Assignment diagram

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described in Table 2.2.1.

Table 2.2.1 Pin names and Functions (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O I/O	Port 0: I/O port that allows I/O to be selected at the bit level Address (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O I/O Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level (with pull-up resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory When P3<RDE> = 0 and P3FC<P30F> = 1, $\overline{RD}$ is output and internal memory is read.
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins D0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data to pins D8 to D15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU Bus Wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus Request: Signal used to request high impedance on pins D0 to D15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$.
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus Acknowledge: Signal used to acknowledge high impedance on pins D0 to D15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ by receiving $\overline{BUSRQ}$.
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37	1	I/O	Port 37: I/O port
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip Select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip Select 1: Outputs 0 when address is within specified address area.
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-down resistor) Chip Select 2: Outputs 0 when address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Pin used to input to AD converter
P60 TXD2	1	I/O Output	Port 60: I/O port Serial Send Data 2 (programmable open drain)
P61 RXD2	1	I/O Input	Port 61: I/O port Serial Receive Data 2 (programmable open drain)
P62 SCLK2 $\overline{CTS2}$	1	I/O I/O Input	Port 62: I/O port Serial Clock I/O 2 Serial Data Send Enable 2 (Clear to Send) (programmable open drain)
P63	1	I/O	Port 63: I/O port
P64 INT0	1	I/O Input	Port 64: I/O port Interrupt Request pin 0: Interrupt request pin with programmable level/rising edge
P65 to P67	3	I/O	Port 65 to 67: I/O ports

Note: A DMAC controller's internal memory or I/O devices cannot be accessed using $\overline{BUSRQ}$ and $\overline{BUSAK}$.

Table 2.2.1 Pin names and Function (2/3)

Pin name	Number of pins	I/O	Functions
P70	1	I/O	Port 70: I/O port
TI0		Input	Timer Input 0: Timer 0 input pin
INT1		Input	Interrupt Request pin 1: Interrupt request on rising edge
P71	1	I/O	Port 71: I/O port
TO1		Output	Timer Output 1: Timer 0 or 1 output
P72	1	I/O	Port 72: I/O port
TO3		Output	Timer Output 3: Timer 2 or 3 output
INT2		Input	Interrupt Request pin 2: Interrupt request on rising edge
P73	1	I/O	Port 74: I/O port
TI4		Input	Timer Input 4: Timer 4 input
INT3		Input	Interrupt Request pin 3: Interrupt request on rising edge
P74	1	I/O	Port 75: I/O port
TO5		Output	Timer Output 5: Timer 4 or 5 output
P75	1	I/O	Port 76: I/O port
TO7		Output	Timer Output 7: Timer 6 or 7 output
INT4		Input	Interrupt Request pin 4: Interrupt request on rising edge
P80	1	I/O	Port 80: I/O port
TI8		Input	Timer Input 8: Timer 8 count or capture trigger signal input
INT5		Input	Interrupt Request pin 5: Interrupt request pin with programmable rising / falling edge
P81	1	I/O	Port 81: I/O port
TI9		Input	Timer Input 9: Timer 8 count or capture trigger signal input
INT6		Input	Interrupt Request pin 6: Interrupt request on rising edge
P82	1	I/O	Port 82: I/O port
TO8		Output	Timer Output 8: Timer 8 output pin
P83	1	I/O	Port 83: I/O port
TO9		Output	Timer Output 9: Timer 9 output pin
P84	1	I/O	Port 84: I/O port
TIA		Input	Timer Input A: Timer 9 count or capture trigger signal input
INT7		Input	Interrupt Request pin 7: Interrupt request pin with programmable rising / falling edge
P85	1	I/O	Port 85: I/O port
TIB		Input	Timer Input B: Timer 9 count or capture trigger signal input
INT8		Input	Interrupt Request pin 8: Interrupt request on rising edge
P86	1	I/O	Port 86: I/O port
TOA		Output	Timer Output A: Timer A output pin
TOB		Output	Timer Output B: Timer B output pin
P90	1	I/O	Port 90: I/O port
TXD0		Output	Serial Send Data 0 (programmable open drain)
P91	1	I/O	Port 91: I/O port
RXD0		Input	Serial Receive Data 0
P92	1	I/O	Port 92: I/O port
SCLK0		I/O	Serial Clock I/O 0
$\overline{CTS0}$		Input	Serial Data Send Enable 0 (Clear to Send)
P93	1	I/O	Port 93: I/O port
TXD1		Output	Serial Send Data 1 (programmable open drain)
P94	1	I/O	Port 94: I/O port
RXD1		Input	Serial Receive Data 1
P95	1	I/O	Port 95: I/O port
SCLK1		I/O	Serial Clock I/O 1
P96	1	I/O	Port 96: I/O port (open drain output)
XT1		Input	Low-frequency oscillator connecting pin
P97	1	I/O	Port 97: I/O port (open drain output)
XT2		Output	Low-frequency oscillator connecting pin

Table 2.2.1 Pin names and Function (3/3)

Pin name	Number of pins	I/O	Functions
PA0 to PA7	3	I/O	Port A0 to A7: I/O ports
ALE	1	Output	Address Latch Enable (can be disabled for reducing noise.)
$\overline{NMI}$	1	Input	Non-Maskable Interrupt Request pin: Interrupt request pin with programmable falling edge or both edges.
CLK	1	Output	Clock Output: Outputs (external input clock/4) clock. Pulled-up during reset
$\overline{EA}$	1	Input	The Vcc pin should be connected.
AM8/$\overline{16}$	1	Input	Address Mode: Selects external data bus width. The Vcc pin should be connected. The data bus width for external access is set by the Chip Select/WAIT Control register and the Port 1 Control register.
TEST1/TEST2	2	Output /Input	TEST1 Should be connected with TEST2 pin.
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
VREFH	1	Input	Reference power supply input pin for AD converter (H)
VREFL	1	Input	Reference power supply input pin for AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND power supply pin for AD converter (0 V)
X1/X2	2	I/O	Oscillator connecting pin
TEST1/TEST2	2	Output /Input	TEST1 should be connected with TEST2 pin.
DVCC1	3		Power supply pin
DVSS	3		GND pin (0 V)

Note: All pins that have built-in pull-up / pull-down resistors (other than the $\overline{RESET}$ pin) can be disconnected from their built-in pull-up / pull-down resistors by software.

3. Operation

This section describes the functions and basic operations of the TMP91CU10. Please also refer to Section 7, Precautions, which describes some points requiring careful attention.

3.1 CPU

TMP91CU10 device has a built-in high-performance 16-bit CPU (TLCS-900/L1 CPU). (For a basic description of the CPU operation, see the information on the TLCS-900/L1 CPU).

This section describes some CPU functions unique to the TMP91CU10 that are not described in the description of the TLCS-900/L1 CPU.

3.1.1 Reset

Figure 3.1.1 shows the basic timing chart for a Reset operation.

To reset a TMP91CU10 device, the $\overline{\text{RESET}}$ pin must be kept at 0 for at least ten consecutive system clock cycles (equivalent to 160 states: 24 μs at 13.5 MHz). The pin must be kept within the specified operating voltage range and stable clock oscillation must be maintained.

When a Reset signal is received, the CPU is set as follows:

- The Program Counter (PC) is set according to the Reset Vector that is stored from FFFF00H to FFFF02H.
  PC (7 to 0) ← data in location FFFF00H
  PC (15 to 8) ← data in location FFFF01H
  PC (23 to 16) ← data in location FFFF02H
- The Stack Pointer (XSP) for System mode is set to 100H.
- The <IFF2 to 0> bits of the Status register SR are set to 111. (The Mask register is set to interrupt level 7.)
- The <MAX> bit of SR is set to 1 (Maximum mode).
  (Note: This device does not support Minimum mode. Do not set <MAX> to 0.)
- The <REP2 to 0> bits of SR are set to 000. (The register banks are cleared to 0.)

When the Reset is released, instruction execution starts from PC (the Reset Vector). The Reset makes no changes to the values in any CPU internal registers other than those specifically mentioned above.

When a Reset is received, signal and data processing for built-in I/Os, ports and other pins is affected as follows:

- Initializes built-in I/O registers as described in the specifications.
- Sets port pins (including pins also used as built-in I/Os) to General-Purpose Input/Output Port mode.
- Pulls up the CLK pin to 1.
- Sets the ALE pin to High Impedance (Hi-Z).

Note 1: Resetting makes no change to the contents of any registed in the CPU except the Program Counter (PC), Status Register (SR) and Stack Pointer (XSP), nor to the data in the internal RAM.

Note 2: The CLK pin is pulled up during a Reset. When the voltage is externally reduced, there is a possibility of malfunction.

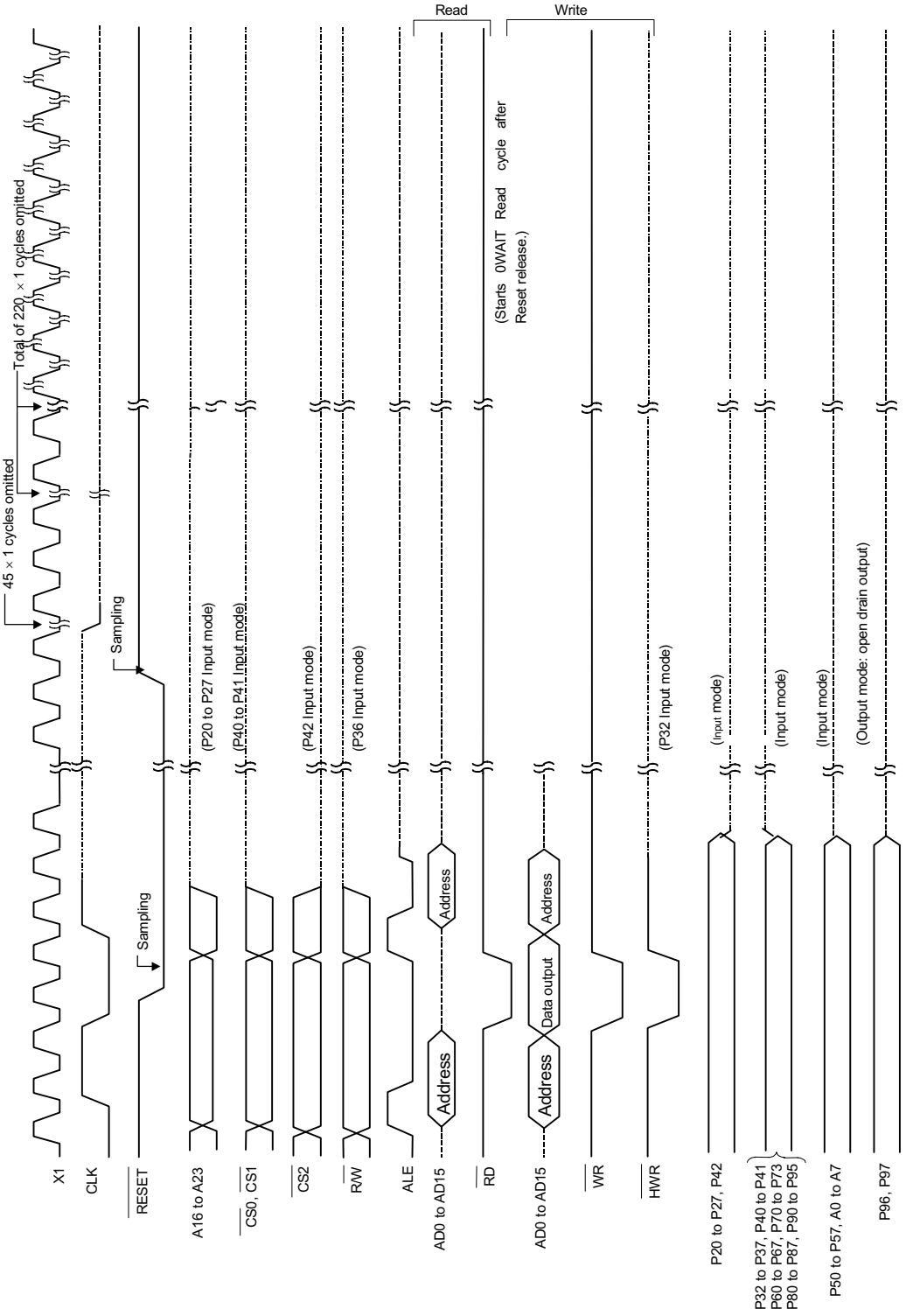
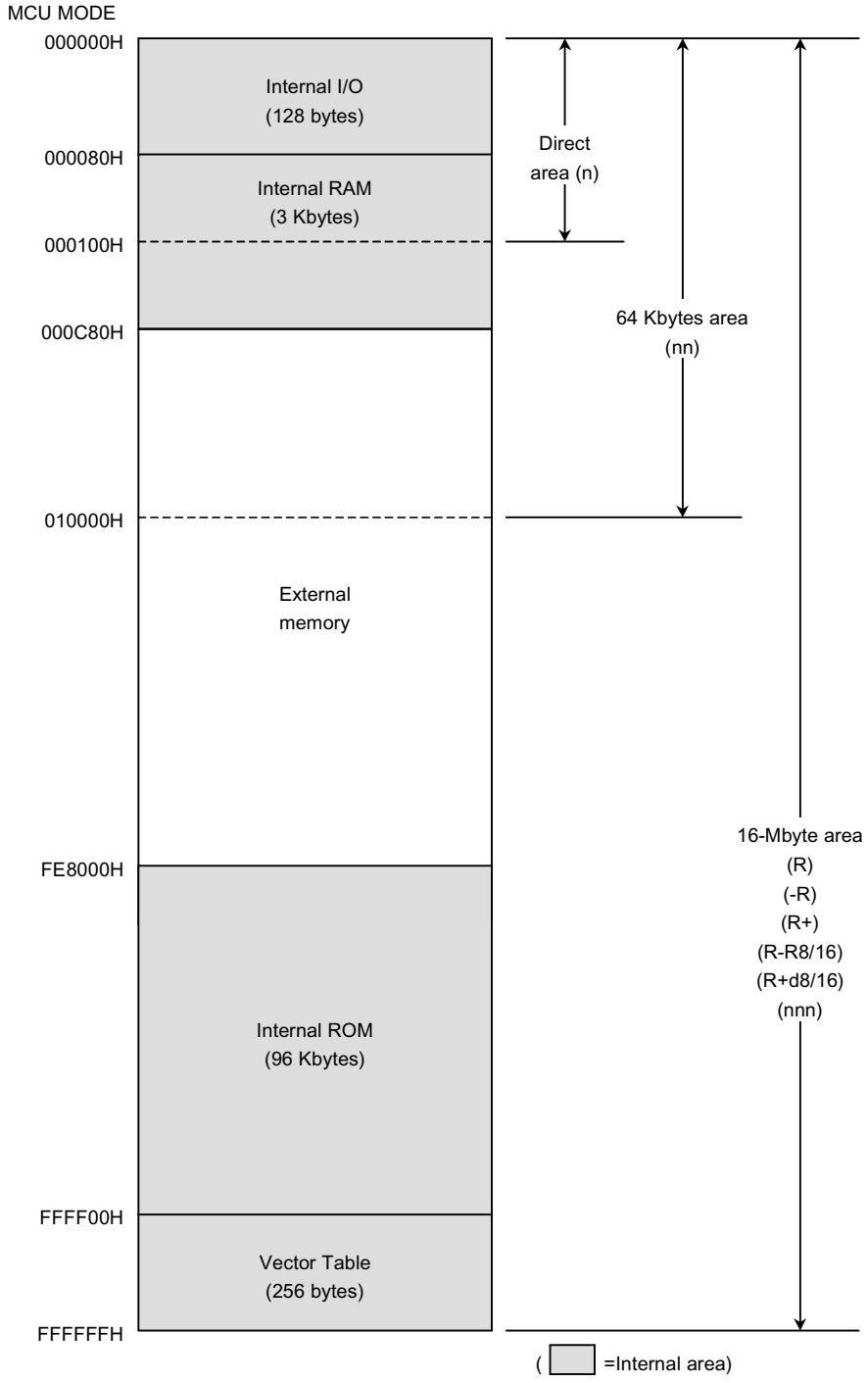


Figure 3.1.1 TMP91CU10F Reset Timing Chart

3.2 Memory Map

The TMP91CU10 uses an address area of 128 bytes as the internal I/O area, which is allocated from addresses 000000H to 00007FH. The CPU can access this internal I/O using a short internal code in Direct Addressing Mode.

Figure 3.2.1 shows the memory map and the accessible area for each CPU addressing mode.



Note: The stack pointer XSP is set to 100H after a Reset.

Figure 3.2.1 TMP91CU10 Memory Map

4. Electrical Characteristics

"X" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear=1/fc (SYSCR1<SYSCK, GEAR2 to 0>=0000).

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 4.0	V
Input Voltage	VIN	−0.5 to Vcc + 0.5	V
Output Current (total)	ΣIOL	120	mA
Output Current (total)	ΣIOH	−80	mA
Power Dissipation (Ta=85°C)	PD	600	mW
Soldering Temperature (10 s)	TSOLDER	260	°C
Storage Temperature	TSTG	−65 to 150	°C
Operating Temperature	TOPR	−40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note1)	Max	Unit
Power Supply Voltage AVCC=VCC AVSS=VSS=0V		VCC	fc = 4 to 16 MHz fs = 30 to 34 kHz (Ta = −40 to 85°C)	2.7		3.6	V
			fc = 4 to 10 MHz fs = 30 to 34 kHz (Ta = −40 to 85°C)	2.2 (Note 2)			
Input Low Voltage	AD0 to 15	VIL	Vcc ≥ 2.7 V	−0.3		0.8	V
			Vcc < 2.7 V			0.4	
	Port2 to A(exceptP87, P5)	VIL1	Vcc = 2.7 to 3.6 V			0.3 Vcc	
	$\overline{\text{RESET}}$, $\overline{\text{NIMI}}$, INT0	VIL2				0.25 Vcc	
	$\overline{\text{EA}}$, AM8/$\overline{16}$	VIL3				0.3	
	X1, Port5	VIL4				0.2 Vcc	
Input High Voltage	AD0 to 15	VIH	Vcc ≥ 2.7 V	2.2		Vcc+0.3	V
			Vcc < 2.7 V	2.0			
	Port2 to A(exceptP87)	VIH1	Vcc = 2.7 to 3.6 V	0.7 Vcc			
	$\overline{\text{RESET}}$, $\overline{\text{NIMI}}$, INT0	VIH2		0.75 Vcc			
	$\overline{\text{EA}}$, AM8/$\overline{16}$	VIH3		Vcc−0.3			
	X1	VIH4		0.8 Vcc			

Note 1: Typical values are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: The operation of the A/D converter is guaranteed at Vcc = 2.7 to 3.6 V.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ. (Note1)	Max	Unit
Output Low Voltage	VOL	IOL = 1.6 mA (Vcc = 2.7 to 3.6 V)				0.45	V
Output High Voltage	VOH1	IOH = –400 μA (Vcc = 2.2 V ± 10%)		1.4			
	VOH2	IOH = –400 μA (Vcc = 3 V ± 10 %)		2.4			
Darlington Drive Current (8 Output Pins max.)	IDAR (Note2)	VEXT = 1.5 V REXT = 1.1 kΩ (Vcc = 3 V ± 10%)		–1.0		–3.5	mA
Input Leakage Current	ILI	0.0 ≤ VIN ≤ Vcc			0.02	± 5	μA
Output Leakage Current	ILO	0.2 ≤ VIN ≤ Vcc–0.2			0.05	± 10	
Power Down Voltage (@STOP,RAM Back up)	VSTOP	VIL2 = 0.2 Vcc, VIH2 = 0.8 Vcc		2.0		6.0	V
RESET Pull Up Resister	RRST	Vcc = 3 V ± 10%		50		250	kΩ
		Vcc = 2.2 V ± 10%		80		500	
Pin Capacitance	CIO	fc = 1 MHz				10	pF
Schmitt Width $\overline{\text{RESET}}$, $\overline{\text{NIMI}}$, INT0	VTH			0.4	1.0		V
Programmable Pull Down Resistor	PKL	Vcc = 3 V ± 10%		30		200	kΩ
		Vcc = 2.2 V ± 10%		80		500	
Programmable Pull Up Resistor	PKH	Vcc = 3 V ± 10%		80		300	
		Vcc = 2.2 V ± 10%		80		500	
NORMAL2	Icc	Vcc = 3 V ± 10% fc = 13.5 MHz (Typ. : Vcc = 3.0 V)			14	23	mA
RUN					10	17	
IDLE2					6	11	
IDLE1					1.1	2.8	
NORMAL2		Vcc = 2.2 V ± 10% fc = 10 MHz (Typ. : Vcc = 2.2 V)			8.0	12	mA
RUN					4.5	9.5	
IDLE2					2.5	6.5	
IDLE1					0.5	1.5	
SLOW		Vcc = 3 V ± 10% fs = 32.768 kHz (Typ. : Vcc = 3.0 V)			40	55	μA
RUN					32	45	
IDLE2					18	35	
IDLE1					6	20	
STOP		Ta ≤ 50°C	Vcc = 2.0 to 3.6 V		0.2	10	μA
		Ta ≤ 70°C				20	
		Ta ≤ 85°C				50	

Note 1: Typical values are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: I-DAR is guaranteed for up to eight ports.

Note 3: I_{CC} measurement condition (NORMAL2):

All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 2.5 to 3.6 V

No.	Parameter	Symbol	Variable		12.5 MHz		16 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (=x)	t_{OSC}	62.5	31250	80		74		ns
2	CLK width	t_{CLK}	2x – 40		120		108		ns
3	A0 to A23 Valid→CLK Hold	t_{AK}	0.5x – 20		20		7		ns
4	CLK Valid→A0 to A23 Hold	t_{KA}	1.5x – 70		50		26		ns
5	A0 to A15 Valid→ALE Fall	t_{AL}	0.5x – 15		25		30		ns
6	ALE Fall→A0 to A15 Hold	t_{LA}	0.5x – 20		20		7		ns
7	ALE High Width	t_{LL}	x – 40		40		24		ns
8	ALE Fall→ $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 25		15		10		ns
9	$\overline{RD}$ / $\overline{WR}$ Rise→ALE Rise	t_{CL}	0.5x – 20		20		7		ns
10	A0 to A15 Valid→ $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 25		55		34		ns
11	A0 to A23 Valid→ $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACH}	1.5x – 50		70		61		ns
12	$\overline{RD}$ / $\overline{WR}$ Rise→A0 to A23 Hold	t_{CA}	0.5x – 25		15		0		ns
13	A0 to A15 Valid→D0 to D15 Input	t_{ADL}		3.0x – 55		130		182	ns
14	A0 to A23 Valid→D0 to D15 Input	t_{ADH}		3.5x – 65		215		194	ns
15	$\overline{RD}$ Fall→D0 to D15 Input	t_{RD}		2.0x – 60		100		103	ns
16	$\overline{RD}$ Low Pulse Width	t_{RR}	2.0x – 40		120		108		ns
17	$\overline{RD}$ Rise→D0 to D15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ Rise→A0 to A15 Output	t_{RAE}	x – 15		65		54		ns
19	WR Low Pulse Width	t_{WW}	2.0x – 40		120		108		ns
20	D0 to D15 Valid→ $\overline{WR}$ Rise	t_{DW}	2.0x – 55		105		68		ns
21	$\overline{WR}$ Rise→D0 to D15 Hold	t_{WD}	0.5x – 15		25		5		ns
22	A0 to A23 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWH}		3.5x – 90		190		199	ns
23	A0 to A15 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWL}		3.0x – 80		160		162	ns
24	RD/WR Fall→ $\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		160		148		ns
25	A0 to A23 Valid→PORT Input	t_{APH}		2.5x – 120		80		65	ns
26	A0 to A23 Valid→PORT Hold	t_{APH2}	2.5x + 50		250		235		ns
27	WR Rise→PORT Valid	t_{CP}		200		200		359	ns

AC Measuring Conditions

- Output Level: High 2.2 V/Low 0.8 V, CL=50 pF
  (However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CLK}$)
- Input Level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc/Low 0.2 Vcc (except for AD0 to AD15)

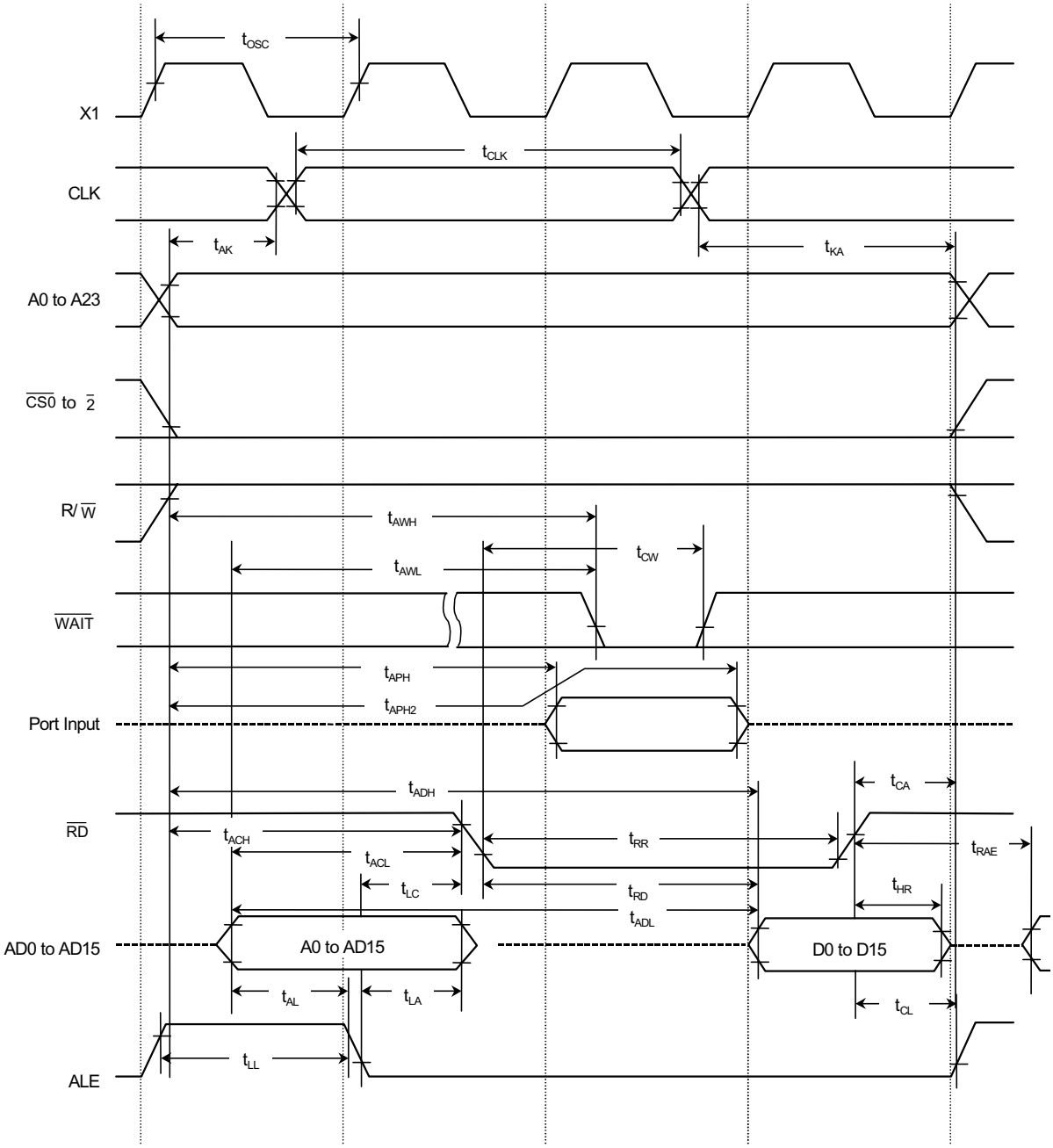
(2) Vcc = 2.2 V ± 10 %

No.	Parameter	Symbol	Variable		10 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (=x)	t_{OSC}	100	31250	100		ns
2	CLK width	t_{CLK}	2x – 40		160		ns
3	A0 to A23 Valid→CLK Hold	t_{AK}	0.5x – 30		20		ns
4	CLK Valid→A0 to A23 Hold	t_{KA}	1.5x – 80		70		ns
5	A0 to A15 Valid→ALE Fall	t_{AL}	0.5x – 35		15		ns
6	ALE Fall→A0 to A15 Hold	t_{LA}	0.5x – 35		15		ns
7	ALE High Width	t_{LL}	x – 60		40		ns
8	ALE Fall→ $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 35		15		ns
9	$\overline{RD}$ / $\overline{WR}$ Rise→ALE Rise	t_{CL}	0.5x – 40		10		ns
10	A0 to A15 Valid→ $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 50		50		ns
11	A0 to A23 Valid→ $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACH}	1.5x – 50		100		ns
12	$\overline{RD}$ / $\overline{WR}$ Rise→A0 to A23 Hold	t_{CA}	0.5x – 40		10		ns
13	A0 to A15 Valid→D0 to D15 Input	t_{ADL}		3.0x – 110		190	ns
14	A0 to A23 Valid→D0 to D15 Input	t_{ADH}		3.5x – 125		225	ns
15	$\overline{RD}$ Fall→D0 to D15 Input	t_{RD}		2.0x – 115		85	ns
16	$\overline{RD}$ Low Pulse Width	t_{RR}	2.0x – 40		160		ns
17	$\overline{RD}$ Rise→D0 to D15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$ Rise→A0 to A15 Output	t_{RAE}	x – 25		75		ns
19	$\overline{WR}$ Low Pulse Width	t_{WW}	2.0x – 40		160		ns
20	D0 to D15 Valid→ $\overline{WR}$ Rise	t_{DW}	2.0x – 120		80		ns
21	$\overline{WR}$ Rise→D0 to D15 Hold	t_{WD}	0.5x – 40		10		ns
22	A0 to A23 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWH}		3.5x – 130		220	ns
23	A0 to A15 Valid→ $\overline{WAIT}$ Input (1WAIT + n mode)	t_{AWL}		3.0x – 100		200	ns
24	$\overline{RD}$ / $\overline{WR}$ Fall→ $\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		200		ns
25	A0 to A23 Valid→PORT Input	t_{APH}		2.5x – 120		130	ns
26	A0 to A23 Valid→PORT Hold	t_{APH2}	2.5x + 50		200		ns
27	$\overline{WR}$ Rise→PORT Valid	t_{CP}		200		200	ns

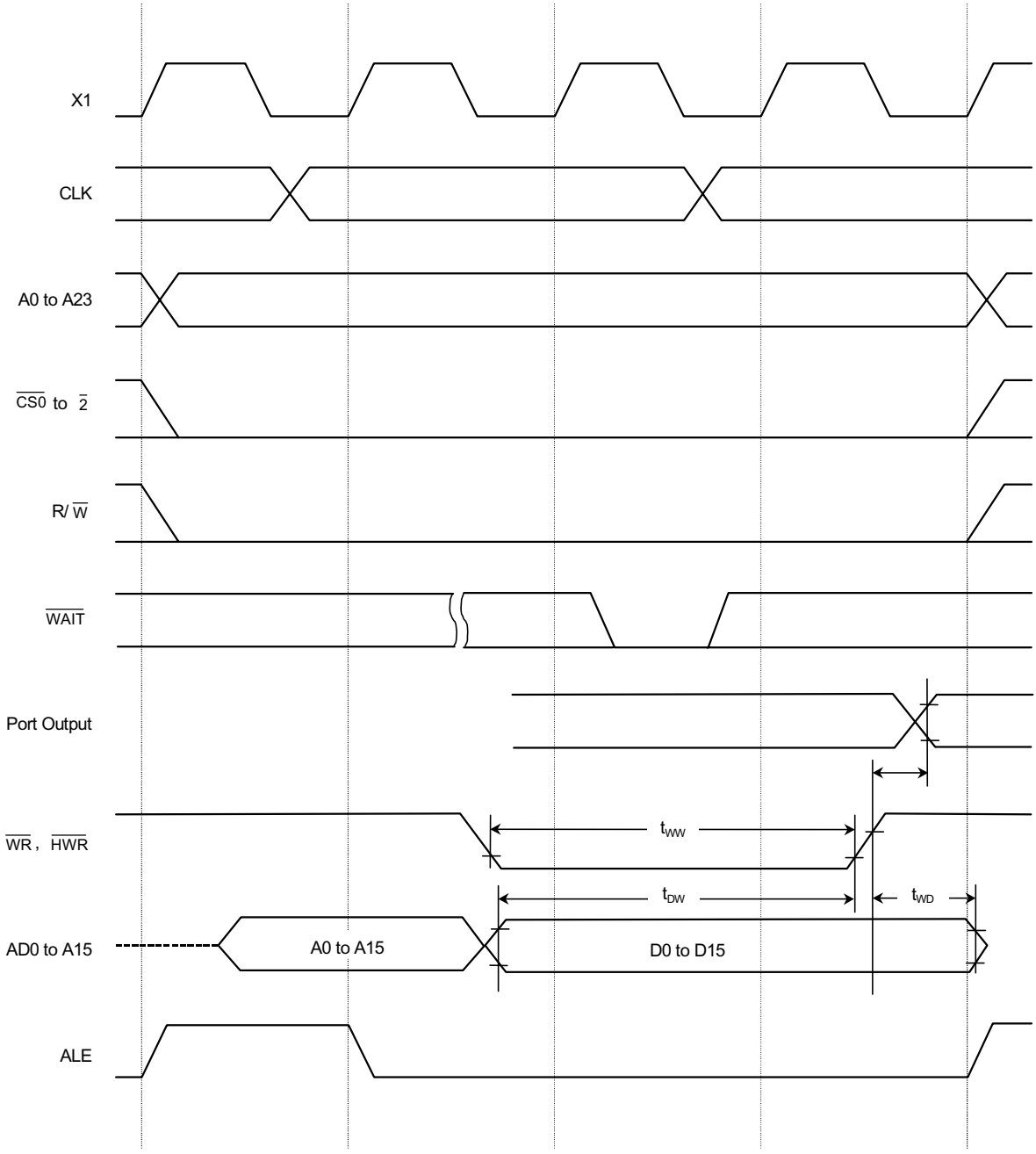
AC Measuring Conditions

- Output Level: High × 0.7 Vcc/Low 0.3 V × Vcc , CL = 50 pF
- Input Level: High × 0.9 Vcc/Low 0.1 V × Vcc

(3) Read Cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to A23
CS0 to 2
R/W
tAWH
tCW
tAWL
WAIT
tAPH
tAPH2
Port Input
tADH
tCA
RD
tACH
tRR
tRAE
tACL
tLC
tRD
tHR
tADL
AD0 to AD15
A0 to AD15
D0 to D15
tAL
tLA
tCL
tLL
ALE

(4) Write Cycle



4.4 A/D Conversion Characteristics

AVCC = VCC, AVSS = VSS

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	V_{REFH}	Vcc – 0.2 V	Vcc	Vcc	V
Analog Reference Voltage (–)	V_{REFL}	Vss	Vss	Vss + 0.2 V	
Analog Input Voltage Range	V_{AIN}	V_{REFL}		V_{REFH}	
Analog Current for Analog Reference Voltage Vcc = 3 V ± 10% <VREFON>=1	I_{REF} (V_{REFL} = 0 V)		0.5	1.5	mA
Vcc = 3 V ± 10% <VREFON>=0			0.02	5.0	μA
Error (not including quantizing errors)	—		± 1	± 3	LSB

Note 1: 1LSB = (V_{REFH} - V_{REFL}) / 2^{10} [V]

Note 2: The operation of the A/D converter is guaranteed only when fc (the high frequency oscillator) is used (it is not guaranteed when fs is used). It is guaranteed when $f_{FPH} \geq 4$ MHz.

Note 3: The value Icc includes the current which flows through the AVCC pin.

Note 4: The operation of the TMP91CU10 is guaranteed within 2.7 to 3.6 V.

4.5 Serial Channel Timing

(1) I/O Interface Mode

□ SCLK Input Mode

Parameter	Symbol	Variable		32.768 kHz Note)		13.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle	t_{SCY}	16x		488 μs		1.18		μs
Output Data → Rising Edge or Falling Edge* of SCLK	t_{OSS}	t_{SCY}/2–5x–50		91.5 μs		172		ns
SCLK Rising Edge or Falling Edge * →Output Data Hold	t_{OHS}	5x–100		152 μs		270		ns
SCLK Rising Edge or Falling Edge* →Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge or Falling Edge* →Effective Data Input	t_{SRD}		t_{SCY}–5x–100		336 μs		714	ns

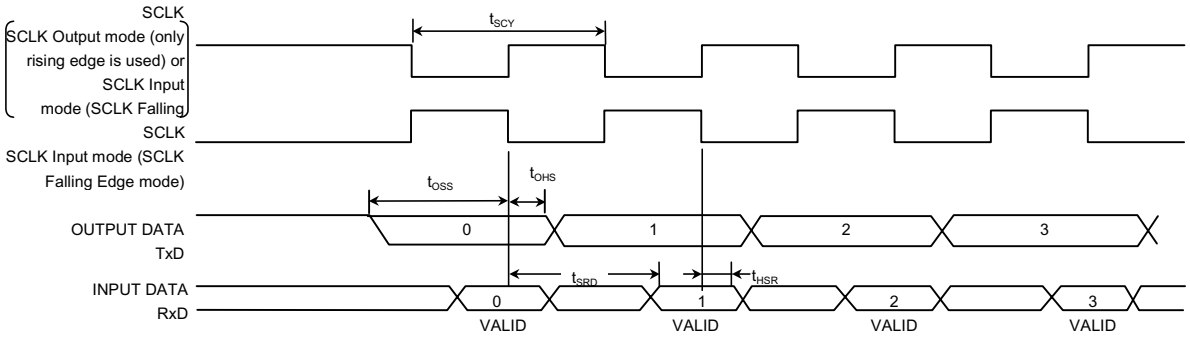
Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

*) The rising edge is used in SCLK Rising mode. The falling edge is used SCLK Falling mode.

□ SCLK Output mode

Parameter	Symbol	Variable		32.768 kHz Note)		13.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Cycle (Programmable)	t_{SCY}	16x	8192x	488 μs	250 ms	1.18	655.4	μs
Output Data → SCLK Rising Edge	t_{OSS}	t_{SCY}/2–5x–50		427 μs		886		ns
SCLK Rising Edge→ Output Data Hold	t_{OHS}	2x–80		60 μs		68		ns
SCLK Rising Edge→ Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge→ Effective Data Input	t_{SRD}		t_{SCY}–2x–150		428 μs		886	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.



4.6 Event Counter (TI0, TI4, TI8, TI9, TIA,TIB)

Parameter	Symbol	Variable		13.5 MHz		Unit
		Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		692		ns
Low Level Clock Pulse Width	t_{VCKL}	4X + 40		336		ns
High Level Clock Pulse Width	t_{VCKH}	4X + 40		336		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		13.5 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, INT0 to 4 Low Level Pulse Width	t_{INTAL}	4X		296		ns
$\overline{NMI}$, INT0 High Level Pulse Width	t_{INTAH}	4X		296		ns

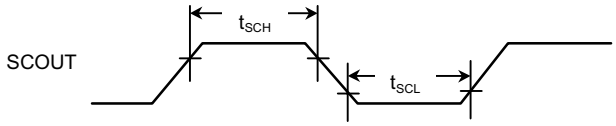
(2) INT5 to 8 interrupts, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

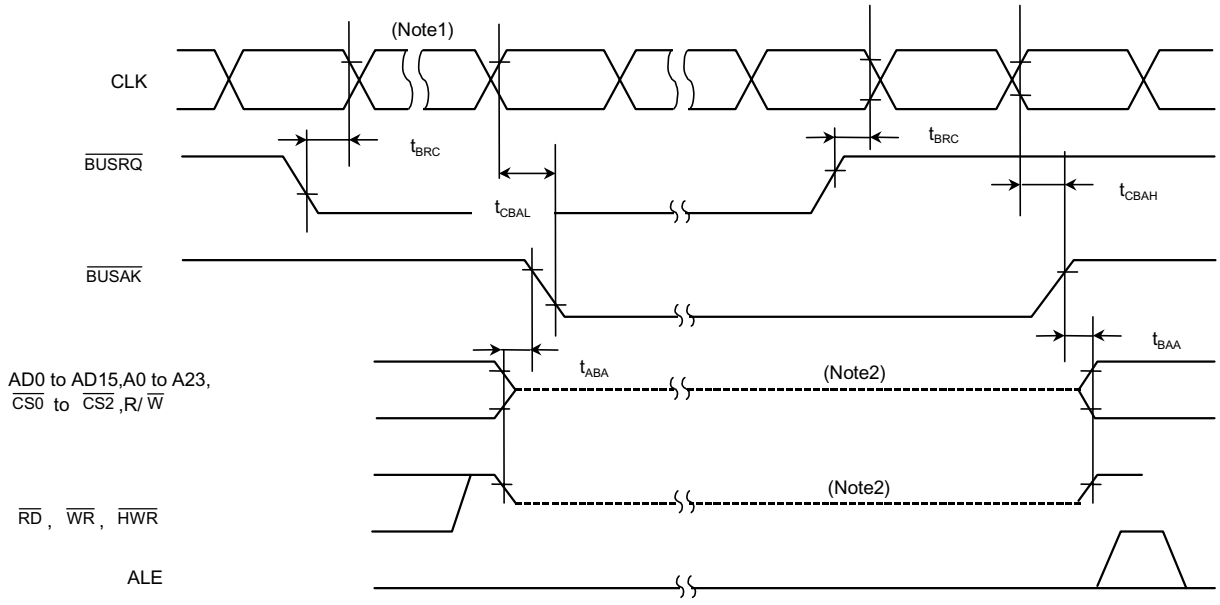
System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT5 to 8 low level pulse width)		t_{INTBH} (INT5 to 8 high level pulse width)		Unit
		Variable	13.5 MHz	Variable	13.5 MHz	
		Min	Min	Min	Min	
0(fc)	00 (f_{FPH})	8X + 100	692	8X + 100	692	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128X + 0.1	9.572	128X + 0.1	9.572	
1 (fs)(Note 2)	00 (f_{FPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

Note 1: XT represents the frequency of the low frequency clock fs. Calculated at fs = 32.768 kHz.

Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.



4.8 Timing Chart for Bus Request / Bus Acknowledge



Parameter	Symbol	Variable		13.5 MHz		Unit
		Min	Max	Min	Max	
BUSRQ BUSRQ Set−up Time to CLK	t_{BRC}	120		120		ns
CLK→BUSAK BUSAK Falling Edge	t_{CBAL}		1.5x + 120		231	ns
CLK→BUSAK Rising Edge	t_{CBAH}		0.5x + 40		77	ns
Output Buffer off to BUSAK	t_{ABA}	0	80	0	80	ns
BUSAK to Output Buffer on	t_{BAA}	0	80	0	80	ns

Note 1: Even if the BUSRQ signal goes low, the bus will not be released while the WAIT signal is low. The bus will only be released when BUSRQ goes low while WAIT is high.

Note 2: This line shows only that the output buffer is in the off state.It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary as fixing of the level is delayed.

The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.