Low Voltage / Low Power CMOS 16-bit Microcontrollers

TMP93CW44DF

1. Outline and Device Characteristics

The TMP93CW44 are high-speed, advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment.
The TMP93CW44DF are housed in 80-pin flat package (P-QFP80-1420-0.80B).
The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer / arithmetic instructions
- Micro DMA: 4 channels (1.6 μs per 2 bytes at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal RAM: 4 Kbytes

Internal ROM: 128 Kbytes

(4) External memory expansion

- Can be expanded up to 16-Mbytes (for both programs and data).
- AM8/$\overline{16}$ pin (select the external data bus width)
- Can mix 8- and 16-bit external data buses.
  (Dynamic bus sizing)

(5) 8-bit timer: 4 channels

(6) 16-bit timer: 2 channel

(7) Serial interface: 2 channels

(8) Serial bus interface: 1 channel

- I^2C bus mode
- Clocked-synchronous 8-bit serial interface mode

(9) 10-bit AD converter: 8 channels

(10) High current output: 8 ports

(11) Watchdog timer

(12) Bus width / wait controller: 3 blocks

(13) Interrupt functions: 33

- 9 CPU interrupts
- 17 internal interrupts
- 7 external interrupts

] 7-level priority can be set.

(14) I/O ports: 62 pins

(15) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)

(16) Clock gear function

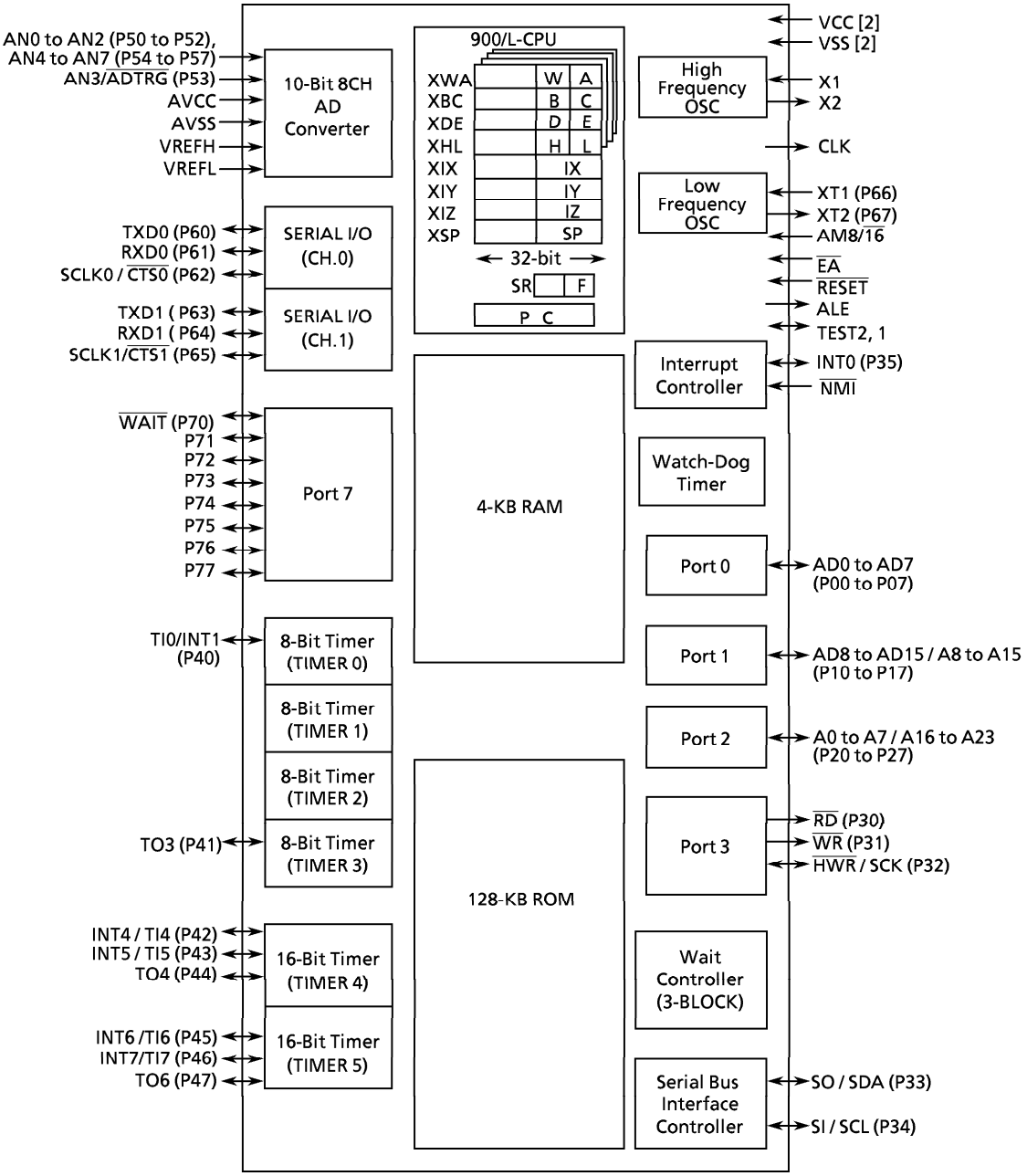
- High-frequency clock can be changed from fc to fc / 16.
- Dual clock Operation

(17) Wide Range of Operating Voltage

- Vcc = 2.7 to 5.5 V

(18) Package

- P-QFP80-1420-0.80B



Note: The items in parentheses ( ) are the initial setting after reset.

Figure 1.1 TMP93CW44 Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CW44, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CW44DF.

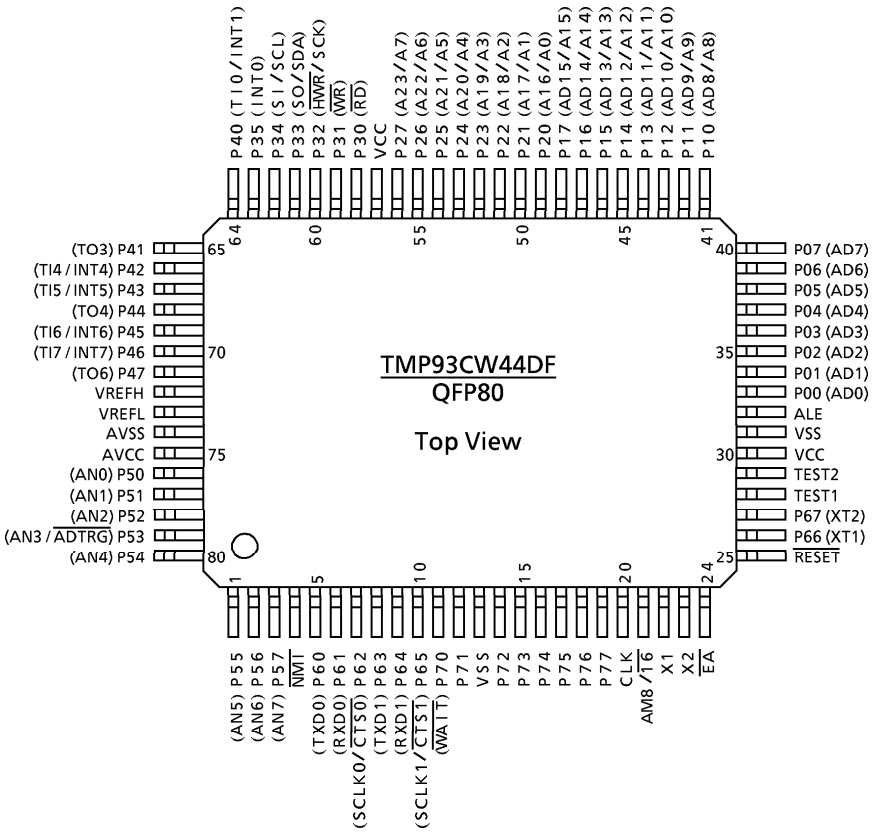


Figure 2.1.1 Pin Assignment (P-QFP80-1420-0.80B)

2.2 Pin Names and Functions

The names of input / output pins and their functions are described below.
Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Function (1/3)

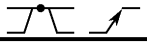
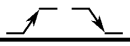
Pin name	Number of pins	I/O	Functions
P00 to P07 / AD0 to AD7	8	I/O	Port 0: I/O port that allows selection of I/O on a bit basis
		3-state	Address/data (lower): Bits 0 to 7 for address/data bus
P10 to P17 / AD8 to AD15 / A8 to A15	8	I/O	Port 1: I/O port that allows selection of I/O on a bit basis
		3-state	Address/data (upper): Bits 8 to 15 for address/data bus
		Output	Address: Bits 8 to 15 for address bus
P20 to P27 / A0 to A7 / A16 to A23	8	I/O	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)
		Output	Address: Bits 0 to 7 for address bus
		Output	Address: Bits 16 to 23 for address bus
P30 / $\overline{RD}$	1	Output	Port 30: Output port
		Output	Read: Strobe signal for reading external memory
P31 / $\overline{WR}$	1	Output	Port 31: Output port
		Output	Write: Strobe signal for writing data on pins AD0 to 7
P32 / $\overline{HWR}$ / SCK	1	I/O	Port 32: I/O port (with pull-up resistor)
		Output	High write: Strobe signal for writing data on pins AD8 to 15
		I/O	Mode clock SBI SIO mode clock
P33 / SO / SDA	1	I/O	Port 33: I/O port
		Output	Serial Send Data
		I/O	SBI I^2C bus mode channel data
P34 / SI / SCL	1	I/O	Port 34: I/O port
		Input	Serial Receive Data
		I/O	SBI I^2C bus mode clock
P35 / INT0	1	I/O	Port 35: I/O port
		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge 
P40 / TI0 / INT1	1	I/O	Port 40: I/O port
		Input	Timer input 0: Timer 0 input
		Input	Interrupt request pin 1: Interrupt request pin with rising edge
P41 / TO3	1	I/O	Port 41: I/O port
		Output	Timer output 3: 8-bit Timer 3 output
P42 / TI4 / INT4	1	I/O	Port 42: I/O port
		Input	Timer input 4: Timer 4 input
		Input	Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge 
P43 / TI5 / INT5	1	I/O	Port 43: I/O port
		Input	Timer input 5: Timer 4 input
		Input	Interrupt request pin 5: Interrupt request pin with rising edge
P44 / TO4	1	I/O	Port 44: I/O port
		Output	Timer output 4: Timer 4 output

Table 2.2.1 Pin Names and Function (2/3)

Pin name	Number of pins	I/O	Functions
P45 / TI6 / INT6	1	I/O	Port 45: I/O port
		Input	Timer input 6: Timer 5 input
		Input	Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P46 / TI7 / INT7	1	I/O	Port 46: I/O port
		Input	Timer input 7: Timer 5 input
		Input	Interrupt request pin 7: Interrupt request pin with rising edge
P47 / TO6	1	I/O	Port 47: I/O port
		Output	Timer output 6: Timer 5 output pin
P50 to P52, P54 to P57 / AN0 to AN2, AN4 to AN7	7	Input	Port 50 to Port 52, Port 54 to Port 57: Input port
		Input	Analog input: Analog signal input for AD converter
P53 / AN3 / $\overline{\text{ADTRG}}$	1	Input	Port53: Input Port
		Input	Analog input: Analog signal input for AD converter
		Input	AD converter external start trigger input
P60 / TXD0	1	I/O	Port 60: I/O port (with pull-up resistor)
		Output	Serial send data 0
P61 / RXD0	1	I/O	Port 61: I/O port (with pull-up resistor)
		Input	Serial receive data 0
P62 / $\overline{\text{CTS0}}$ / SCLK0	1	I/O	Port 62: I/O port (with pull-up resistor)
		Input	Serial data send enable 0 (Clear to Send)
		I/O	Serial Clock I/O 0
P63 / TXD1	1	I/O	Port 63: I/O port (with pull-up resistor)
		Output	Serial send data 1
P64 / RXD1	1	I/O	Port 64: I/O port (with pull-up resistor)
		Input	Serial receive data 1
P65 / $\overline{\text{CTS1}}$ / SCLK1	1	I/O	Port 65: I/O port (with pull-up resistor)
		Input	Serial data send enable 1 (Clear to Send)
		I/O	Serial clock I/O 1
P70 / $\overline{\text{WAIT}}$	1	I/O	Port 70: I/O port (High current output available)
		Input	WAIT: Pin used to request CPU bus wait (It is active in 1 WAIT + N mode. Set by the Bus-width/wait control register.)
P71 to P77	7	I/O	Port 71 to Port 77: I/O port (High current output available)
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program.
CLK	1	Output	Clock output: Outputs "$f_{SYS} \div 2$" Clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	External access: "1" should be inputted with TMP93CW44.

Table 2.2.1 Pin Names and Function (3/3)

Pin name	Number of pins	I/O	Functions
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. "1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register.
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP93CW44. (With pull-up resistor)
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1	1	Input	High Frequency Oscillator connecting pin
X2	1	Output	High Frequency Oscillator connecting pin
P66	1	I/O	Port 66: I/O port (Open Drain Output)
/ XT1		Input	Low Frequency Oscillator connecting pin
P67	1	I/O	Port 67: I/O port (Open Drain Output)
/ XT2		Output	Low Frequency Oscillator connecting pin
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.
VCC	2		Power supply pin (All VCC pins should be connected with GND (0 V).)
VSS	2		GND pin (0 V) (All VSS pins should be connected with GND (0 V).)

Note: Built-in Pull-up resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

3. Operation

This section describes the functions and basic operational blocks of TMP93CW44 devices.

3.1 CPU

TMP93CW44 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous section)

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CW44.

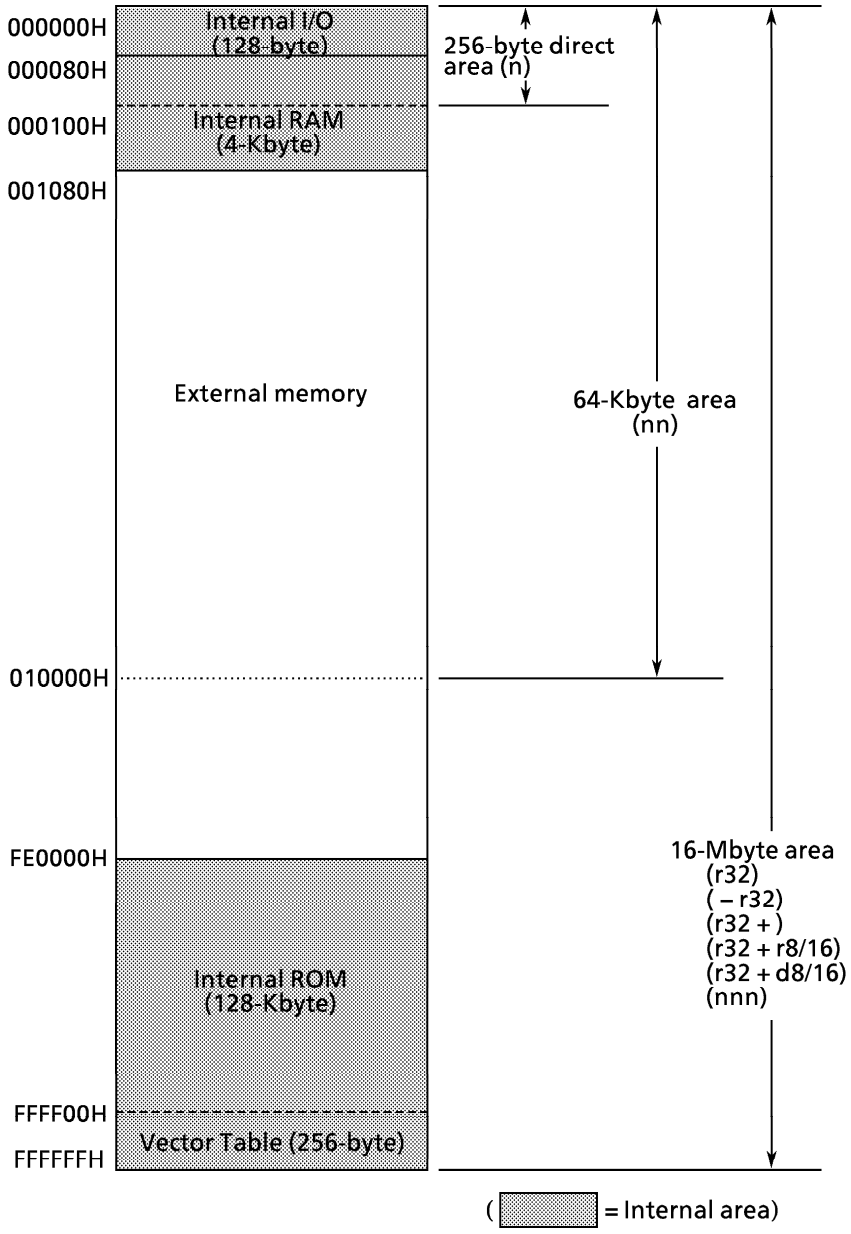


Figure 3.2.1 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP93CW44DF)

"X" used in an expression shows a cycle of clock f_{FPH} selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = "0000").

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	− 0.5 to 6.5	V
Input Voltage	V_{IN}	− 0.5 to Vcc + 0.5	V
Output current (Per 1 pin) P7	I_{OL1}	20	mA
Output current (Per 1 pin) except P7	I_{OL2}	2	mA
Output Current (P7 total)	ΣI_{OL1}	80	mA
Output Current (total)	ΣI_{OL}	120	mA
Output Current (total)	ΣI_{OH}	− 80	mA
Power Dissipation (Ta = 85℃)	P_D	350	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	℃
Storage Temperature	T_{STG}	− 65 to 150	℃
Operating Temperature	T_{OPR}	− 40 to 85	℃

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = − 40 to 85°C

Parameter		Symbol	Condition		Min	Typ. (Note)	Max	Unit
Power Supply Voltage		Vcc	fc = 4 to 20 MHz	fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz		2.7			
Input Low Voltage	AD0 to 15	V_{IL}	Vcc ≧ 4.5 V		− 0.3		0.8	V
			Vcc < 4.5 V				0.6	
	Port2 to 7 (except P35)	V_{IL1}	Vcc = 2.7 to 5.5 V				0.3 Vcc	
	RESET, NMI, INT0	V_{IL2}					0.25 Vcc	
	EA, AM8/16	V_{IL3}					0.3	
	X1	V_{IL4}					0.2 Vcc	
Input High Voltage	AD0 to 15	V_{IH}	Vcc ≧ 4.5 V		2.2		Vcc + 0.3	
			Vcc < 4.5 V		2.0			
	Port2 to 7 (except P35)	V_{IH1}	Vcc = 2.7 to 5.5 V		0.7 Vcc			
	RESET, NMI, INT0	V_{IH2}			0.75 Vcc			
	EA, AM8/16	V_{IH3}			Vcc − 0.3			
	X1	V_{IH4}			0.8 Vcc			
Output Low Voltage		V_{OL}	I_{OL} = 1.6 mA (Vcc = 2.7 to 5.5 V)				0.45	V
Output Low current (P7)		I_{OL7}	V_{OL} = 1.0V	(Vcc = 5 V ± 10%)	16			mA
				(Vcc = 3 V ± 10%)	7			
Output High Voltage		V_{OH1}	I_{OH} = − 400 μA (Vcc = 3 V ± 10%)		2.4			V
		V_{OH2}	I_{OH} = − 400 μA (Vcc = 5 V ± 10%)		4.2			V

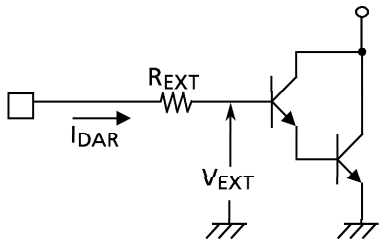
Note: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ.(Note1)	Max	Unit
Darlington Drive Current (8 Output Pins Max)	I_{DAR} (Note2)	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ (Vcc = 5 V ± 10% only)		−1.0		−3.5	mA
Input Leakage Current	I_{LI}	0.0 ≦ V_{IN} ≦ V_{CC}			0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≦ V_{IN} ≦ V_{CC} − 0.2			0.05	±10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc		2.0		6.0	V
$\overline{RESET}$ Pull Up Resistance	R_{RST}	Vcc = 5.5 V		45		130	kΩ
		Vcc = 4.5 V		50		160	
		Vcc = 3.3 V		70		280	
		Vcc = 2.7 V		90		400	
Pin Capacitance	C_{IO}	fc = 1 MHz				10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}			0.4	1.0		V
Programmable Pull Up Resistance	R_{KH}	Vcc = 5.5 V		45		130	kΩ
		Vcc = 4.5 V		50		160	
		Vcc = 3.3 V		70		280	
		Vcc = 2.7 V		90		400	
NORMAL (Note3)	Icc	Vcc = 5 V ± 10% fc = 20 MHz			21	28	mA
RUN					17	25	
IDLE2					12.5	17	
IDLE1					2.5	4	
NORMAL (Note3)		Vcc = 3 V ± 10% fc = 12.5 MHz (Typ.: Vcc = 3.0 V)			7	10	
RUN					5.5	9	
IDLE2					4.5	6	
IDLE1					0.7	1	
SLOW (Note3)		Vcc = 3 V ± 10% fs = 32.768 kHz (Typ.: Vcc = 3.0 V)			20	35	μA
RUN					16	30	
IDLE2					11	25	
IDLE1					4	15	
STOP		Ta ≦ 50°C	Vcc = 2.7 V to 5.5 V		0.2	10	μA
		Ta ≦ 70°C				20	
		Ta ≦ 85°C				50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.
Note 2: I_{DAR} is guranteed for total of up to 8 ports.
Note 3: I_{CC} measurement conditions (NORMAL, SLOW).
Only CPU is operational; output pins are open and input pins are fixed.

(Reference) Definition of I_{DAR}



4.3 AC Characteristics

(1) Vcc = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= X)	t_{OSC}	50	31250	62.5		50		ns
2	CLK pulse width	t_{CLK}	2X – 40		85		60		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5X – 20		11		5		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5X – 70		24		5		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5X – 15		16		10		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5X – 20		11		5		ns
7	ALE High pulse width	t_{LL}	X – 40		23		10		ns
8	ALE fall→ $\overline{RD}$/$\overline{WR}$ fall	t_{LC}	0.5X – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ rise→ ALE rise	t_{CL}	0.5X – 20		11		5		ns
10	A0 to 15 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACL}	X – 25		38		25		ns
11	A0 to 23 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACH}	1.5X – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5X – 25		6		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0X – 55		133		95	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5X – 65		154		110	ns
15	$\overline{RD}$fall →D0 to 15 input	t_{RD}		2.0X – 60		65		40	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0X – 40		85		60		ns
17	$\overline{RD}$rise→ D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$rise→ A0 to 15output	t_{RAE}	X – 15		48		35		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0X – 40		85		60		ns
20	D0 to 15 Valid→ $\overline{WR}$ rise	t_{DW}	2.0X – 55		70		45		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5X – 15		16		10		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+\ n\ mode})$	t_{AWH}		3.5X – 90		129		85	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+\ n\ mode})$	t_{AWL}		3.0X – 80		108		70	ns
24	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ Hold $(^{1\ WAIT}_{+\ n\ mode})$	t_{CW}	2.0X + 0		125		100		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5X – 120		36		5	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5X + 50		206		175		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200		200	ns

AC Measuring Conditions

- Output Level: High 2.2 V / Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 × Vcc / Low 0.2 × Vcc (Except for AD0 to AD15)

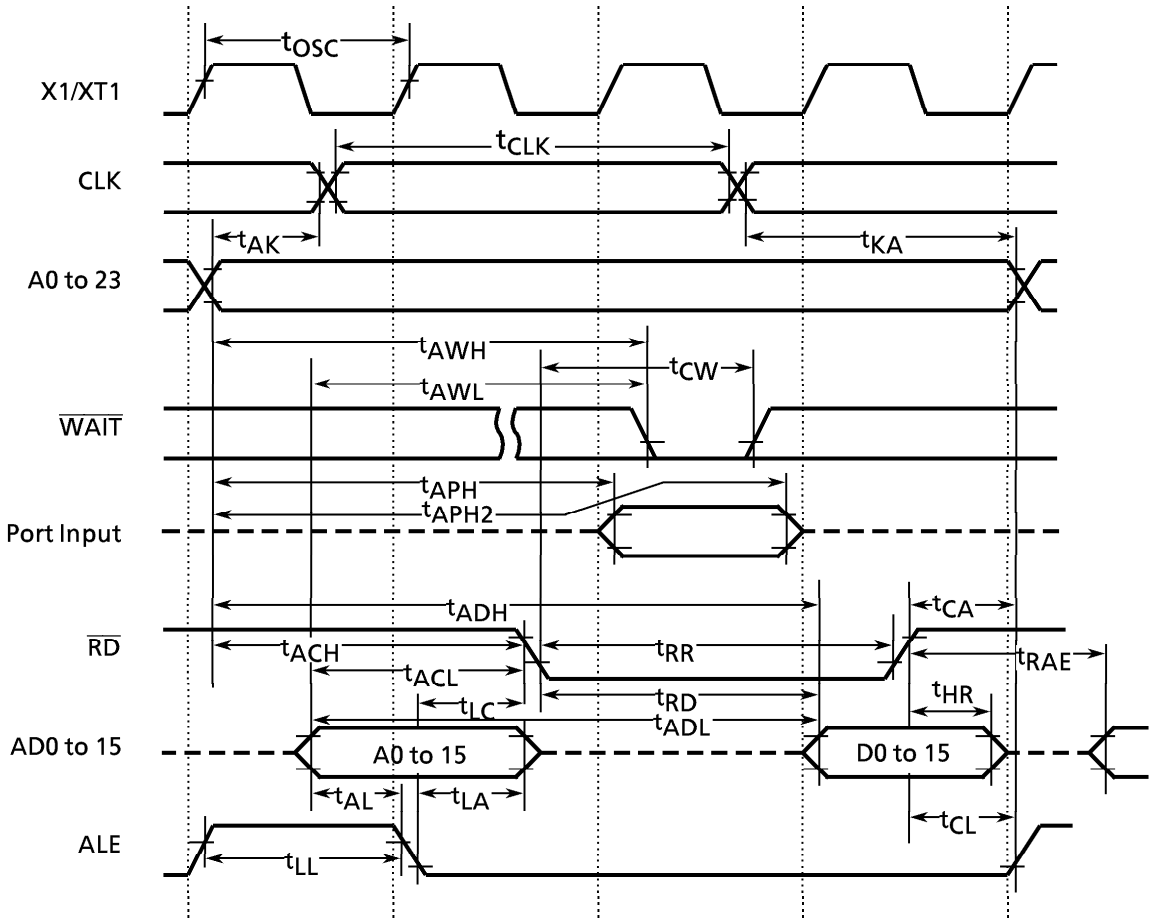
(2) Vcc = 3 V ± 10%

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (= X)	t_{OSC}	80	31250	80		ns
2	CLK pulse width	t_{CLK}	2X – 40		120		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5X – 30		10		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5X – 80		40		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5X – 35		5		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5X – 35		5		ns
7	ALE High pulse width	t_{LL}	X – 60		20		ns
8	ALE fall→ $\overline{RD}/\overline{WR}$ fall	t_{LC}	0.5X – 35		5		ns
9	$\overline{RD}/\overline{WR}$ rise→ ALE rise	t_{CL}	0.5X – 40		0		ns
10	A0 to 15 Valid→ $\overline{RD}/\overline{WR}$ fall	t_{ACL}	X – 50		30		ns
11	A0 to 23 Valid→ $\overline{RD}/\overline{WR}$ fall	t_{ACH}	1.5X – 50		70		ns
12	$\overline{RD}/\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5X – 40		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0X – 110		130	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5X – 125		155	ns
15	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.0X – 115		45	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0X – 40		120		ns
17	$\overline{RD}$rise→ D0 to 15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$rise→ A0 to 15output	t_{RAE}	X – 25		55		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0X – 40		120		ns
20	D0 to 15 Valid→ $\overline{WR}$rise	t_{DW}	2.0X – 120		40		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5X – 40		0		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+\ n\ mode})$	t_{AWH}		3.5X – 130		150	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input $(^{1\ WAIT}_{+\ n\ mode})$	t_{AWL}		3.0X – 100		140	ns
24	$\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold $(^{1\ WAIT}_{+\ n\ mode})$	t_{CW}	2.0X + 0		160		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5X – 195		5	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5X + 50		250		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200	ns

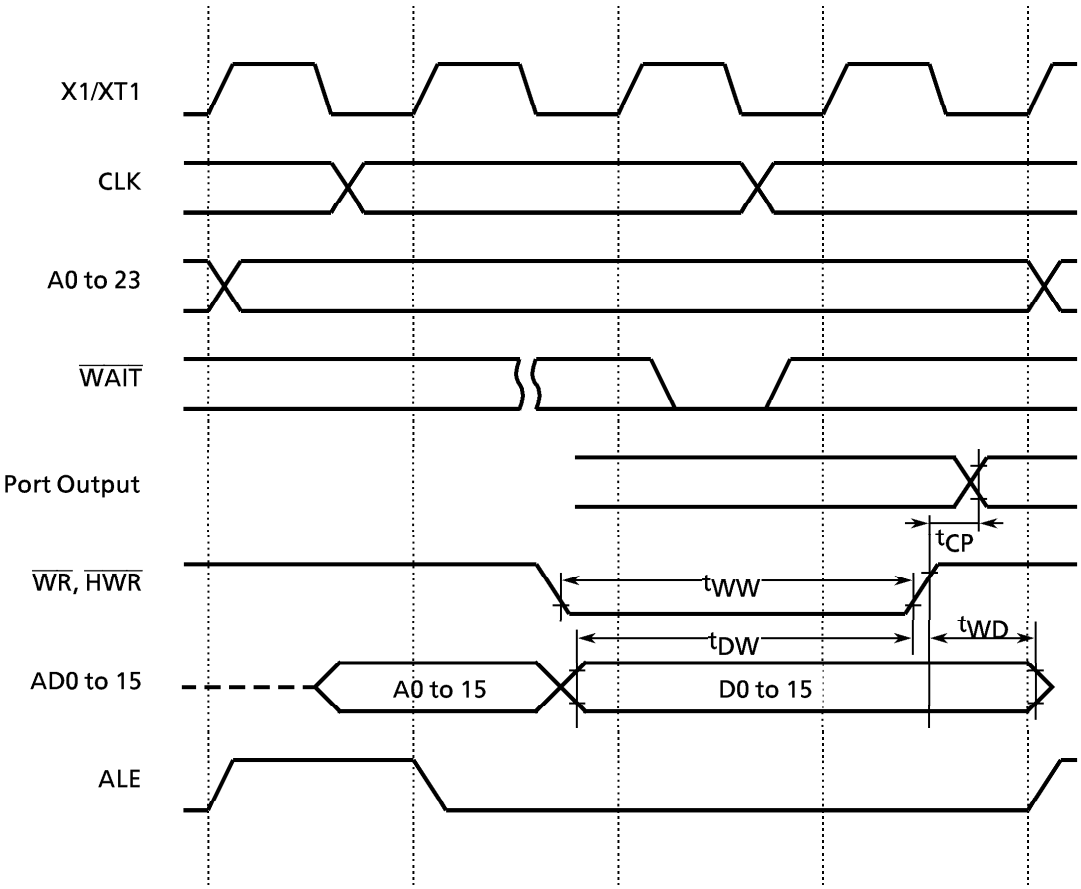
AC Measuring Conditions

- Output Level: High 0.7 × V_{CC} / Low 0.3 × V_{CC}, CL = 50 pF
- Input Level: High 0.9 × V_{CC} / Low 0.1 × V_{CC}

(3) Read Cycle


X1/XT1
CLK
A0 to 23
WAIT
Port Input
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tLC
tRD
tADL
tHR
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(4) Write Cycle



4.4 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		488 μs		1.28		0.8		μs
Output Data → falling edge of SCLK	t_{OSS}	$t_{SCY}/2 - 5X - 50$		91.5 μs		190		100		ns
SCLK rising / falling edge → Output Data hold	t_{OHS}	5X – 100		152 μs		300		150		ns
SCLK rising / falling edge → Input Data hold	t_{HSR}	0		0		0		0		ns
SCLK rising / falling edge → effective data input	t_{SRD}		$t_{SCY} - 5X - 100$		336 μs		780		450	ns

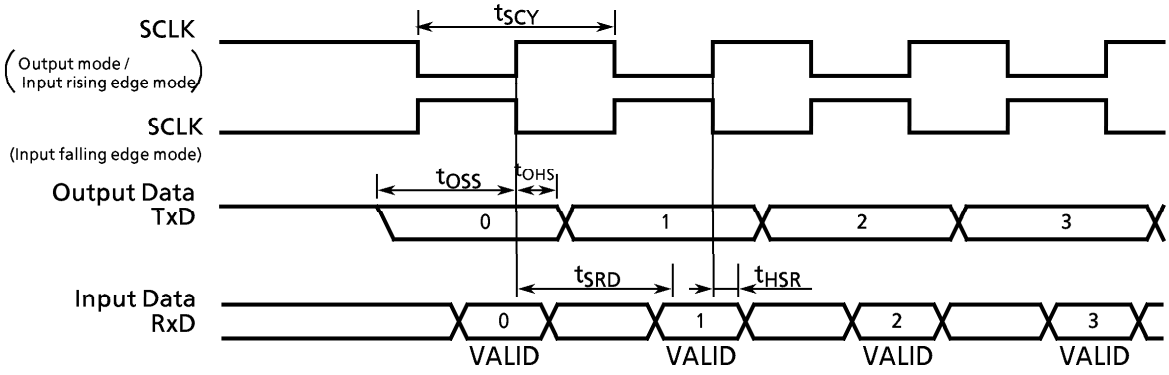
Note 1: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

Note 2: SCLK rising/falling timing; SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
Output Data → SCLK rising edge	t_{OSS}	$t_{SCY} - 2X - 150$		427 μs		970		550		ns
SCLK rising edge → Output Data hold	t_{OHS}	2X – 80		60 μs		80		20		ns
SCLK rising edge → Input Data hold	t_{HSR}	0		0		0		0		ns
SCLK rising edge → effective Data input	t_{SRD}		$t_{SCY} - 2X - 150$		428 μs		970		550	ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.



(2) UART Mode (SCLK0, 1 are external input)

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4X + 20		122 μs		340		220		ns
SCLK Low level pulse width	t_{SCYL}	2X + 5		6 μs		165		105		ns
SCLK High level pulse width	t_{SCYH}	2X + 5		6 μs		165		105		ns

Note: When fs is used as system clock or fs divided by 4 is used as input clock to prescaler.

4.5 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Power Supply	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	V_{CC} = 5 V ± 10%	V_{CC} – 0.2 V	V_{CC}	V_{CC}	V
		V_{CC} = 3 V ± 10%	V_{CC} – 0.2 V	V_{CC}	V_{CC}	
Analog reference voltage (–)	VREFL	V_{CC} = 5 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
		V_{CC} = 3 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)	V_{CC} = 5 V ± 10%		0.5	1.5	mA
		V_{CC} = 3 V ± 10%		0.3	0.9	
<VREFON> = 0		V_{CC} = 2.7 to 5.5 V		0.02	5.0	μA
Error (except quantization errors)	–	V_{CC} = 5 V ± 10%		± 1.0	± 3.0	LSB
		V_{CC} = 3 V ± 10%		± 1.0	± 5.0	

Note 1: $1LSB = (V_{REFH} - V_{REFL}) / 2^{10}$ [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.6 Event Counter Input Clock (external input clock: TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		740		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		360		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture Operation

(1) $\overline{NMI}$, INT0 Interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level Pulse width	t_{INTAL}	4X		320		200		ns
$\overline{NMI}$, INT0 High level Pulse width	t_{INTAH}	4X		320		200		ns

(2) INT1, 4 to 7 Interrupts and Capture

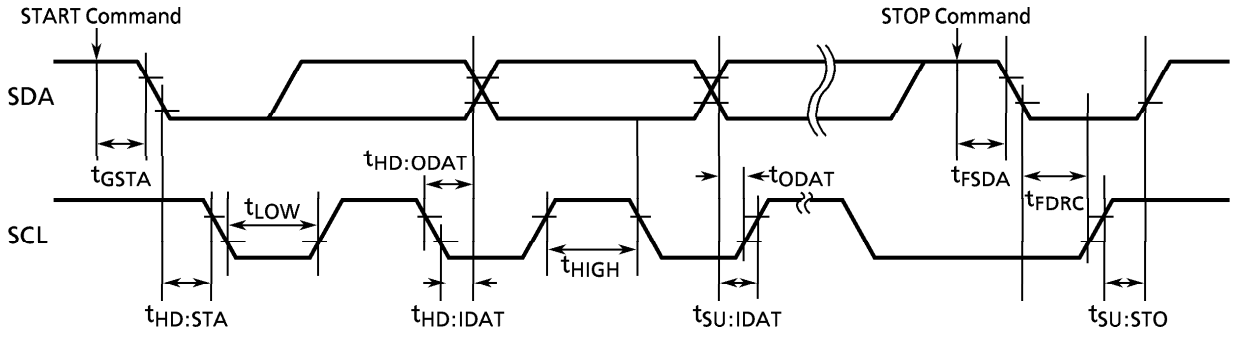
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT1, INT4 to INT7 Low level Pulse width	t_{INTBL}	4X + 100		420		300		ns
INT1, INT4 to INT7 High level Pulse width	t_{INTBH}	4X + 100		420		300		ns

4.8 Serial Bus Interface Timing

(1) I²C bus Mode

Parameter	Symbol	Variable			Unit
		Min	Typ.	Max	
START command → SDA fall	t_{GSTA}	3X			s
Hold time START condition	$t_{HD:STA}$	2^nX			s
SCL Low level pulse width	t_{LOW}	2^nX			s
SCL High level pulse width	t_{HIGH}	2^nX + 12X			s
Data hold time (input)	$t_{HD:IDAT}$	0			ns
Data set-up time (input)	$t_{SU:IDAT}$	250			ns
Data hold time (output)	$t_{HD:ODAT}$	7X		11X	s
Data output → SCL Rising edge	t_{ODAT}		2^nX – $t_{HD:ODAT}$		s
STOP command → SDA fall	t_{FSDA}	3X			s
SDA Falling edge → SCL Rising edge	t_{FDRC}	2^nX			s
Set-up time STOP condition	$t_{SU:STO}$	2^nX + 16X			s

Note: "n" value is set by SBICR1 <SCK2 to 0>



(2) Clocked-synchronous 8-bit SIO Mode

① SCK Input Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling edge→ Output data hold	t_{OHS2}	6X		s
Output data → SCK rising edge	t_{OSS2}	t_{SCY2} – 6X		s
SCK rising edge→ Input data hold	t_{HSR2}	6X		ns
Input data→ SCK rising edge	t_{ISS2}	0		ns

② SCK Output Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling edge → Output data hold	t_{OHS2}	2X		s
Output data→ SCK rising edge	t_{OSS2}	t_{SCY2} – 2X		s
SCK rising edge→ Input data hold	t_{HSR2}	2X		s
Input data→ SCK rising edge	t_{ISS2}	0		ns