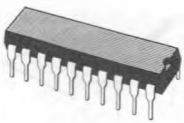
SGS-THOMSON MICROELECTRONICS

TS5070
TS5071

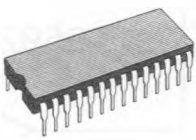
PROGRAMMABLE CODEC/FILTER COMBO 2ND GENERATION

- COMPLETE CODEC AND FILTER SYSTEM INCLUDING :
  - TRANSMIT AND RECEIVE PCM CHANNEL FILTERS
  - μ-LAW OR A-LAW COMPANDING CODER AND DECODER
  - RECEIVE POWER AMPLIFIER DRIVES 300 Ω
  - 4.096 MHz SERIAL PCM DATA (max)
- PROGRAMMABLE FUNCTIONS :
  - TRANSMIT GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - RECEIVE GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - HYBRID BALANCE CANCELLATION FILTER
  - TIME-SLOT ASSIGNMENT : UP to 64 SLOTS/FRAME
  - 2 PORT ASSIGNMENT (TS5070)
  - 6 INTERFACE LATCHES (TS5070)
  - A or μ-LAW
  - ANALOG LOOPBACK
  - DIGITAL LOOPBACK
- DIRECT INTERFACE TO SOLID-STATE SLICs
- SIMPLIFIES TRANSFORMER SLIC, SINGLE WINDING SECONDARY
- STANDARD SERIAL CONTROL INTERFACE
- 70 mW OPERATING POWER (typ)
- 2 mW STANDBY POWER (typ)
- MEETS OR EXCEEDS ALL CCITT AND LSSGR SPECIFICATIONS
- TTL AND CMOS COMPATIBLE DIGITAL INTERFACES
- SECOND SOURCE OF TP3070, TP3071/COMBO II ®



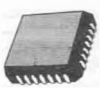
DIP20
(Plastic and Ceramic)

ORDER CODE : TS5071N
TS5071J



DIP28L
(Ceramic)

ORDER CODE : TS5070J



PLCC28

ORDER CODE : TS5070FN

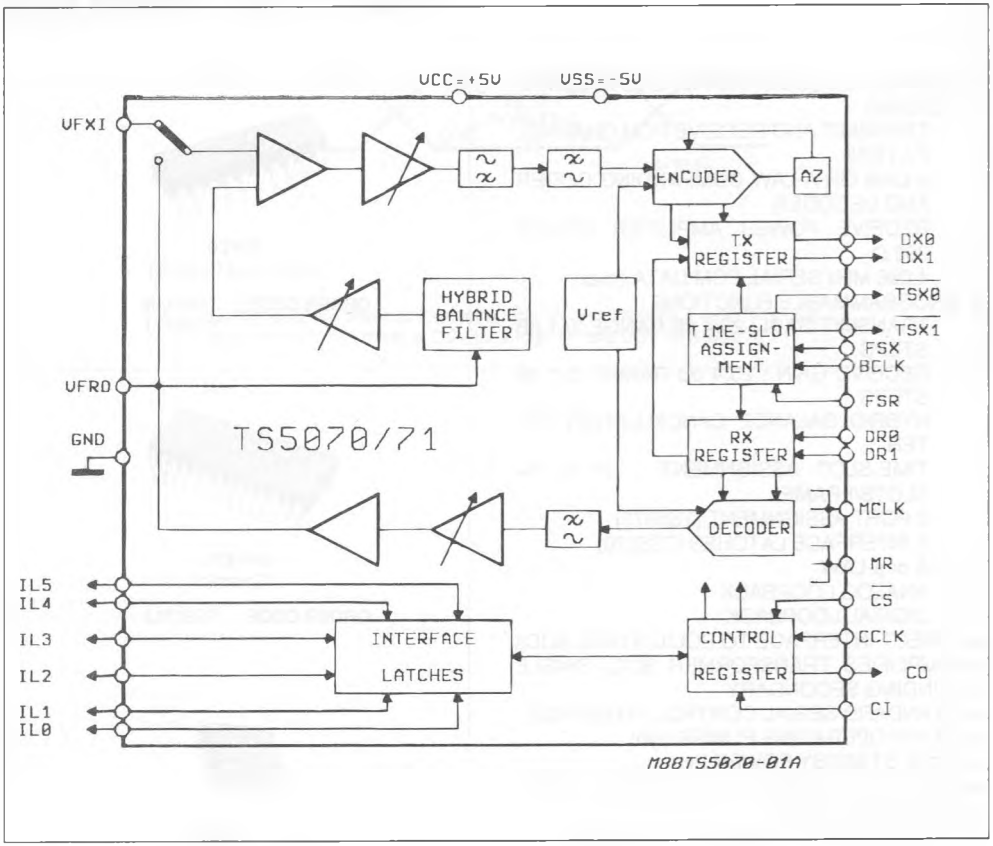
DESCRIPTION

The TS5070 series are second generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards. Using advanced switched capacitor techniques the TS5070 and TS5071 combine transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO IIG to interface to the SLIC control leads, a number of programmable latches are included ; each may be configured as either an input or an output. The TS5070 provides 6 latches and the TS5071 5 latches.

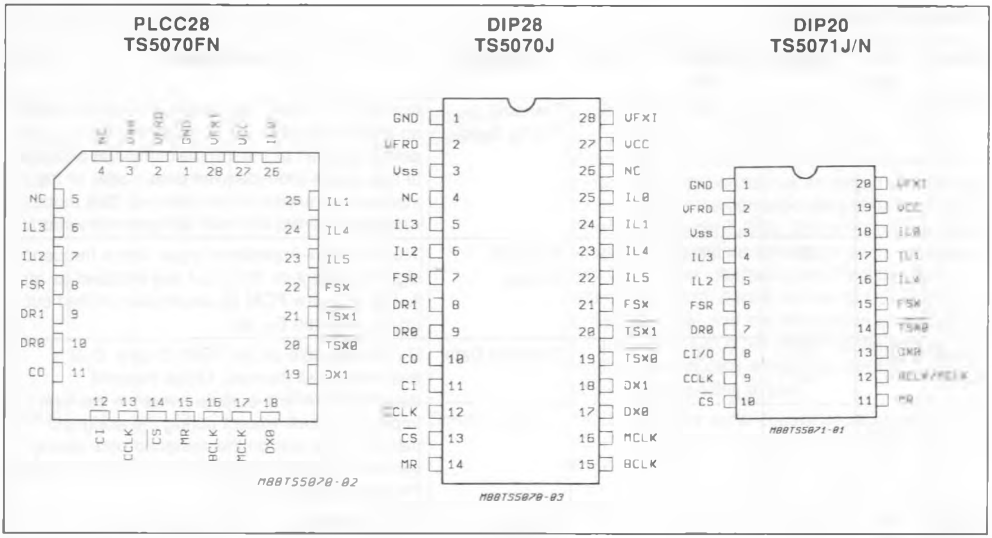
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	7	V
V_{SS}	V_{SS} to GND	– 7	V
	Voltage at VFXI	V_{CC} + 0.5 to V_{SS} – 0.5	V
V_{IN}	Voltage at Any Digital Input	V_{CC} + 0.5 to GND – 0.5	V
	Current at VFRO	± 100	mA
I_O	Current at Any Digital Output	± 50	mA
T_{stg}	Storage Temperature Range	– 65, + 150	°C
T_{lead}	Lead Temperature Range (soldering, 10 seconds)	300	°C

PIN CONNECTIONS



PIN DESCRIPTION

POWER SUPPLY, CLOCK

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
V_{CC}	S	27	27	19	Positive Power Supply	+ 5 V ± 5 %
V_{SS}	S	3	3	3	Negative Power Supply	− 5 V ± 5 %
GND	S	1	1	1	Ground	All analog and digital signals are referenced to this pin.
BCLK	I	15	16	12	Bit Clock	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	I	16	17	12	Master Clock	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1. 536/1. 544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK. BCLK and MCLK are wired together in the TS5071.

PIN DESCRIPTION (continued)

TRANSMIT SECTION

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
FS_X	I	21	22	15	Transmit Frame Sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time-slot assigned to this device (non–delayed data mode) or the start of the transmit frame (delayed data mode using the internal time–slot assigment counter).
VF_XI	I	28	28	20	Transmit Analog	This is a high–impedance input. Voice frequency signals present on this input are encoded as an A–law or μ–law PCM bit stream and shifted out on the selected D_X pin.
D_X0 D_X1	0 0	17 18	18 19	13 –	Transmit Data	D_X1 is available on the TS5070 only, D_X0 is available on all devices. These transmit data TRI–STATE® outputs remain in the high impedance state except during the assigned transmit time–slot on the assigned port, during wich the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS_X0}$ $\overline{TS_X1}$	0 0	19 20	20 21	14 –	Transmit Time–slot	$\overline{TS_X1}$ is available on the TS5070 only. $\overline{TS_X0}$ is available on all devices. Normally these opendrain outputs are floating in a high impedance state except when a time–slot is active on one of the D_X outputs, when the apppropriate $\overline{TS_X}$ output pulls low to enable a backplane line–driver. Should be strapped to ground (GND) when not used.

RECEIVE SECTION

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
FS_R	I	7	8	6	Receive Frame Sync.	Normally a pulse or squrewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time–slot assigned to this device (non-delayed frame mode) or the start of the receive frame (delayed frame mode using the internal time–slot assignment counter).
VF_R0	0	2	2	2	Receive Analog	The receive analog power amplifier output, capable of driving load impedances as low as 300 Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_R0 D_R1	I I	9 8	10 9	7 –	Receive Data	D_R1 is available on the TS5070 only, D_R0 is available on all devices. These receive data input(s) are inactive except during the assigned receive time–slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.

PIN DESCRIPTION (continued)

INTERFACE, CONTROL, RESET

Name	Pin Type	TS5070 J	TS5070 FN	TS5071	Function	Description
IL5 IL4 IL3 IL2 IL1 IL0	I/O I/O I/O I/O I/O I/O	22 23 5 6 24 25	23 24 6 7 25 26	– 16 4 5 17 18	Interface Latches	IL5 through IL0 are available on the TS5070, IL4 through IL0 are available on the TS5071. Each interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR) . For pins configured as inputs, the logic state sensed on each input is latched into the interface Latch Register (ILR) whenever control data is written to COMBO IIG, while $\overline{CS}$ is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
CCLK	I	12	13	9	Control Clock	This clock shifts serial control information into or out of CI or CO (or CI/O) when the $\overline{CS}$ input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI/O	I/O	–	–	8	Control Data Input/output	This is Control Data I/O pin wich is provided on the TS5071. Serial control information is shifted into or out of COMBO IIG on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table 1.
CI CO	I O	11 10	12 11	– –	Control Data Input Control Data Output	These are separate controls, availables only on the TS5070. They can be wired together if required.
$\overline{CS}$	I	13	14	10	Chip Select	When this pins is low, control information can be written into or out of COMBO IIG via the CI and CO pins (or CI/O).
MR	I	14	15	11	Master Reset	This logic input must be pulled low for normal operation of COMBO IIG. When pulled momentarily high, all programmable registers in the device are reset to the states specified under "Power–on Initialization".

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes COMBO IIG and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for no output, the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing a Power-Down instruction into the serial control port as indicated in table 1. The power down instruction may be included within any other instruction code. It is recommended that the chip be powered down before executing any instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 and D_X1 outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains operational. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control a SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are needed to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active prefilter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see table 1 and 2). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Post-Filter/Power Amplifier capable of driving a 300 Ω load to ± 3.5 V, a 600 Ω load to ± 3.8 V or 15 kΩ load to ± 4.0 V at peak overload.

A decode cycle begins immediately after each receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (1/2 frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK to a square wave. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see table 2). Non delayed data mode is similar to long-frame timing on the ETC 5050/60 series of devices : time-slots being nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode which is similar to short-frame sync timing, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot.

The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing. When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters. Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles.

During each assigned transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. TS_X0 (or TS_X1 as appropriate) also pulls low for the first 7 1/2 bit times of the time-slot to control the TRI-STATE Enable of a backplane line driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TS5070 only.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO IIG via the serial control port consisting of the control clock CCLK ; the serial data input/output CI/O (or separate input CI, and output $\overline{CO}$ on the TS5070 only) ; and the Chip Select input $\overline{CS}$. All control instructions require 2 bytes, as

listed in table 1, with the exception of a single byte power-up/down command. To shift control data into COMBO IIG, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI or CI/O input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first continuously, i.e. it is not mandatory for $\overline{CS}$ to return high in between the first and second control bytes. On the falling edge of the 8th CCLK clock pulse in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However $\overline{CS}$ should be set high when no data transfers are in progress.

To readback interface Latch data or status information from COMBO IIG, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in table 1. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO or CI/O pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together. Thus, to summarize, 2-byte READ and WRITE instructions may use either two 8-bit wide $\overline{CS}$ pulses or a single 16-bit wide $\overline{CS}$ pulse.

Table 1 : Programmable Register Instructions.

Function	Byte 1 7	6	5	4	3	2	1	0	Byte 2
Single Byte Power–up/down	P	X	X	X	X	X	0	X	None
Write Control Register	P	0	0	0	0	0	1	X	See Table 2
Read–back Control Register	P	0	0	0	0	1	1	X	See Table 2
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table 4
(LDR)	P	0	0	1	0	1	1	X	See Table 4
Read Latch Direction Register									
Write Latch Content Register (ILR)	P	0	0	0	1	0	1	X	See Table 5
Read Latch Content Register	P	0	0	0	1	1	1	X	See Table 5
Write Transmit Time–slot/port	P	1	0	1	0	0	1	X	See Table 6
Read–back Transmit Time–slot/port	P	1	0	1	0	1	1	X	See Table 6
Write Receive Time–slot/port	P	1	0	0	1	0	1	X	See Table 6
Read–back Receive Time–slot/port	P	1	0	0	1	1	1	X	See Table 6
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table 7
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table 7
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table 8
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table 8
Write Hybrid Balance Register ≠ 1	P	0	1	1	0	0	1	X	See Table 9
Read Hybrid Balance Register ≠ 1	P	0	1	1	0	1	1	X	See Table 9
Write Hybrid Balance Register ≠ 2	P	0	1	1	1	0	1	X	See Table 10
Read Hybrid Balance Register ≠ 2	P	0	1	1	1	1	1	X	See Table 10
Write Hybrid Balance Register ≠ 3	P	1	0	0	0	0	1	X	
Read Hybrid Balance Register ≠ 3	P	1	0	0	0	1	1	X	

Notes : 1. Bit 7 of bytes 1 and 2 is always the first bit clocked into or out of the CI, CO or CI/CO pin.
2. "P" is the power-up/down control bit, see "Power-up" section ("0" = Power Up "1" = Power Down).
X = Don't Care.

PROGRAMMABLE FUNCTIONS

POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in table 1 into COMBO IIG with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down be setting the "P" bit as indicated. When the power up or down control is ente-

red as a single byte instruction, bit one (1) must be set to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in table 1. The second byte functions are detailed in table 2.

MASTER CLOCK FREQUENCY SELECTION

A Master clock must be provided to COMBO IIG for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see table 2) must be set during initialization to select the correct internal divider.

CODING LAW SELECTION

Bits "MA" and "IA" in table 2 permit the selection of μ255 coding or A-law coding with or without even-bit inversion.

ANALOG LOOPBACK

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in table 2. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

DIGITAL LOOPBACK

Digital Loopback mode is entered by setting the "DL" bit in the Control Register as shown in table 2. This

Table 2 : Control Register Byte 2 Functions.

Bit Number								Function
7	6	5	4	3	2	1	0	
F1	F0	MA	IA	DN	DL	AL	PP	
0 0 1 1	0 1 0 1							MCLK = 512 kHz MCLK = 1. 536 or 1. 544 MHz MCLK = 2. 048 MHz * MCLK = 4. 096 MHz
		0 1 1	X 0 1					Select μ. 255 Law * A–law, Including Even Bit Inversion A–Law, No Even Bit Inversion
				0 1				Delayed Data Timing Non–delayed Data Timing *
					0 1 0	0 X 0		Normal Operation * Digital Loopback Analog Loopback
							0 1	Power Amp Enabled in PDN * Power Amp Disabled in PDN

* = State at power-on initialization (bit 4 = 0).

Table 3 : Coding Law Conventions.

	μ255 Law								True A–law Including Even Bit Inversion								A–law Without Even Bit Inversion							
	MSB							LSB	MSB							LSB	MSB							LSB
V_{IN} = + Full Scale	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
V_{IN} = 0 V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
V_{IN} = – Full Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1	1	1	1

Note : The MSB is always the first PCM bit shifted in or out of COMBO IIG.

mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at D_X0 or D_X1.

For Analog Loopback as well as for Digital Loopback PCM decoding continues and analog output appears at VF_RO. The output can be disabled by programming "no output" in the Receive Gain Register (see table 8).

INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see table 1 and 4. Bits L_5-L_0 must be set by writing the specific instruction to the LDR with the L bits in the second byte set as specified in table 4. Unused interface latches should be programmed as outputs.

Table 4 : Byte 2 Functions of Latch Direction Register.

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

L_N Bit	IL Direction
0	Input *
1	Output

* = State at power-on initialization.
Note : L5 should be programmed as an output for the TS5071.

INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Latch Content Register (ILR) as shown in tables 1 and 5. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR. It is recommended that, during initialization, the state of IL pins to be configured as outputs should first be programmed, followed immediately by the Latch Direction Register.

Table 5 : Interface Latch Data Bit Order.

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

TIME-SLOT ASSIGNMENT

COMBO IIG can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delayed Data timing : see figure 6. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Table 6 : Byte 2 of Time-slot and Port Assignment Instructions.

Bit Number								Function
7 EN	6 PS (note 1)	5 T5 (note 2)	4 T4	3 T3	2 T2	1 T1	0 T0	
0	X	X	X	X	X	X	X	Disable D_X Outputs (transmit instruction) * Disable D_R Inputs (receive instruction) *
1	0	Assign One Binary Coded Time–slot from 0–63						Enable D_X0 Output, Disable D_X1 Output (Transmit instruction)
		Assign One Binary Coded Time–slot from 0–63						Enable D_R0 Input, Disable D_R1 Input (receive instruction)
1	1	Assign One Binary Coded Time–slot from 0–63						Enable D_X1 Output, Disable D_X0 Output (Transmit instruction)
		Assign One Binary Coded Time–slot from 0–63						Enable D_R1 Input, Disable D_R0 Input (receive instruction)

Notes : 1. The "PS" bit MUST always be set to 0 for the TS5071.
2. T5 is the MSB of the time-slot assignment.
* = State at power-on initialization.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in table 1 and 6. The last 6 bits of the second byte indicate the selected time-slot from 0-63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip Select for the second control byte. The "EN" bit allows the PCM inputs $D_R0/1$ or outputs $D_X0/1$ as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed timing format shown in figure 6.

PORT SELECTION

On the TS5070 only, an additional capability is available : 2 Transmit serial PCM ports, D_X0 and D_X1 and 2 receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte.

On the TS5071, only ports D_X0 and D_R0 are available, therefore the "PS" bit MUST always be set to 0 for these devices.

Table 6 shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in tables 1 and 7. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.087 Vrms (equivalent to + 6.4 dBm to – 19.0 dBm in 600 Ω). To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10} (V/\sqrt{0.6}) + 191$$

and convert to the binary equivalent. Some examples are given in table 7.

Table 7 : Byte 2 of Transmit Gain Instructions.

Bit Number								0dBm0 Test Level at VF_XI	
7	6	5	4	3	2	1	0	In dBm (into 600 Ω)	In Vrms
0	0	0	0	0	0	0	0	No Output *	
0	0	0	0	0	0	0	1	– 19	0. 087
0	0	0	0	0	0	1	0	– 18. 9	0. 088
1	0	1	1	1	1	1	1	0	0. 775
1	1	1	1	1	1	1	0	+ 6.3	1. 60
1	1	1	1	1	1	1	1	+ 6.4	1. 62

* = state at power initialization.

RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in table 1 and 8. Note the following restriction on output drive capability :

a) 0 dBm0 levels ≤ 1.97 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND,

b) 0 dBm0 levels ≤ 1.86 Vrms at VF_RO may be driven into a load of ≥ 600 Ω to GND,

c) 0 dBm levels ≤ 1.71 Vrms at VF_RO may be driven into a load of ≥ 300 Ω to GND.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10} (V/\sqrt{0.6}) + 174$$

and convert to the binary equivalent. Some examples are given in table 8.

Table 8 : Byte 2 of Receive Gain Instructions.

Bit Number								0dBm0 Test Level at VF_RO	
7	6	5	4	3	2	1	0	In dBm (into 600 Ω)	In Vrms
0	0	0	0	0	0	0	0	No Output * (low Z to GND)	
0	0	0	0	0	0	0	1	− 17. 3	0. 106
0	0	0	0	0	0	1	0	− 17. 2	0. 107
1	0	1	0	1	1	1	0	0	0. 775
1	1	1	1	0	0	1	1	+ 6. 9 (note 1)	1. 71
1	1	1	1	1	0	1	0	+ 7.6 (note 2)	1. 86
1	1	1	1	1	1	1	1	+ 8.1 (note 3)	1. 97

Notes : 1. Maximum level into 300 Ω.
2. Maximum level into 600 Ω.
3. RL ≥ 15 kΩ.
* = State at power on initialization.

HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO IIG is a programmable filter consisting of a second-order Bi-Quad section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The Bi-Quad is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals. The attenuator can be programmed to compensate for VF_RO to VF_XI echos in the range of − 2.5 to − 8.5 dB.

As a Bi-Quad, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring the Bi-Quad, matching the phase of the hybrid at low to midband frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The Bi-Quad mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low frequency pole and 0 Hz zero. In this mode, the pole frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Table 9 : Hybrid Balance Register 1 Byte 2 Instruction.

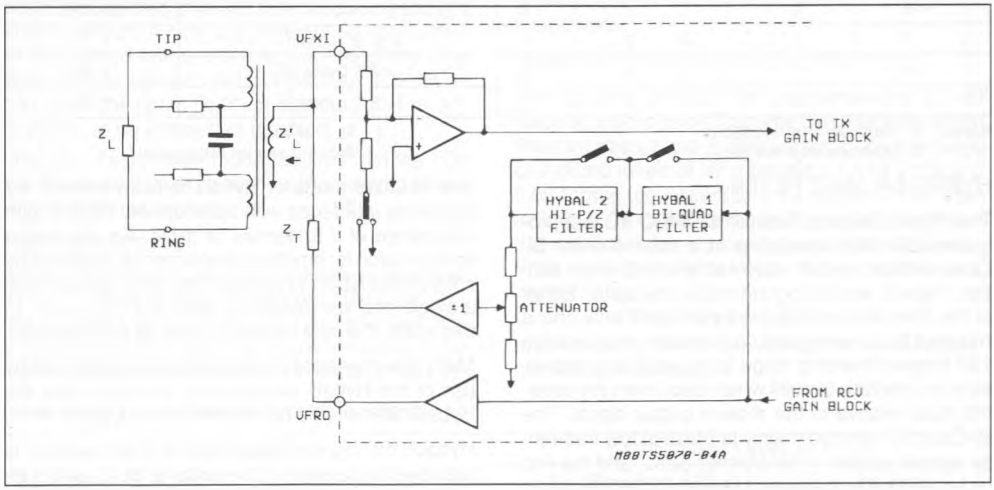
Bit	State	Function
7	0	Disable Hybrid Balance Circuit Completely. No internal cancellation is provided. *
	1	Enable Hybrid Balance Cancellation Path
6	0	Phase of the internal cancellation signal assumes inverted phase of the echo path from VF_RO to VF_XI.
	1	Phase of the internal cancellation signal assumes no phase inversion in the line interface.
5	0	Bypass Hybal 2 Filter Section
	1	Enable Hybal 2 Filter Section
G4–G0		Attenuation Adjustment for the Magnitude of the Cancellation Signal. Range is − 2.5 dB (00000) to − 8.5 dB (11000).

* = State at power on initialization.
Settling = Please refer to software TS5077-2.

Figure 1 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI are a function of the termination impedance Z_T, the line transformer and the impedance of the 2 W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is :

$$H(W) = Z_L' / (Z_T + Z_L')$$

Figure 1 : Simplified Diagram of Hybrid Balance Circuit.



PROGRAMMING THE FILTER

On initial power-up the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2 W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900 Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in figure 1. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input D_R0, to the PCM digital output D_X0, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO IIG to fully configure the Hybrid Balance Filter as follows :

Register 1 : select/de-select Hybrid Balance Filter
invert/non-invert cancellation signal
select/de-select Hybal2 filter section attenuator setting.

Register 2 : select/de-select Hybal1 filter
set Hybal1 to Bi-Quad or 1st order
program pole and zero frequency.

Table 10 : Hybrid Balance Register 2 Byte 2 Instruction.

Bit Number								Function
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	By Pass Hybal 1 Filter
X	X	X	X	X	X	X	X	Pole/zero Setting

Register 3 : program pole frequency in Hybal2 filter
program zero frequency in Hybal2 filter
settings = Please refer to software TS5077-2.

Standard filter design techniques may be used to model the echo path and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter programmed to replicate it.

An Hybrid Balance filter design guide and software optimization program are available under license from SGS-Thomson Microelectronics (order TS5077-2).

APPLICATION INFORMATION

Figure 2 shows a typical application of the TS5070 together with a transformer SLIC.

The design of the transformer is greatly simplified due to the on-chip hybrid balance cancellation filter. Only one single secondary winding is required (see application note AN.091 - Designing a subscriber line card module using the TS5070/COMBO IIG). Figures 3 and 4 show an arrangement with SGS-Thomson monolithic SLICS.

POWER SUPPLIES

While the pins of the TS5070 and TS5071/COMBO IIG devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a Schottky diode connected between V_{SS} and GND. To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 µF should be connected from this common device ground point to V_{CC} and V_{SS} as close to the device pins as possible. V_{CC} and V_{SS} should be decoupled with low effective series resistance capacitors of at least 10 µF near the card edge connector.

Figure 2 : Transformer SLIC + COMBO IIG.

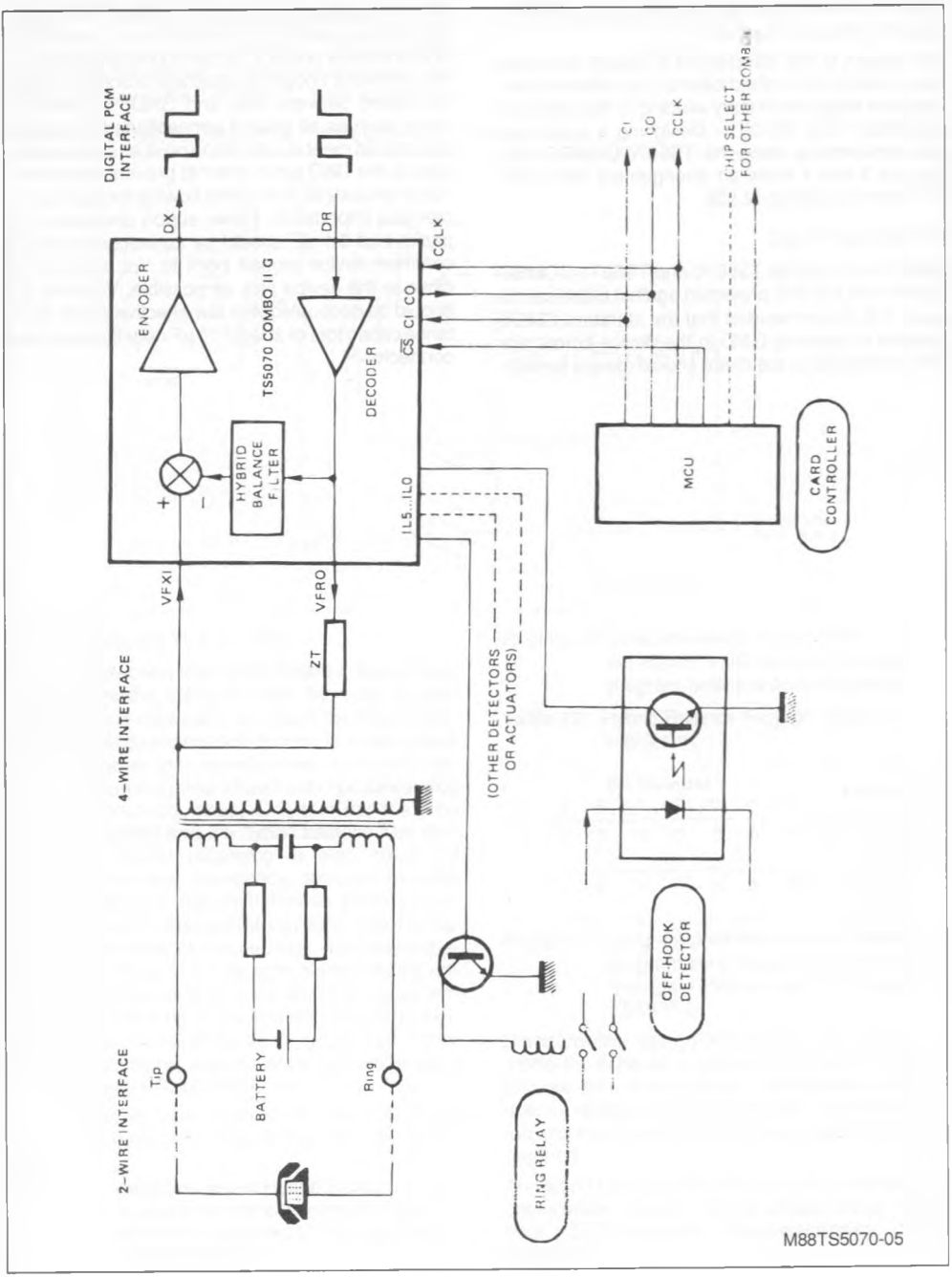


Figure 3 : Interface with TDB 7711 + 7712 or L3010 + L3000 Silicon SLIC.

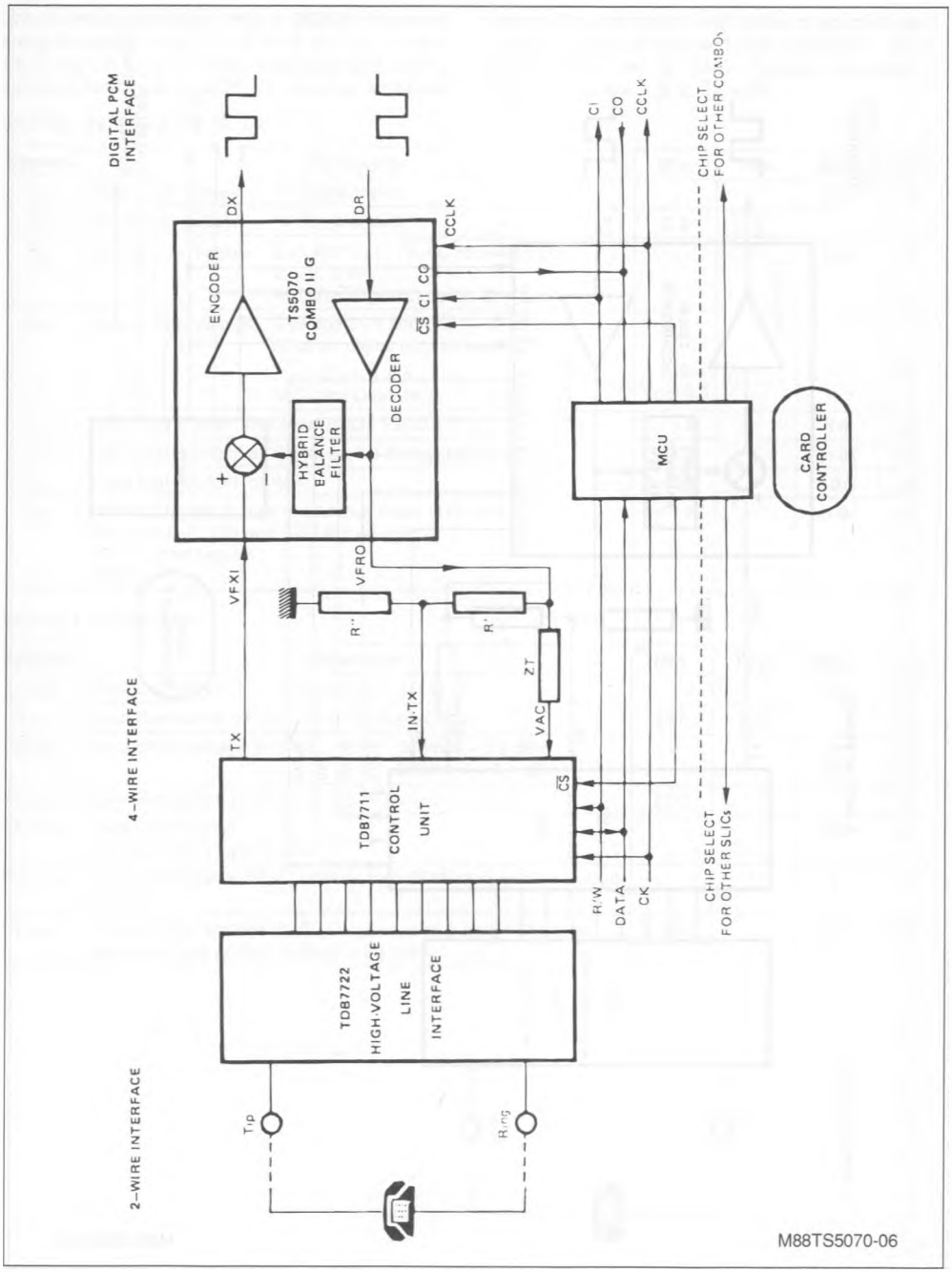
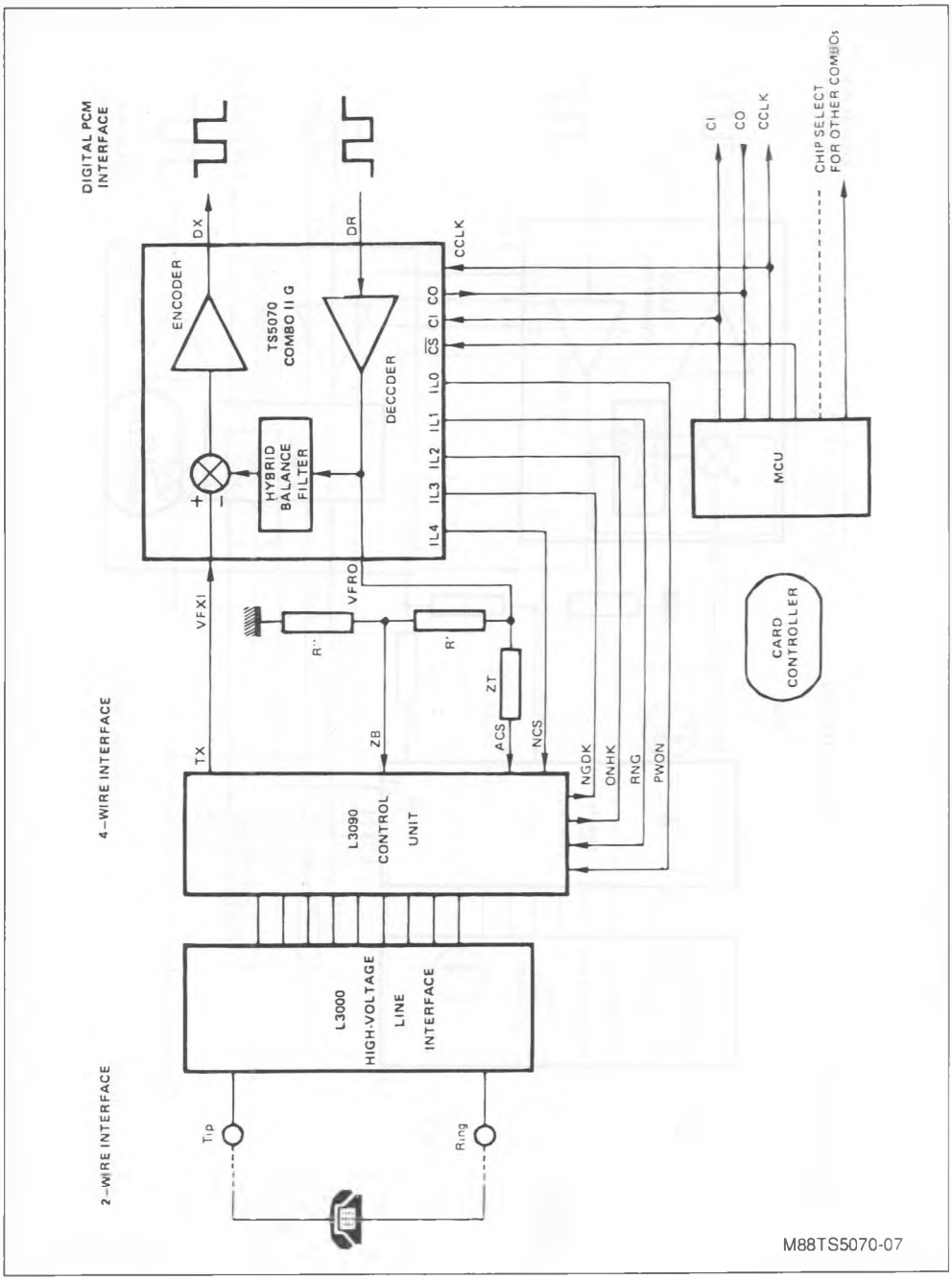


Figure 4 : Interface with L3090 + L3000 Silicon SLIC.



ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, limits in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = − 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterisation. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = − 5 V, T_A = 25 °C.

DIGITAL INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			**0.7**	V
V_{IH}	Input high Voltage	All Digital Inputs	**2.0**			
V_{OL}	Output Low Voltage	D_X0 and D_X1, TS_XO, $\overline{TS_X}1$ and CO, IL = 3. 2 mA All Other Digital Outputs, IL = 1 mA			**0.4**	V
V_{OH}	Output high Voltage	D_X0 and D_X1 and CO, I_L = − 3.2 mA All other digital outputs except $\overline{TS_X}$, IL = − 1 mA All Digital Outputs, I_L = − 100 µA	**2.4** V_{CC}–0.5			V V
I_{IL}	Input Low Current all Digital Inputs (GND < V_{IN} < V_{IL})		**− 10**		**10**	µA
I_{IH}	Input High Current all Digital Inputs Except MR (V_{IH} < V_{IN} < V_{CC})		**− 10**		**10**	µA
I_{IH}	Input High Current on MR		**− 10**		**100**	µA
I_{OZ}	Output Current in High Impedance State (TRI–STATE) D_X0 and D_X1, CO and CI/O (as an input) IL5 – IL0 as Inputs (GND < V_O < V_{CC})		**− 10**		**10**	µA

ANALOG INTERFACE

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{VFXI}	Input Current VF_XI (− 3.3 V < VF_XI < 3.3 V)		**− 10**		**10**	µA
R_{VFXI}	Input Resistance VF_XI (− 3.3 V < VF_XI < 3.3 V)		**390**	620		kΩ
VOS_X	Input offset voltage at VF_XI	0dBm0= − 19 dBm 0dBm0 = + 6.4 dBm			20 200	mV mV
RL_{VFRO}	Load Resistance at VF_RO (− 3.5 V < VF_RO < 3.5 V)		**300**			Ω
CL_{VFRO}	Load Capacitance CL_{VFRO} from VF_RO to GND				**200**	pF
RO_{VFRO}	Output Resistance VF_RO (steady zero PCM code applied to D_R0 or D_R1)			1	3	Ω
V_{OSR}	Output Offset Voltage at VF_RO (alternating ± zero PCM code applied to D_R0 or D_R1, 0dBm0 = 8.1 dBm)		**− 200**		**200**	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
ICC0	Power Down Current (CCLK, CI/O, CI = 0.4 V, $\overline{CS}$ = 2.4 V) Interface latches set as outputs with no load. All Other Inputs active, Power Amp Disabled		.3	**1.5**	mA
–ISS0	Power Down Current (as above)		.1	**0.3**	mA
ICC1	Power Up Current (CCLK, CI/O, CI = 0.4 V, $\overline{CS}$ = 2.4 V) No Load on Power Amp Interface latches set as outputs with no load.		7	**10**	mA
–ISS1	Power Up Current (as above)		7	**10**	mA

TIMING SPECIFICATIONS

Unless otherwise noted, limits in BOLD characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = 5 V, T_A = 25 °C. All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.

See Definitions and Timing Conventions section for test methods information.

MASTER CLOCK TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK (selection of frequency is programmable, see table 2)		512 1.536 1.544 2.048 **4.096**		kHz MHz MHz MHz MHz
t_{WMH}	Period of MCLK High (measured from V_{IH} to V_{IH}, see note 1)	**80**			ns
t_{WML}	Period of MCLK Low (measured from V_{IL} to V_{IL}, see note 1)	**80**			ns
t_{RM}	Rise Time of MCLK (measured from V_{IL} or V_{IH})			30	ns
t_{FM}	Fall Time of MCLK (measured from V_{IH} to V_{IL})			30	
t_{HBM}	Hold Time, BCLK Low to MCLK High (TS5070 only)	**50**			ns
t_{WFL}	Period of FS_X or FS_R Low	2			µs

TIMING SPECIFICATIONS (continued)

PCM INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{BCLK}	Frequency of BCLK (may vary from 64 kHz to 4.096 MHz in 8 kHz increments, TS5070 only)	**64**		**4.096**	kHz
t_{WBH}	Period of BCLK High (measured from V_{IH} to V_{IH})	**80**			ns
t_{WBL}	Period of BCLK Low (measured from V_{IL} to V_{IL})	**80**			ns
t_{RB}	Rise Time of BCLK (measured from V_{IL} to V_{IH})			30	ns
t_{FB}	Fall Time of BCLK (measured from V_{IH} to V_{IL})			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low	**0**			ns
t_{SFB}	Setup Time $FS_{X/R}$ High to BCLK Low	**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid (load = 100 pF plus 2 LSTTL loads)			**80**	ns
t_{DBZ}	Delay Time from BCLK8 Low to Dx disabled (if FSx already low) ; FSx Low to Dx Disabled (if BCLK8 low) ; BCLK9 High to Dx Disabled (if FSx still high) ;	**15**		**80**	ns
t_{DBT}	Delay Time, from BCLK and FS_X Both High to $\overline{TS}_X$ Low (load = 100 pF plus 2 LSTTL loads)			60	ns
t_{ZBT}	Delay Time from BCLK8 low to $\overline{TS}x$ Disabled (if FSx already low) ; FSx Low to $\overline{TS}x$ Disabled (if BCLK8 low) ; BCLK9 High to $\overline{TS}x$ Disabled (if FSx still high) ;	15		60	ns
t_{DFD}	Delay Time, FS_X High to Data Valid (load = 100 pF plus 2 LSTTL loads, applies if FS_X rises later than BCLK rising edge in non–delayed data mode only)			**80**	ns
t_{SDB}	Setup Time , D_R 0/1 Valid to BCLK Low	**30**			ns
t_{HDB}	Hold Time, BCLK Low to D_R 0/1 Invalid	**10**			ns

Note : 1. Applies only to MCLK frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ± 2 % duty cycle must be used.

Figure 5 : Non Delayed Data Timing (long frame mode).

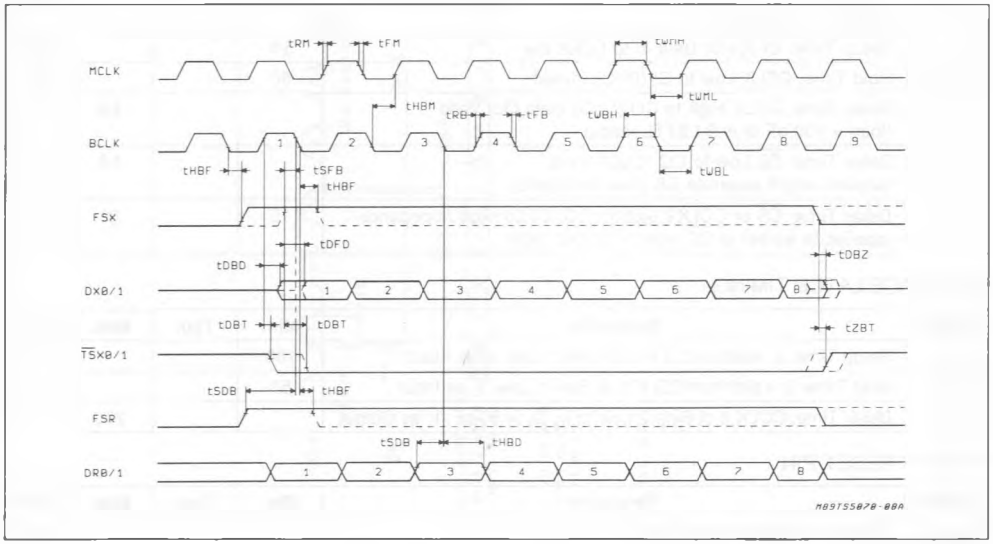
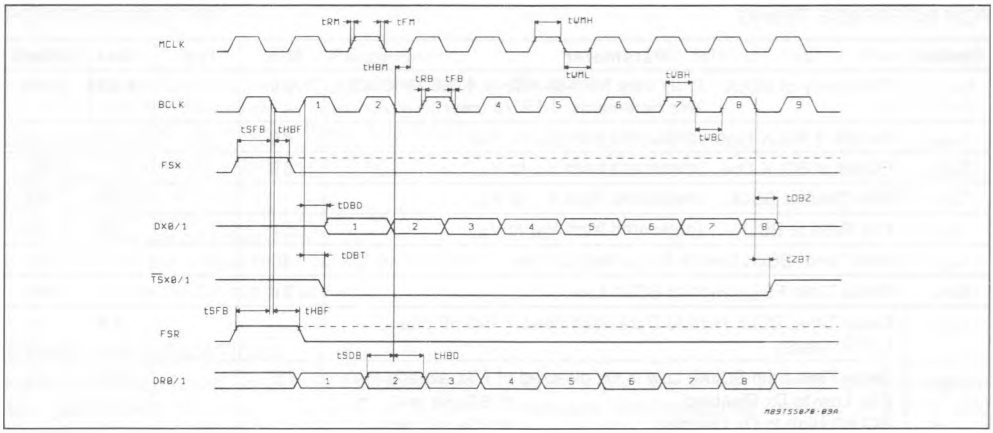


Figure 6 : Delayed Data Timing (short frame mode).



SERIAL CONTROL PORT TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK			**2.048**	MHz
t_{WCH}	Period of CCLK High (measured from V_{IH} to V_{IH})	**160**			ns
t_{WCL}	Period of CCLK Low (measured from V_{IL} to V_{IL})	**160**			ns
t_{RC}	Rise Time of CCLK (measured from V_{IL} to V_{IH})			50	ns
t_{FC}	Fall Time of CCLK (measured from V_{IH} to V_{IL})			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low (CCLK1)	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High (CCLK8)	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low	**70**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High (to insure CO is not enabled for single byte)	**50**			ns
t_{SDC}	Setup Time, CI (CI/O) Data in to CCLK low	**50**			ns
t_{HCD}	Hold Time, CCLK Low to CI (CI/O) Invalid	50			ns
t_{DCD}	Delay Time, CCLK High to CO (CI/O) Data Out Valid (load = 100 pF plus 2 LSTTL loads)			**50**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid (applies only if separate $\overline{CS}$ used for byte 2)			**50**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or CCLK9 High to CO (CI/O) High Impedance (applies to earlier of $\overline{CS}$ high or CCLK9 high)	15		80	ns

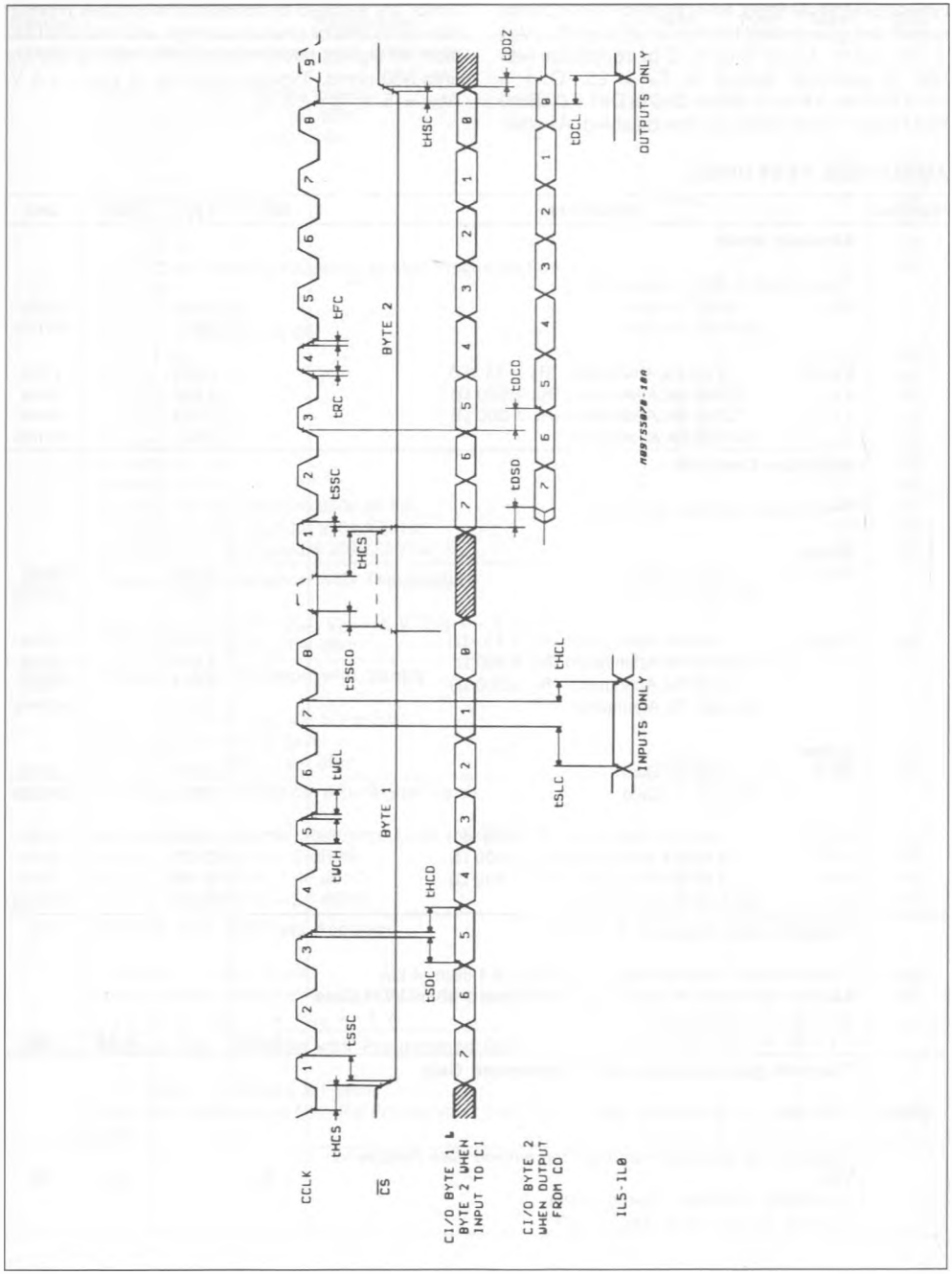
INTERFACE LATCH TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SLC}	Setup Time, I_L Valid to CCLK 8 of Byte 1 Low. I_L as Input	**100**			ns
t_{HCL}	Hold Time, I_L Valid from CCLK 8 of Byte 1 Low. I_L as Input	50			ns
t_{DCL}	Delay Time, CCLK 8 of Byte 2 Low to I_L. C_L = 50 pF. I_L as Output			200	ns

MASTER RESET PIN

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WMR}	Duration of Master Reset High	1			µs

Figure 7 : Control Port Timing.



TRANSMISSION CHARACTERISTICS

Unless otherwise noted, limits printed in BOLD characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = − 5 V ± 5 %, T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code, Hybrid Balance filter disabled. All other limits are assured by correlation with other production tests and/or product de-sign and characterization. All signals referenced to GND. dBm levels are into 600 ohms. Typicals specified at V_{CC} = + 5 V, V_{SS} = 5 V, T_A = 25 °C.

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels				
	The nominal 0 dBm 0 levels are :				
	VF_XI 0 dB Tx Gain		1.618		Vrms
	25.4 dB Tx Gain		86.9		mVrms
	VF_RO 0 dB Rx Attenuation (RL ≥ 15 kΩ)		1.968		Vrms
	0.5 dB Rx Attenuation (RL ≥ 600 Ω)		1.858		Vrms
	1.2 dB Rx Attenuation (RL ≥ 300 Ω)		1.714		Vrms
	25.4 dB Rx Attenuation		105.7		mVrms
	Maximum Overload				
	The nominal overload levels are :				
	A-law				
	VF_XI 0 dB Tx Gain		2.323		Vrms
	25.4 dB Tx Gain		124.8		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.825		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 300 Ω)		2.667		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.461		Vrms
	25.4 dB Rx Attenuation		151.7		mVrms
	μ-law				
	VF_XI 0 dB Tx Gain		2.332		Vrms
	25.4 dB Tx Gain		125.2		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.836		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 600 Ω)		2.677		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.470		Vrms
	25.4 dB Rx Attenuation		152.3		mVrms
	Transmit Gain Absolute Accurary				
GXA	Transmit Gain Programmed for 0 dBm0 = 6.4 dBm, A-law Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$, f = 1015.625 Hz T_A = 25 °C, V_{CC} = 5 V, V_{SS} = − 5 V	**− 0.15**		**0.15**	dB
	Transmit gain Variation with Programmed Gain				
GXAG	− 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm Calculate the Deviation from the Programmed Gain Relative to GXA i.e., GXAG = Gactual − Gprog − GXA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = − 5 V	**− 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GXAF	**Transmit Gain Variation with Frequency**				
	Relative to 1015.625 Hz (note 2) – 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm D_R0 (or D_R1) = 0 dBm0 Code				
	f = 60 Hz			– 26	dB
	f = 200 Hz	– 1.8		– 0.1	dB
	f = 300 Hz to 3000 Hz	– 0.15		0.15	dB
	f = 3400 Hz	– 0.7		0	dB
	f = 4000 Hz			– 14	dB
	f ≥ 4600 Hz Measure Response at Alias Frequency from 0 kHz to 4 kHz			– 32	dB
	0 dBm0 = 6.4 dBm VF_XI = – 4 dBm0 (note 2)				
	f = 62.5 Hz			**– 24.9**	dB
	f = 203.125 Hz	**– 1.7**		**– 0.1**	dB
	f = 2093.750 Hz	**– 0.15**		**0.15**	dB
	f = 2984.375 Hz	**– 0.15**		**0.15**	dB
	f = 3296.875 Hz	**– 0.15**		**0.15**	dB
	f = 3406.250 Hz	**– 0.7**		**0**	dB
	f = 3984.375 Hz			**– 13.5**	dB
	f = 4593.750 Hz, Measure 3406.25 Hz			**– 32**	dB
	f = 5015.625 Hz, Measure 2984.375 Hz			**– 32**	dB
	f = 10015.625 Hz, Measure 2015.625 Hz			**– 32**	dB
GXAT	**Tansmit Gain Variation with Temperature**				
	Measured Relative to G_{XA}, V_{CC} = 5 V, V_{SS} = – 5 V – 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm	– 0.1		0.1	dB
GXAV	**Transmit Gain Variation with Supply**				
	V_{CC} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 % Measured Relative to GXA T_A = 25 °C, 0 dBm0 = 6.4 dBm	**– 0.05**		**0.05**	dB
GXAL	**Transmit Gain Variation with Signal Level**				
	Sinusoidal Test Method, Reference Level = 0 dBm0				
	VF_XI = – 40 dBm0 to + 3 dBm0	**– 0.2**		**0.2**	dB
	VF_XI = – 50 dBm0 to – 40 dBm0	**– 0.4**		**0.4**	dB
	VF_XI = – 55 dBm0 to – 50 dBm0	**– 1.2**		**1.2**	dB
GRA	**Receive Gain Absolute Accuracy**				
	0 dBm0 = 8.1 dBm, A-law Apply 0 dBm0 PCM Code to D_R0 or D_R1 Measure VF_RO T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.15**		**0.15**	dB
GRAG	**Receive Gain Variation with Programmed Gain**				
	– 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm Calculate the Deviation from the Programmed Gain Relative to GRA	**– 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	i.e. GRAG = Gactual – Gprog – GRA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V				
GRAT	**Receive Gain Variation with Temperature** Measured Relative to GRA V_{CC} = 5 V, V_{SS} = – 5 V – 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm	– 0.1		0.1	dB
GRAV	**Receive Gain Variation with Supply** Measured Relative to G_{RA} V_{CC} = 5 V ± 5 %, V_{SS} = – 5 V ± 5 % T_A = 25 °C, 0 dBm 0 = 8.1 dBm	**– 0.05**		**0.05**	dB
GRAF	**Receive Gain Variation with Frequency** Relative to 1015.625 Hz, (note 2) D_R0 or D_R1 = 0 dBm0 Code – 17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz GR = 0 dBm0 = 8.1 dBm GX = D_R0 = – 4 dBm0 f = 296.875 Hz f = 1906.250 Hz f = 2812.500 Hz f = 2984.375 Hz f = 3406.250 Hz f = 3984.375 Hz	 – 0.25 – 0.15 – 0.7 **– 0.15** **– 0.15** **– 0.15** **– 0.15** **– 0.7**		 0.15 0.15 0 – 14 **0.15** **0.15** **0.15** **0.15** **0** **– 13.5**	 dB dB dB dB dB dB dB dB dB dB
GRAL	**Receive Gain Variation with Signal Level** Sinusoidal Test Method Reference Level = 0 dBm0 D_R0 = – 40 dBm0 to + 3 dBm0 D_R0 = – 50 dBm0 to – 40 dBm0 D_R0 = – 55 dBm0 to – 50 dBm0	 **– 0.2** **– 0.4** **– 1.2**		 **0.2** **0.4** **1.2**	 dB dB dB

ENVELOPPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
DXA	**Tx Delay Absolute**			315	µs
	f = 1600 Hz				
DXR	**Tx Delay, Relative**				
	f = 500 – 600 Hz			220	µs
	f = 600 – 800 Hz			145	µs
	f = 800 – 1000 Hz			75	µs
	f = 1000 – 1600 Hz			40	µs
	f = 1600 – 2600 Hz			75	µs
	f = 2600 – 2800 Hz			105	µs
	f = 2800 – 3000 Hz			155	µs
DRA	**Rx Delay, Absolute**				
	f = 1600 Hz			200	µs
DRR	**Rx Delay, Relative**				
	f = 500 – 1000 Hz	– 40			µs
	f = 1000 – 1600 Hz	– 30			µs
	f = 1600 – 2600 Hz			90	µs
	f = 2600 – 2800 Hz			125	µs
	f = 2800 – 3000 Hz			175	µs

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
NXC	**Transmit Noise, C Message Weighted** μ-law Selected (note 3) o dBm0 = 6.4 dBm		12	**15**	dBrnC0
NXP	**Transmit Noise, Psophometric Weighted** A-law Selected (note 3) 0 dBm0 = 6.4 dBm		– 74	**– 67**	dBm0p
NRC	**Receive Noise, C Message Weighted** μ-law Selected PCM code is alternating positive		8	**11**	dBrnC0
NRP	**Receive Noise, Psophometric Weighted** A-law Selected PCM Code Equals Positive Zero		– 82	**– 79**	dBm0p
NRS	**Noise, Single Frequency** f = 0 kHz to 100 kHz, Loop Around Measurement VF_XI = 0 Vrms			– 53	dBm0
PPSRX	**Positive Power Supply Rejection Transmit** V_{CC} = 5 V_{DC} + 100 mVrms f = kHz – 50 kHz (note 4)	**30**			dBp
NPSRX	**Negative Power Supply Rejection Transmit** V_{SS} = – 5 VDC + 100 mVrms	**30**			dBp
PPSRR	**Positive Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{CC} = 5 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 **30** 40 36			 dBp dB dB
NPSRR	**Negative Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{SS} = – 5 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 **30** 40 36			 dBp dB dB
SOS	**Spurious Out-of Band Signals at the Channel Output** 0 dBm0 300 Hz to 3400Hz input PCM applied at D_R0 (D_R1) 4600 Hz – 7600 Hz 7600 Hz – 8400 Hz 8400 Hz – 100 000 Hz			 – 30 – 40 – 30	 dB dB dB

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STDX	**Signal to Total Distortion Transmit** Sinusoidal Test Method Half Channel				
	Level = 3 dBm0	**33**			dBp
	– 30 dBm0 to 0 dBm0	**36**			dBp
	– 40 dBm0	**29**			dBp
	– 45 dBm0	**25**			dBp
STDR	**Signal to Total Distortion Receive** Sinusoidal Test Method Half Channel				
	Level = 3 dBm0	**33**			dBp
	– 30 dBm0 to 0 dBm0	**36**			dBp
	– 40 dBm0	**30**			dBp
	– 45 dBm0	**25**			dBp
SFDX	Single frequency Distortion Transmit			**– 46**	dB
SFDR	Single Frequency Distortion Receive			**– 46**	dB
IMD	Intermodulation Distortion Transmit or Receive Two Frequencies in the Range 300 Hz – 3400 Hz			**– 41**	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CTX-R	transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 – 3400 Hz DR = Steady PCM Code		– 90	**– 75**	dB
CTR-X	Receive to transmit Crosstalk, 0 dBm0 Receive Level f = 300 – 3400 Hz, (note 4)		– 90	**– 70**	dB

Notes : 1. Applies only to MCLK frequencies ≥ 1.536 MHz. At 512 kHz A 50:50 ± 2 % duty cycle must be used.
2. A multi-tone test technique is used (peak/rms ≤ 9.5 dB).
3. Measured by extrapolation from distortion test result at – 50 dBm0.
4. PPSRX, NPSRX and CTR-X are measured with a – 50 dBm0 activation signal applied to VF_XI.
A signal is Valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purpose of the specification the following conditions apply :
a) All input signals are defined as V_{IL} = 0.4 V, V_{IH} = 2.7 V, t_R < 10 ns, t_F 10 ns
b) t_R is measured from V_{IL} to V_{IH}, t_F is measured from V_{IH} to V_{IL}
c) Delay Times are measured from the input signal Valid to the clock input invalid
d) Setup Times are measured from the data input Valid to the clock input invalid
e) Hold Times are measured from the clock signal Valid to the data input invalid
f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}

DEFINITIONS AND TIMING CONVENTIONS

DEFINITIONS

V_{IH}	V_{IH} is the D.C. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the D.C. input level below which an input level is guaranteed to appear as a logical zero the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltage applied to the device.
V_{OH}	V_{OH} is the minimmum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region Valid Signal	The threshold region is the range of input voltages between V_{IL} and V_{IH}. A signal is Valid if it is in one of the valid logic states. (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid signal	A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purpose of this timing specifications the following conventions apply :

Input Signals	All input signals may be characterized as : V_L = 0.4 V, V_H = 2.4 V, tR < 10 ns, tF < 10 ns.
Period	The period of the clock signal is designated as tPxx where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as tRyy, where yy represents a mnemonic of the signal whose rise time is being specified, tRyy is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as tFyy, where yy represents a mnemonic of the signal whose fall time is being specified, tFyy is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as tWzzH, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse width are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse is designated as tWzzL' where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse width are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as tSwwxx where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as THwwxx where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as TDxxyy [H/L], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.