

## CURRENT MODE PWM CONTROLLER

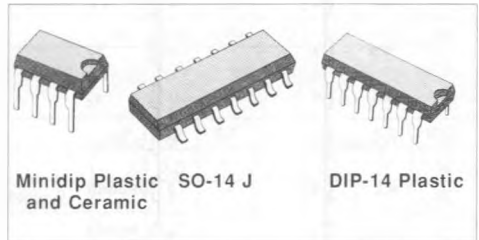
- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT ( $< 1 \text{ mA}$ )
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW  $R_O$  ERROR AMP

tor which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

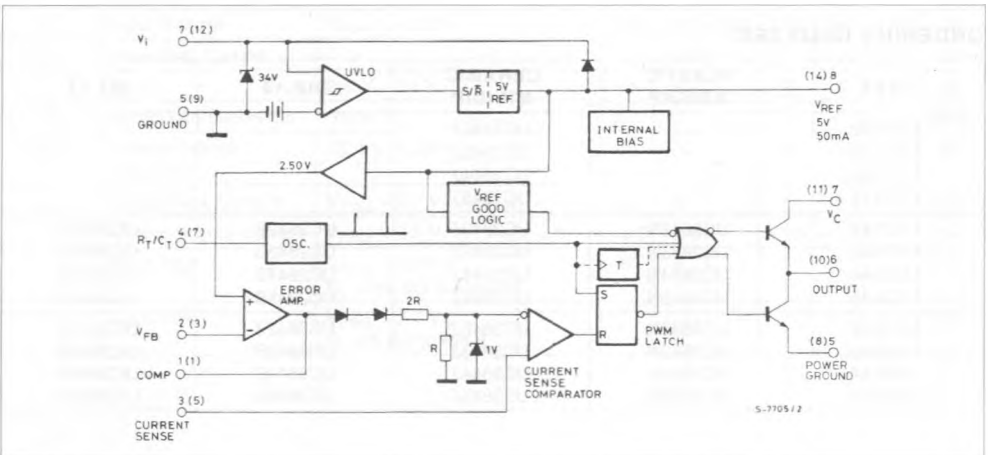
Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16 V (on) and 10 V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5 V and 7.9 V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of the zero to  $< 50\%$  is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

### DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM compara-



### BLOCK DIAGRAM (toggle flip flop used only in UC1844 and UC1845)



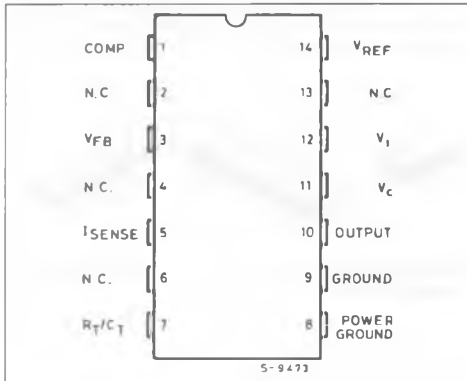
**ABSOLUTE MAXIMUM RATINGS \***

| Symbol    | Parameter   | Value         | Unit    |
|-----------|---|---------------|---------|
| $V_i$     | Supply Voltage (low impedance source)                       | 30            | V       |
| $V_i$     | Supply Voltage ( $I_i < 30$ mA)                             | Self Limiting |         |
| $I_O$     | Output Current  | $\pm 1$       | A       |
| $E_O$     | Output Energy (capacitive load)                             | 5             | $\mu$ J |
|           | Analog Inputs (pins 2, 3)                                   | - 0.3 to 6.3  | V       |
|           | Error Amplifier Output Sink Current                         | 10            | mA      |
| $P_{Tot}$ | Power Dissipation at $T_{amb} \leq 50$ °C (minidip, DIP-14) | 1             | W       |
| $P_{Tot}$ | Power Dissipation at $T_{amb} \leq 25$ °C (SO-14)           | 725           | mW      |
| $T_{sig}$ | Storage Temperature Range                                   | - 65 to 150   | °C      |
| $T_L$     | Lead Temperature (soldering 10 s)                           | 300           | °C      |

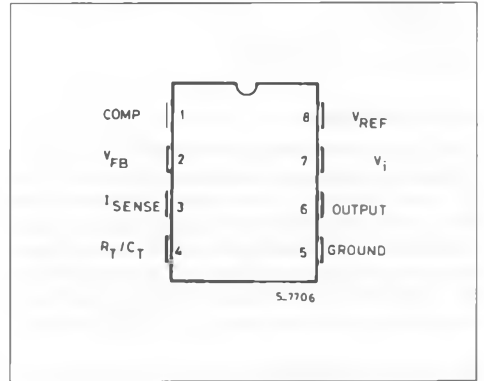
\* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

**BLOCK DIAGRAM (top view)**

DIP-14 / SO-14.



Minidip Plastic and Ceramic.



**ORDERING NUMBERS**

| TYPE   | PLASTIC MINIDIP | CERAMIC MINIDIP | DIP-14  | SO-14   |
|--------|-----------------|-----------------|---------|---------|
| UC1842 |                 | UC1842J         |         |         |
| UC1843 |                 | UC1843J         |         |         |
| UC1844 |                 | UC1844J         |         |         |
| UC1845 |                 | UC1845J         |         |         |
| UC2842 | UC2842N         | UC2842J         | UC2842B | UC2842D |
| UC2843 | UC2843N         | UC2843J         | UC2843B | UC2843D |
| UC2844 | UC2844N         | UC2844J         | UC2844B | UC2844D |
| UC2845 | UC2845N         | UC2845J         | UC2845B | UC2845D |
| UC3842 | UC3842N         | UC3842J         | UC3842B | UC3842D |
| UC3843 | UC3843N         | UC3843J         | UC3843B | UC3843D |
| UC3844 | UC3844N         | UC3844J         | UC3844B | UC3844D |
| UC3845 | UC3845N         | UC3845J         | UC3845B | UC3845D |

## THERMAL DATA

|                |                                     | Ceramic Minidip | Plastic Minidip | DIP-14 Plastic | SO-14    |
|----------------|-------------------------------------|-----------------|-----------------|----------------|----------|
| $R_{th j-amb}$ | Thermal Resistance Junction-ambient | 200 °C/W        | 100 °C/W        | 100 °C/W       | 165 °C/W |

**ELECTRICAL CHARACTERISTICS** (unless otherwise stated, these specifications apply for  $-55 \leq T_{amb} \leq 125$  °C for UC184X ;  $-25 \leq T_{amb} \leq 85$  °C for UC284X ;  $0 \leq T_{amb} \leq 70$  °C for UC384X ;  $V_i = 15$  V (Note 5) ;  $R_T = 10$  K ;  $C_T = 3.3$  nF)

| Symbol | Parameter | Test Conditions | UC184X<br>284X |      |      | UC384X |      |      | Unit |
|--------|-----------|-----------------|----------------|------|------|--------|------|------|------|
|        |           |                 | Min.           | Typ. | Max. | Min.   | Typ. | Max. |      |

## REFERENCE SECTION

|                           |                        |   |      |      |      |      |      |      |         |
|---------------------------|------------------------|---|------|------|------|------|------|------|---------|
| $V_{REF}$                 | Output Voltage         | $T_j = 25$ °C $I_o = 1$ mA  | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V       |
| $\Delta V_{REF}$          | Line Regulation        | $12 \text{ V} \leq V_i \leq 25 \text{ V}$                         |      | 6    | 20   |      | 6    | 20   | mV      |
| $\Delta V_{REF}$          | Load Regulation        | $1 \leq I_o \leq 20$ mA   |      | 6    | 25   |      | 6    | 25   | mV      |
| $\Delta V_{REF}/\Delta T$ | Temperature Stability  | (Note 2)  |      | 0.2  | 0.4  |      | 0.2  | 0.4  | mV/°C   |
|                           | Total Output Variation | Line Load Temperature (Note 2)                                    | 4.9  |      | 5.1  | 4.82 |      | 5.18 | V       |
| $e_N$                     | Output Noise Voltage   | $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$ $T_j = 25$ °C (Note 2) |      | 50   |      |      | 50   |      | $\mu$ V |
|                           | Long Term Stability    | $T_{amb} = 125$ °C. 1000 Hrs (Note 2)                             |      | 5    | 25   |      | 5    | 25   | mV      |
| $I_{sc}$                  | Output Short Circuit   |   | -30  | -100 | -180 | -30  | -100 | -180 | mA      |

## OSCILLATOR SECTION

|       |                       |  |    |     |    |    |     |    |     |
|-------|-----------------------|--|----|-----|----|----|-----|----|-----|
| $f_s$ | Initial Accuracy      | $T_j = 25$ °C (Note 6)                       | 47 | 52  | 57 | 47 | 52  | 57 | KHz |
|       | Voltage Stability     | $12 \leq V_i \leq 25$ V                      |    | 0.2 | 1  |    | 0.2 | 1  | %   |
|       | Temperature Stability | $T_{MIN} \leq T_{amb} \leq T_{MAX}$ (Note 2) |    | 5   |    |    | 5   |    | %   |
| $V_4$ | Amplitude             | $V_{PIN4}$ Peak to Peak                      |    | 1.7 |    |    | 1.7 |    | V   |

## ERROR AMP SECTION

|       |                          |   |      |      |      |      |      |      |         |
|-------|--------------------------|---|------|------|------|------|------|------|---------|
| $V_2$ | Input Voltage            | $V_{PIN1} = 2.5$ V                                      | 2.45 | 2.50 | 2.55 | 2.42 | 2.50 | 2.58 | V       |
| $I_b$ | Input Bias Current       |   |      | -0.3 | -1   |      | -0.3 | -2   | $\mu$ A |
|       | $A_{VOL}$                | $2 \leq V_o \leq 4$ V                                   | 65   | 90   |      | 65   | 90   |      | dB      |
| B     | Unity Gain Bandwidth     | (Note 2)  | 0.7  | 1    |      | 0.7  | 1    |      | MHz     |
| SVR   | Supply Voltage Rejection | $12 \leq V_i \leq 25$ V                                 | 60   | 70   |      | 60   | 70   |      | dB      |
| $I_o$ | Output Sink Current      | $V_{PIN2} = 2.7$ V $V_{PIN1} = 1.1$ V                   | 2    | 6    |      | 2    | 6    |      | mA      |
| $I_o$ | Output Source Current    | $V_{PIN2} = 2.3$ V $V_{PIN1} = 5$ V                     | -0.5 | -0.8 |      | -0.5 | -0.8 |      | mA      |
|       | $V_{OUT}$ High           | $V_{PIN2} = 2.3$ V ;<br>$R_L = 15$ K $\Omega$ to Ground | 5    | 6    |      | 5    | 6    |      | V       |
|       | $V_{OUT}$ Low            | $V_{PIN2} = 2.7$ V ;<br>$R_L = 15$ K $\Omega$ to Pin 8  |      | 0.7  | 1.1  |      | 0.7  | 1.1  | V       |

## ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | UC184X<br>UC284X |      |      | UC384X |      |      | Unit |
|--------|-----------|-----------------|------------------|------|------|--------|------|------|------|
|        |           |                 | Min.             | Typ. | Max. | Min.   | Typ. | Max. |      |

## CURRENT SENSE SECTION

|       |                          |   |      |     |      |     |     |     |               |
|-------|--------------------------|---|------|-----|------|-----|-----|-----|---------------|
| $G_v$ | Gain                     | (Notes 3 & 4)                           | 2.85 | 3   | 3.15 | 2.8 | 3   | 3.2 | V/V           |
| $V_3$ | Maximum Input Signal     | $V_{PIN1} = 5\text{ V}$ (Note 3)        | 0.9  | 1   | 1.1  | 0.9 | 1   | 1.1 | V             |
| SVR   | Supply Voltage Rejection | $12 \leq V_i \leq 25\text{ V}$ (Note 3) |      | 70  |      |     | 70  |     | dB            |
| $I_b$ | Input Bias Current       |   |      | -2  | -10  |     | -2  | -10 | $\mu\text{A}$ |
|       | Delay to Output          |   |      | 150 | 300  |     | 150 | 300 | ns            |

## OUTPUT SECTION

|          |                   |   |    |      |     |    |      |     |    |
|----------|-------------------|---|----|------|-----|----|------|-----|----|
| $I_{OL}$ | Output Low Level  | $I_{SINK} = 20\text{ mA}$   |    | 0.1  | 0.4 |    | 0.1  | 0.4 | V  |
|          |                   | $I_{SINK} = 200\text{ mA}$  |    | 1.5  | 2.2 |    | 1.5  | 2.2 |    |
| $I_{OH}$ | Output High Level | $I_{SOURCE} = 20\text{ mA}$   | 13 | 13.5 |     | 13 | 13.5 |     | V  |
|          |                   | $I_{SOURCE} = 200\text{ mA}$  | 12 | 13.5 |     | 12 | 13.5 |     |    |
| $t_r$    | Rise Time         | $T_j = 25\text{ }^\circ\text{C}$<br>$C_L = 1\text{ nF}$<br>(Note 2) |    | 50   | 150 |    | 50   | 150 | ns |
| $t_f$    | Fall Time         | $T_j = 25\text{ }^\circ\text{C}$<br>$C_L = 1\text{ nF}$<br>(Note 2) |    | 50   | 150 |    | 50   | 150 | ns |

## UNDER-VOLTAGE LOCKOUT SECTION

|  |                                      |        |     |     |     |      |     |      |   |
|--|--------------------------------------|--------|-----|-----|-----|------|-----|------|---|
|  | Start Threshold                      | X842/4 | 15  | 16  | 17  | 14.5 | 16  | 17.5 | V |
|  |                                      | X843/5 | 7.8 | 8.4 | 9.0 | 7.8  | 8.4 | 9.0  |   |
|  | Min. Operating Voltage After Turn-on | X842/4 | 9   | 10  | 11  | 8.5  | 10  | 11.5 | V |
|  |                                      | X843/5 | 7.0 | 7.6 | 8.2 | 7.0  | 7.6 | 8.2  |   |

## PWM SECTION

|  |                    |        |    |    |     |    |    |     |   |
|--|--------------------|--------|----|----|-----|----|----|-----|---|
|  | Maximum Duty Cycle | X842/3 | 93 | 97 | 100 | 93 | 97 | 100 | % |
|  |                    | X844/5 | 44 | 48 | 50  | 45 | 48 | 50  |   |
|  | Minimum Duty Cycle |        |    |    | 0   |    |    | 0   | % |

## TOTAL STANDBY CURRENT

|          |                          |                                    |  |     |    |  |     |    |             |
|----------|--------------------------|------------------------------------|--|-----|----|--|-----|----|-------------|
| $I_{st}$ | Start-up Current         |                                    |  | 0.5 | 1  |  | 0.5 | 1  | $\text{mA}$ |
| $I_i$    | Operating Supply Current | $V_{PIN2} = V_{PIN3} = 0\text{ V}$ |  | 11  | 20 |  | 11  | 20 | $\text{mA}$ |
| $V_{IZ}$ | Zener Voltage            | $I_i = 25\text{ mA}$               |  | 34  |    |  | 34  |    | V           |

Notes : 2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with  $V_{PIN2} = 0$ .

4. Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIND}} ; 0 \leq V_{PIN3} \leq 0.8\text{ V}$$

5. Adjust V. above the start threshold before setting at 15 V.

6. Output frequency equals oscillator frequency for the UC1842 and UC1843

Output frequency is one half oscillator frequency for the UC1844 and UC1845

Figure 1 : Error Amp Configuration.

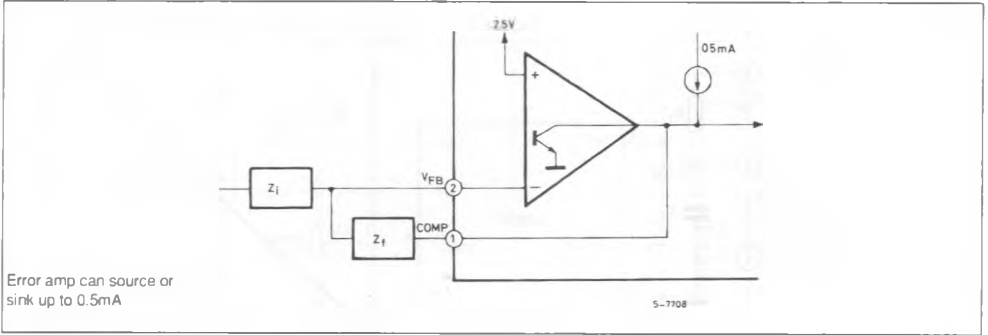
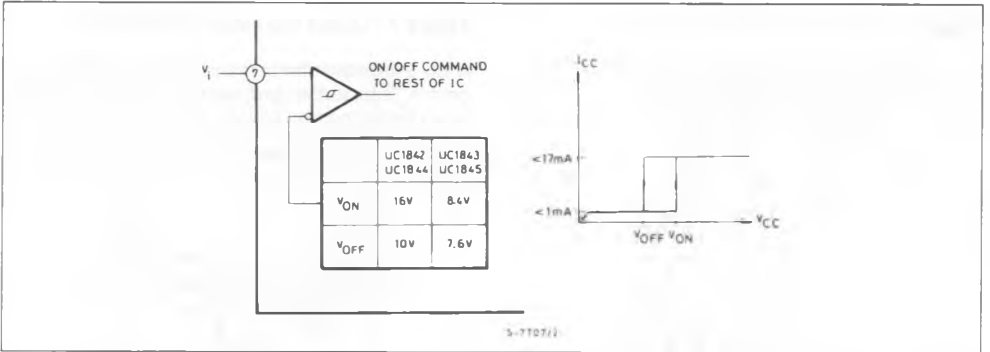


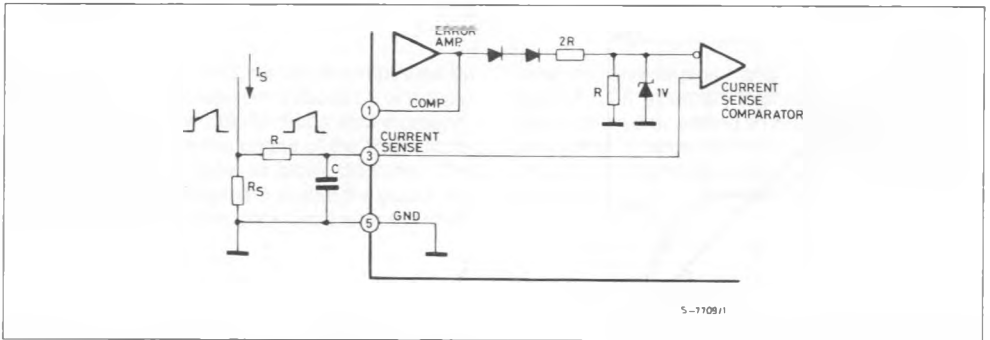
Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor

to prevent activating the power switch with extra-aneous leakage currents.

Figure 3 : Current Sense Circuit .



PEAK CURRENT ( $I_S$ ) IS DETERMINED BY THE FORMULA

$$I_{S \max} \sim \frac{1.0 \text{ V}}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

Figure 4.

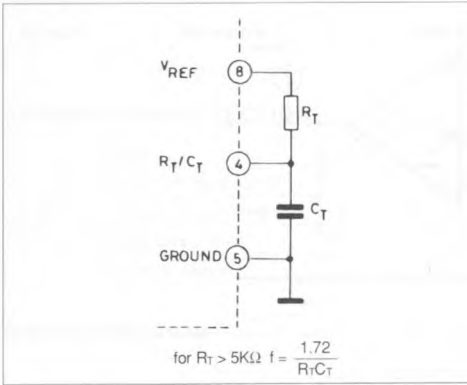


Figure 5 : Deadtime vs.  $C_T$  ( $R_T > 5K\Omega$ ).

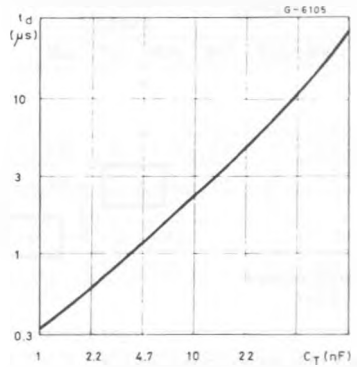


Figure 6 : Timing Resistance vs. Frequency.

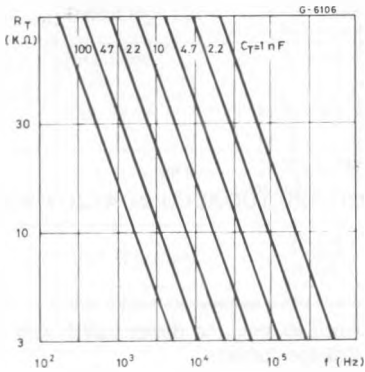


Figure 7 : Output Saturation Characteristics.

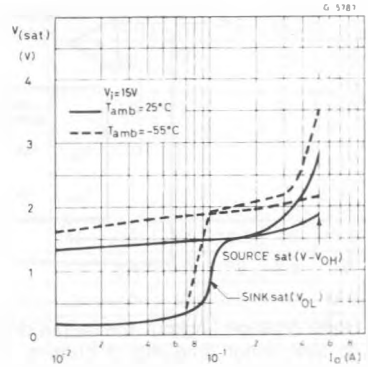


Figure 8 : Error Amplifier Open-loop Frequency Response.

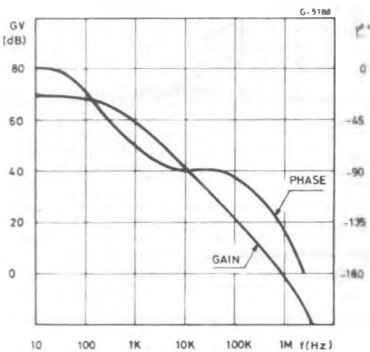
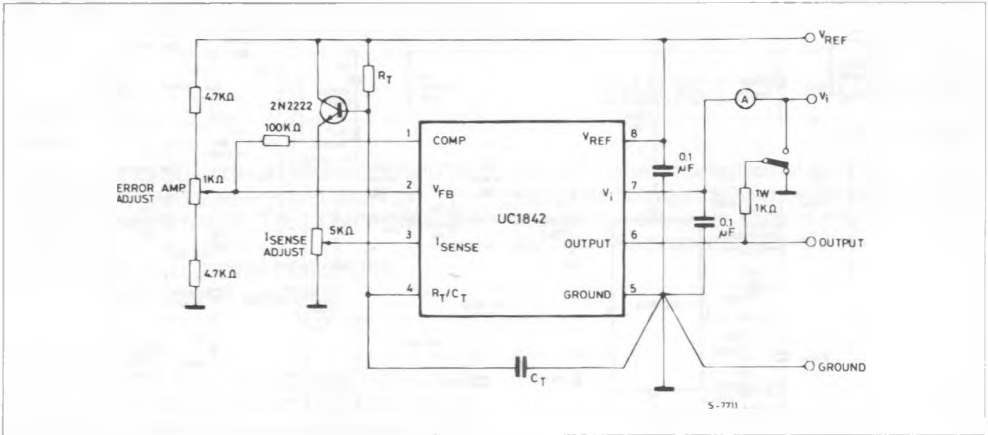


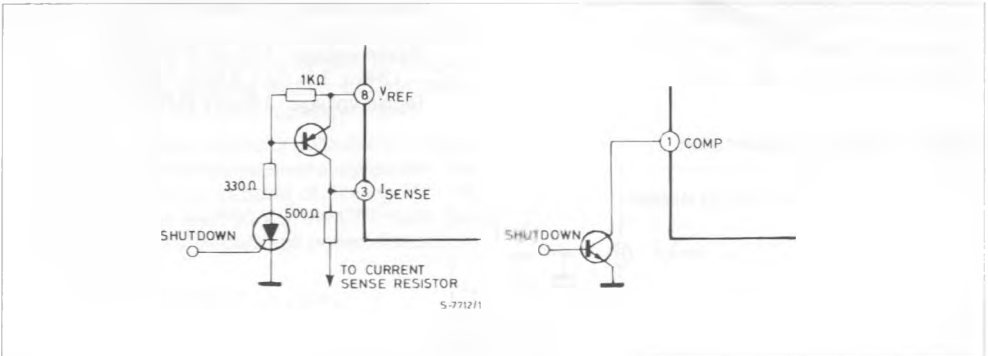
Figure 9 : Open Loop Test Circuit.



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close

to pin 5 in a single point ground. The transistor and 5 K $\Omega$  potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10 : Shutdown Techniques.



Shutdown of the UC1842 can be accomplished by two methods : either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shut-

down condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling  $V_i$  below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

