10-Bit Serial D/A Converter

FEATURES

- 10 Bit Resolution
- 1.1µs Output Rise Time
- 2.5µs Settling Time to 1%
- Single +5V Supply
- Monotonic
- Low Power Sleep Mode
- Three-wire Serial Interface
- 20MHz Data Rate
- 8 Pin SOIC and DIL Package

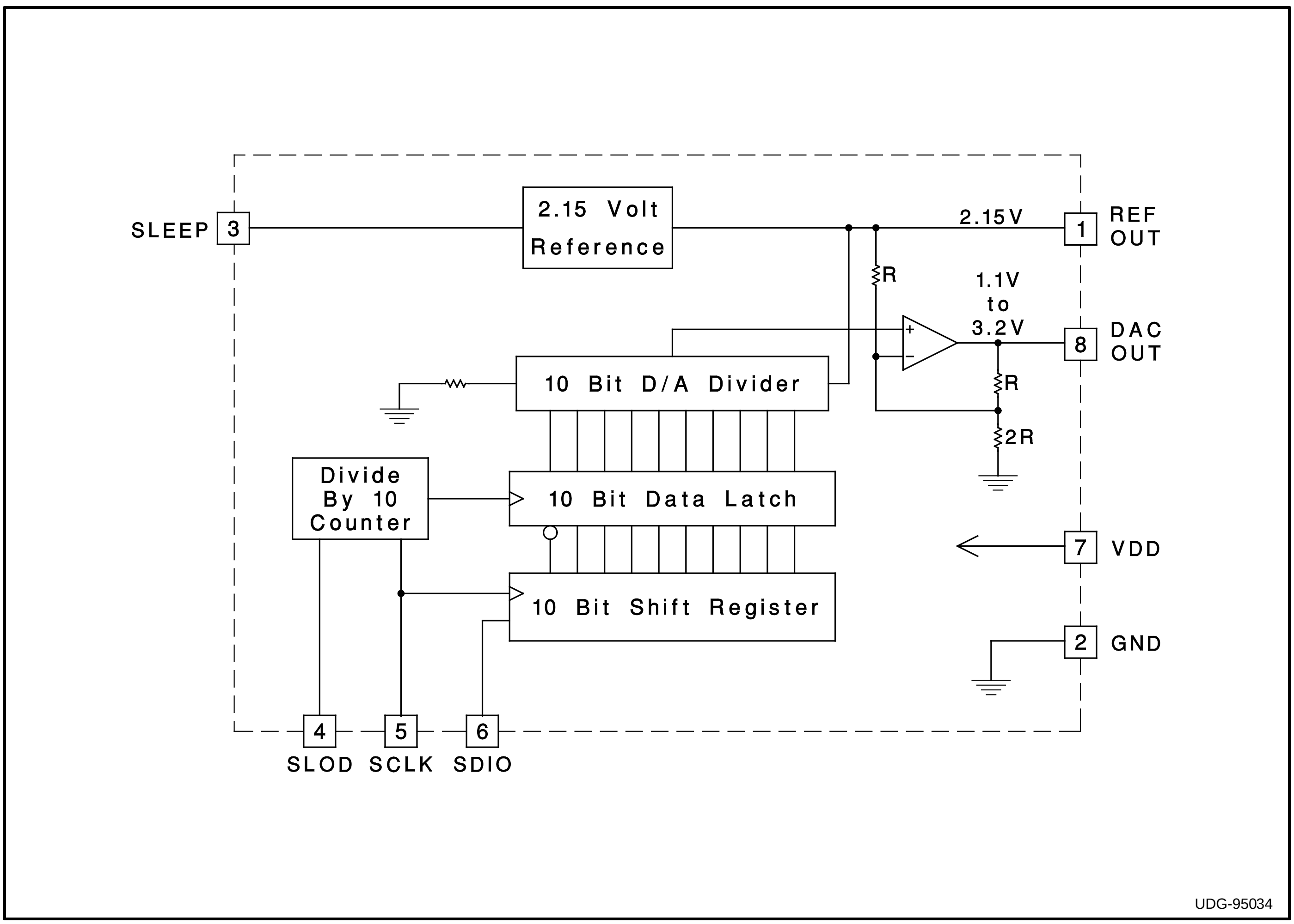
DESCRIPTION

The UCC5950 is a self-contained, microprocessor-compatible 10-bit D/A converter. It contains all of the functions required to take data directly from a three-wire serial data bus and convert it to a precise voltage, including: an input shift register, data latches, a precision voltage reference, a precision 10-bit digital to analog converter, and an output buffer amplifier.

The serial data interface is capable of clock frequencies as high as 20MHz, allowing update rates as high as two words per microsecond. The UCC5950 accepts commands encoded as 2's-complement binary.

The data converter in the UCC5950 is inherently monotonic, making this part ideal for use in closed-loop servo control systems as well as open-loop data conversion. The UCC5950 uses a unique segmented data converter which offers differential linearity better than 1 LSB, integral linearity better than 2 LSB, and fast conversion.

BLOCK DIAGRAM



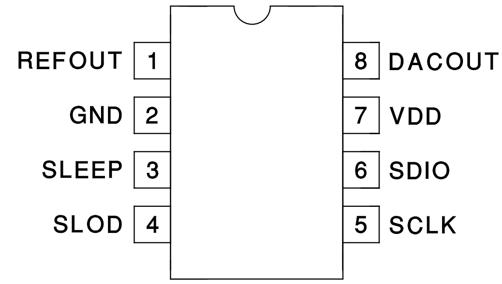
ABSOLUTE MAXIMUM RATINGS

VDD Supply Voltage 6.5V
Input Voltage, Any Input . . . . –0.3V to VDD+0.3V
Output Current, Any Output . . . . ±5mA
Operating Temperature . . . . –55°C to +150°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature . . . . 300°C

All voltages with respect to GND. All currents are positive into, negative out of, the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package

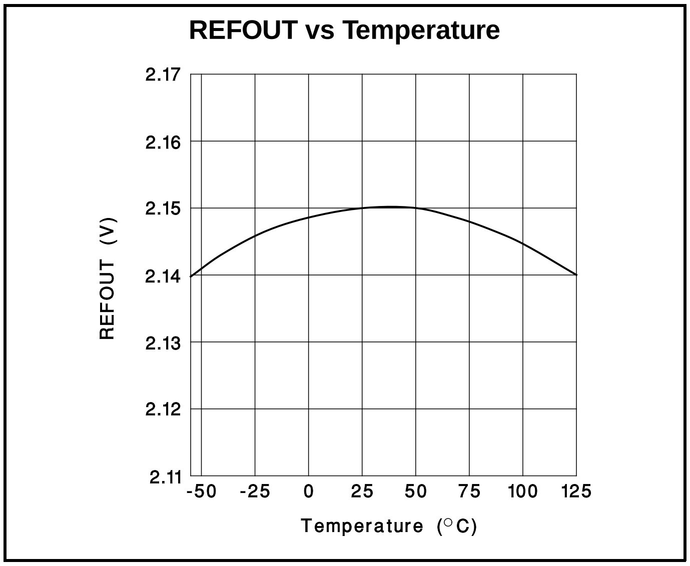


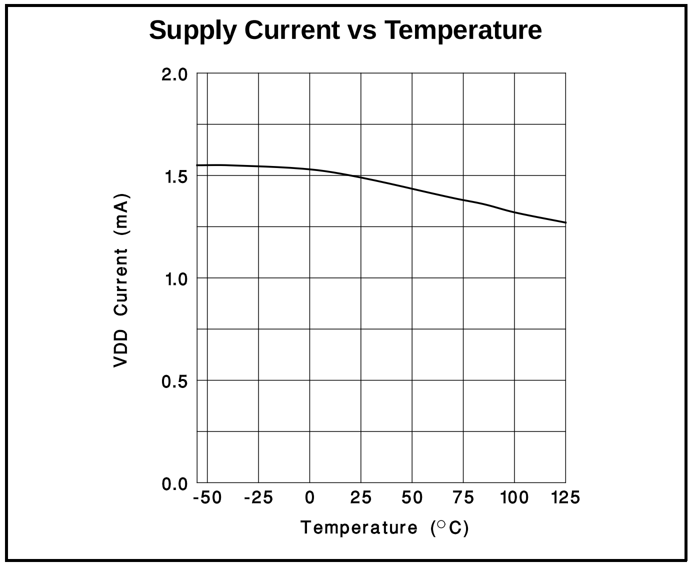
ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for 4.5V < VDD < 5.5V, REFOUT Load < 100pF, DACOUT Load < 100pF, 0°C < T_A < +70°C, and T_A = T_J.

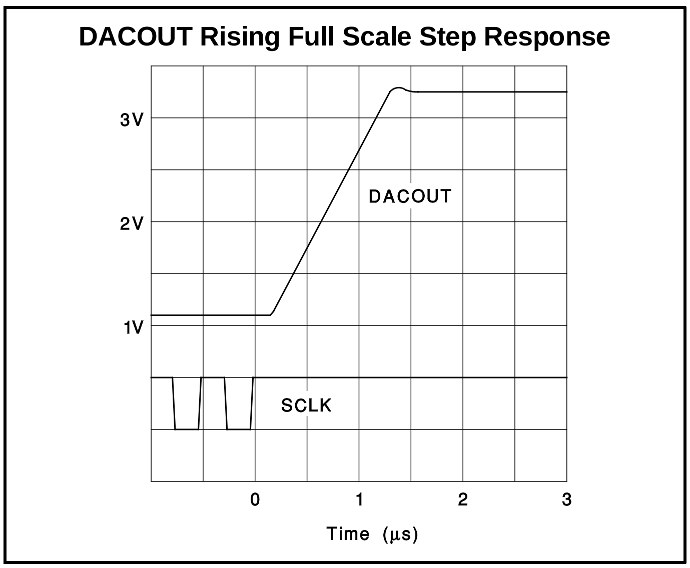
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
OVERALL SECTION					
Supply Current	SLEEP = 0V		1.5	5	mA
Supply Current	SLEEP = 5V		0.1	10	µA
REFERENCE SECTION					
REFOUT Output Voltage		2.10	2.15	2.20	V
REFOUT Change with VDD	4.5V < VDD < 5.5V		1	10	mV
REFOUT Change with Load	–1mA < I_{REFOUT} < 1mA		1	10	mV
D/A SECTION					
Integral Nonlinearity	(Note 1)			2	LSB
Differential Nonlinearity				1	LSB
Full Scale Difference from 1.4924 x REF		–8		8	LSB
Zero Scale Difference from 0.5089 x REF		–8		8	LSB
DACOUT Full Scale Rise/Fall Time	From 10% to 90% of swing (Note 4)		0.7	1.1	µs
DACOUT Full Scale Settling Time (TS)	(Note 2, 3, 4)		1.4	2.5	µs
DACOUT Change with VDD	4.5V < VDD < 5.5V		1.5	10	mV
DACOUT Change with Load	–1mA < I_{DACOUT} < 1mA		1.2	10	mV
LOGIC SECTION					
Logic Input Threshold		1.5	2.5	3.5	V
Logic Input Current	0V < V_{IN} < VDD			5	µA
Logic Input Capacitance	(Note 4)		2.7	10	pF
SLOD Setup Time to SCLK low (TSLS)	(Note 4)	50			ns
SLOD Hold Time from SCLK high (TSLH)	From 10^{TH} SCLK high (Note 4)	50			ns
SDIO Setup Time to SCLK high (TDS)	(Note 4)	15			ns
SDIO Hold Time from SCLK high (TDH)	(Note 4)	7			ns

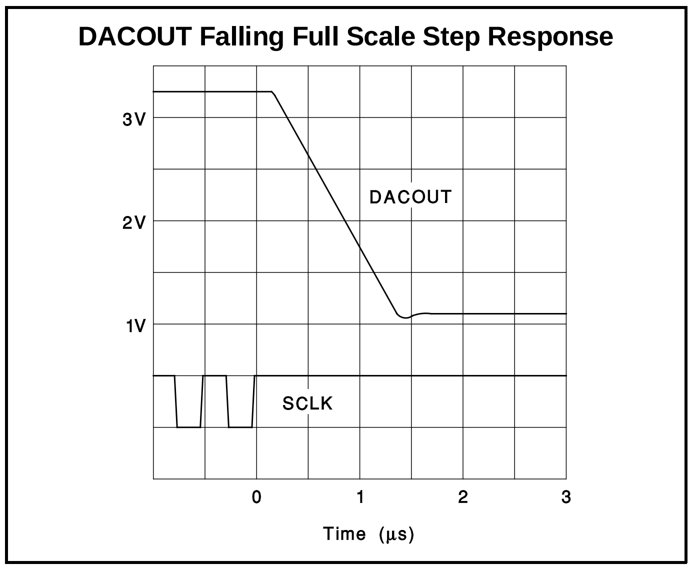
Note 1: Integral nonlinearity is defined as the worst deviation of the converter output from the best-fit straight line through all converter output codes.
Note 2: From 10^{TH} Rising Edge of SCLK.
Note 3: Settling time is to 1% of final value.
Note 4: Guaranteed by design. Not 100% tested in production.

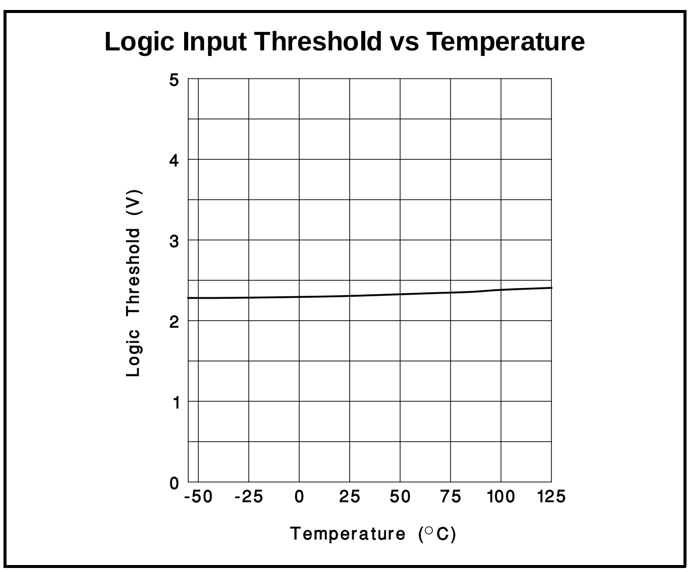
TYPICAL CHARACTERISTICS

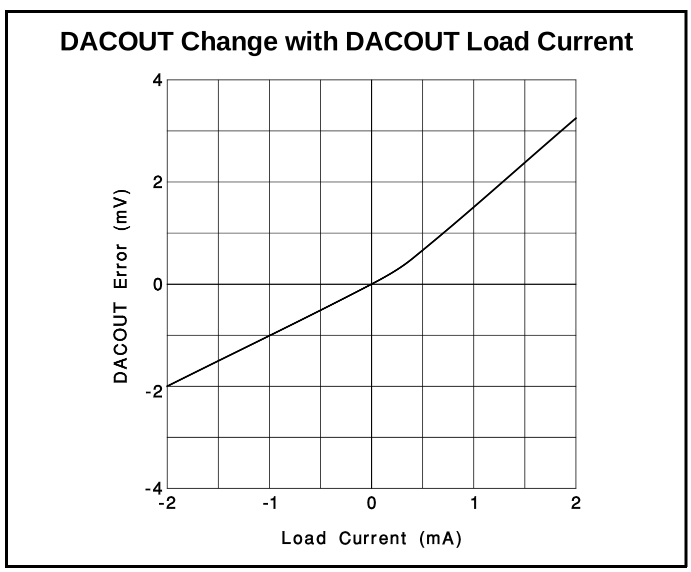












PIN DESCRIPTIONS

DACOUT: The output of the 10-bit D/A Converter. For best settling time, minimize load capacitance.

DACOUT will go to a voltage between 1.094V and 3.208V depending on the digital code loaded into the latches. The digital code follows this pattern:

Input Code	Typical DACOUT	Significance
1000000000	1.094V	Zero Scale
1000000001	1.096V	
1000000010	1.098V	
...		
1111111111	2.151V	
0000000000	2.153V	Mid Scale
0000000001	2.155V	
...		
0111111110	3.206V	
0111111111	3.208V	Full Scale

GND: All signals are referenced to GND.

REFOUT: The output of the temperature-compensated 2.15V reference. *DO NOT BYPASS REFOUT!* For best stability and transient response, minimize capacitance on REFOUT.

SCLK: Data is clocked into the D/A after SLOD goes low on rising edges of SCLK. After 10 rising edges of SCLK, the data is latched into the D/A output register and the output is updated. Further clock signals on SCLK are ignored until SLOD initiates a new read cycle.

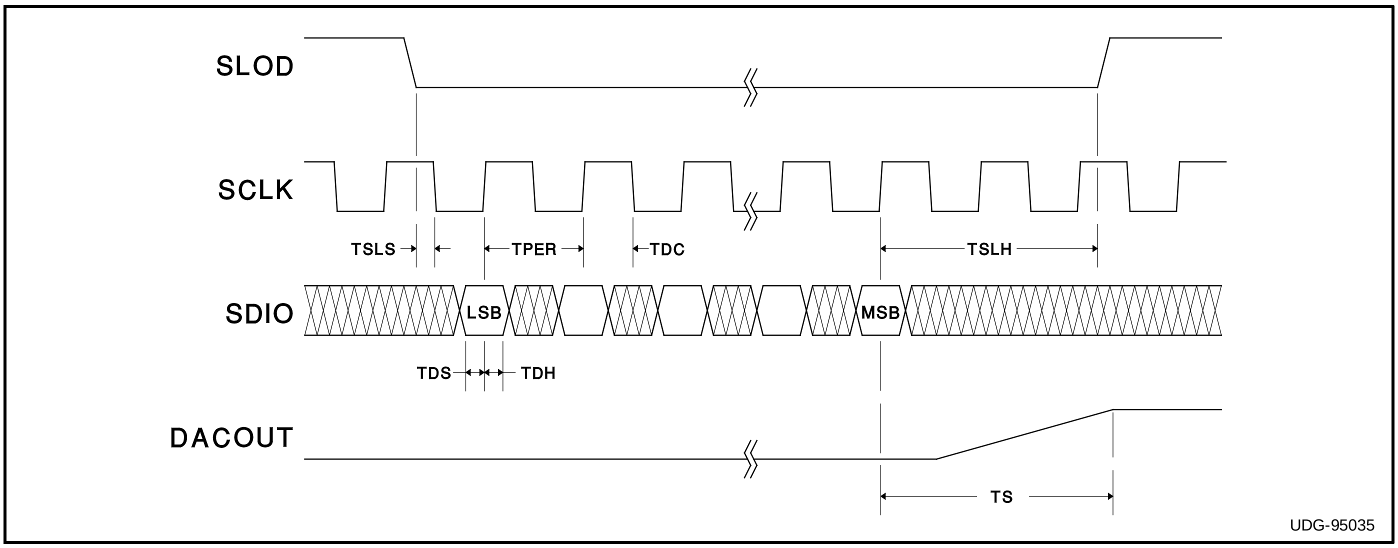
SDIO: After SLOD goes low, data is clocked into the D/A from the SDIO input, on rising edges of SCLK, LSB first. After 10 rising edges, data is latched and converted, and further SCLK and SDIO information is ignored.

SLEEP: SLEEP is the power-down input to the D/A. In systems not requiring this function, wire SLEEP to GND.

SLOD: SLOD is the chip-select input to the UCC5950. SLOD going low selects the D/A and enables clocking of data from SDIO into the D/A. After 10 SCLK pulses, the D/A is updated and SLOD is ignored until SLOD goes high and again goes low.

VDD: All analog and digital functions are powered from VDD. VDD should be a well-regulated supply to minimize output variations. Bypass VDD to GND with a ceramic capacitor very close to the UCC5950.

SERIAL DATA INTERFACE TIMING AND LOGIC TABLE



SLOD	Internal Flag	SCLK	SDIO	Internal Count	Action	DACOUT
1	1	*don't care*	*don't care*	0	*no action*	V(t)
0	0	rising edge	DATA	<10	Shift In DATA	V(t)
0	0	rising edge	DATA	10	Latch New DATA Set Internal Flag Reset Count	V(t+1)
0	1	*don't care*	*don't care*	0	*no action*	V(t)

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IMPORTANT NOTICE