UM82152

Cache Controller

ADVANCED PRODUCT DESCRIPTION

Features

- Controls 32-kB, 4-way, set-associative cache
- Available in 16-MHz, 20-MHz, and 25-MHz speeds
- Direct interface to the 80386
- Direct interface to industry-standard 8K x 8 SRAMs:
  45 ns for 16-MHz systems
  35 ns for 20-MHz systems
  25 ns for 25-MHz systems
- Full 32-bit addressability for 4-GB memory support
- Cache coherency support
- Software cache invalidation
- On-chip programmable noncached regions
- Write buffer support
- Gate A20 support
- 1.5 micron CMOS technology
- 84-lead PLCC, JEDEC standard package
- Pin and functionally identical to A38152*

General Description

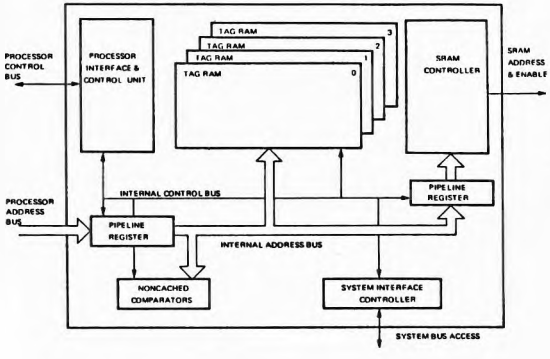
The UM82152 is a high-performance cache controller for Intel 80386 based systems and provides high levels of integration and functionality. It interfaces directly to the 80386; no additional support logic is required. A complete 32-kilobyte cache can be designed with just one UM82152 and four 8K by 8-bit static RAMs.

The UM82152 architecture enables easy design-in with current speed versions of the 80386, and simple migration to faster version processors with no alteration to system or memory design.

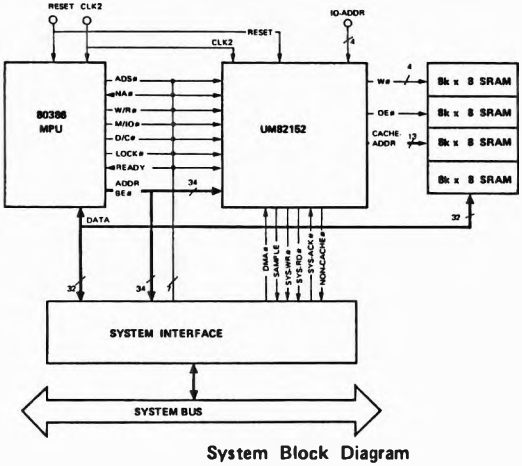
The 80386, operating in pipelined mode with the UM82152, runs with zero wait states during a cache hit (requested data is present in cache). If the data is not present (cache miss), it is fetched from main memory by the UM82152. This approach yields the high-speed performance of fast SRAMs for code and data most frequently used, while providing design economies (such as board space savings and lower component costs) by storing infrequently used code and data in slower dynamic RAM (with cycle times greater than 125 nanoseconds) that can be located in large memory banks either on-board or off-board.

The reduced system bus traffic inherent in the UM82152 implementation produces system performance gains by freeing the bus for use by other devices.

Block Diagrams



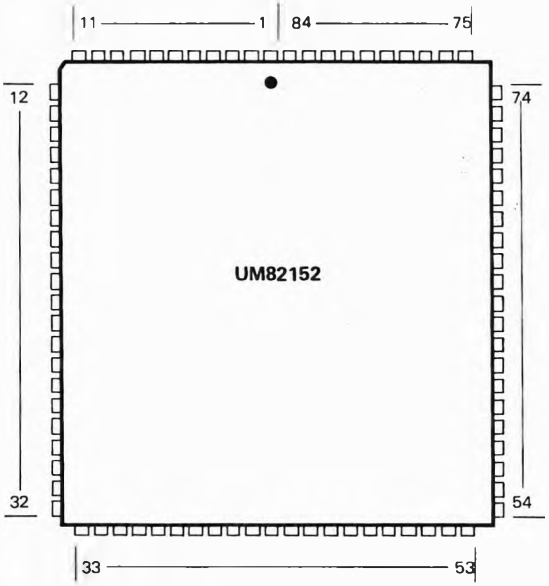
UM82152 Internal Configuration



System Block Diagram

*A38152 is Austek's cache controller for 25 MHz 386 AT system.

Pin Configuration



Pin No	Signal	Pin No	Signal	Pin No	Signal
1	GND	29	CACHE-ADDR10	57	ADDR16
2	ADDR2	30	CACHE-ADDR9	58	ADDR17
3	BE0#	31	CACHE-ADDR8	59	ADDR18
4	BE1#	32	CACHE-ADDR7	60	ADDR19
5	BE2#	33	GND	61	ADDR20
6	BE3#	34	ADDR12	62	ADDR21
7	W/R#	35	ADDR11	63	ADDR22
8	CACHE-ADDR6	36	ADDR10	64	GND
9	CACHE-ADDR5	37	ADDR9	65	ADDR23
10	CACHE-ADDR4	38	ADDR8	66	ADDR24
11	CACHE-ADDR3	39	ADDR7	67	ADDR25
12	CACHE-ADDR2	40	ADS#	68	ADDR26
13	GND	41	V_{CC}	69	ADDR27
14	SYS-WR#	42	CLK2	70	ADDR28
15	SYS-RD#	43	GND	71	ADDR29
16	V_{CC}	44	V_{CC}	72	ADDR30
17	SYS-ACK#	45	RESET	73	ADDR31
18	OE#	46	SAMPLE	74	IO-ADDR3
19	W3#	47	NON-CACHE#	75	V_{CC}
20	W2#	48	NA#	76	IO-ADDR2
21	W1#	49	LOCK#	77	IO-ADDR1
22	W0#	50	DMA#	78	IO-ADDR0
23	CACHE-ADDR1	51	READY#	79	D/C#
24	CACHE-ADDR0	52	CACHE-FAULT	80	M/IO#
25	GND	53	ADDR13	81	ADDR6
26	CACHE-ADDR12	54	V_{CC}	82	ADDR5
27	V_{CC}	55	ADDR14	83	ADDR4
28	CACHE-ADDR11	56	ADDR15	84	ADDR3

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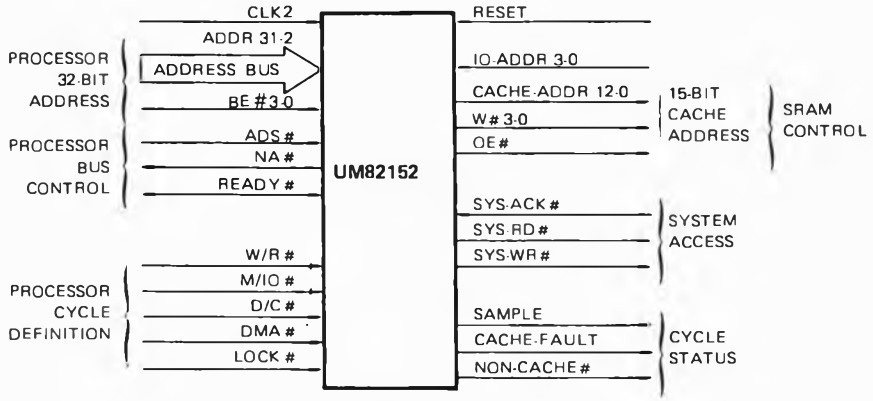

UM82152 Signals

Pin Description

Pin No.	Symbol	I/O	Description
42	CLK2	I	**Clock.** Clock input.
45	RESET	I	**Reset.** Resets the microcache to a known state.
74, 76~78	IO-ADDR	I	**Chip I/O Address.** Address pins to locate the controller in the I/O space of the CPU.
2, 34~39, 53, 55~63, 65~73, 81~84	ADDR	I	**Address Bus.** The 30 physical address pins from the CPU.
3~6	BE#	I	**Byte Enable.** The 4 byte-enable pins from the CPU.
40	ADS#	I	**Address Status.** Direct connection from the CPU. Initiates a valid bus cycle.
48	NA#	O	**Next Address.** Direct connection to the CPU. Requests the CPU to use address pipelining.
51	READY#	I/O	**Ready** Direct to the CPU. Indicates completion of the current bus cycle. This signal is bidirectional as it will also be driven by the system interface.
7	W/R#	I	**Write/Read.** Direct connection from the CPU. Indicates the type of CPU bus cycle, either write or read.
80	M/IO#	I	**Memory/Input, Output.** Direct connection from the CPU. Indicates the type of CPU bus cycle, either memory or I/O.
79	D/C#	I	**Data/Control.** Direct connection from the CPU. Indicates the type of CPU bus cycle, either data or control.
50	DMA#	I	**DMA Cycle.** Indicates that the cycle occurring is due to DMA activity on the system bus. Cache coherency is maintained by clearing any matching entries from the cache.
49	LOCK#	I	**Lock.** Direct connection from the CPU. When asserted indicates the current cycle is locked, exclusive access must be granted to the memory location addressed until LOCK# is negated. For cache coherency reasons, any matching entries are cleared from the cache.
17	SYS-ACK#	I	**System Transfer Acknowledge.**Control input from the system interface to acknowledge completion of read and write transfers to the system.
15	SYS-RD#	O	**System Read.** Control output to the system interface initiating a main memory read.
14	SYS-WR#	O	**System Write.** Control output to the system interface initating a main memory read.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
46	SAMPLE	O	**Sample.** Control output to the system interface to latch address and status information describing a processor bus cycle. SAMPLE is strobed at the end of a Tstate where the A38152 is either in a Ti state or a T2P state (when READY# will be asserted).
52	CACHE-FAULT	O	**Cache Fault.** A request to the system for an interrupt due to an internal error.
47	NON-CACHE#	O	**Noncache Transfers.** Indicates a data access within a noncached region. External decoding of addresses must be performed if necessary.
8-12, 23, 24, 26, 28~32	CACHE-ADDR	O	**Cache Memory Address Bus.** The physical address pins to the cache RAMs.
19~22	W#	O	**Write Enable.** Indicates a write to the cache RAMS when asserted and a read when negated. There is a W# line for cach byte in a word.
18	OE#	O	**Output Enable.** The data output enable for the cache RAMs.
16, 27, 41, 44 54, 75	V_{CC}		+5 Volt
1, 13, 25, 33 43, 64	GND		Ground