UM83C004

Hard Disk Controller Interface

ADVANCED PRODUCT DESCRIPTION

Features

- Interfaces to PC XT systems with Hard-Disk controller
- I/O channel ready signal generator (generates wait state)
- Clock generator
- Sector buffer RAM addressing and control
- Data bus drives directly to slot.
- 68-pin PLCC package.
- Supports RLL/MFM Disk Controller

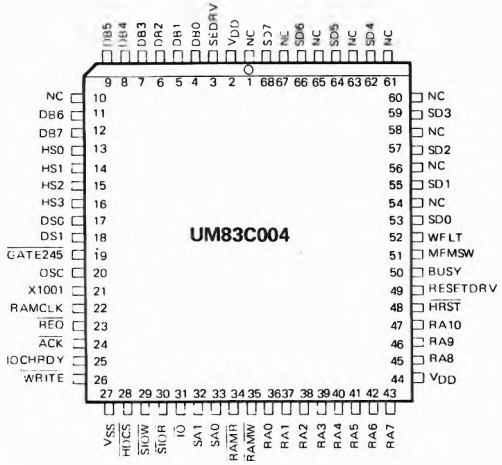
General Description

The UM83C004 incorporates several functions in a single package. Implementation of these functions occurs by combining random logic. The UM83C004 contains the following circuits:

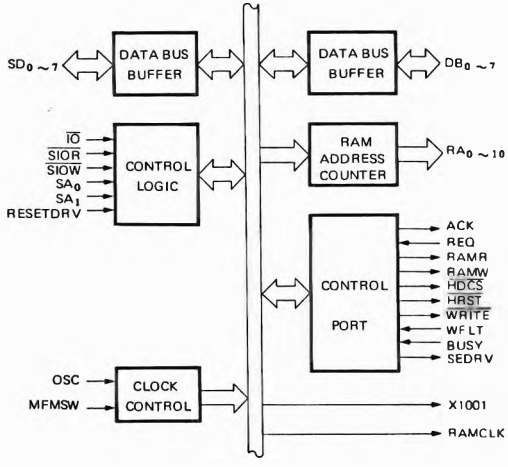
Clock Generator
Sector Buffer RAM Addressing and Control
Data Bus Interface Control
HDC Status & Control Port

The UM83C004 connects directly to the Host interface Data/Command and intraboard Command/Data buses.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to + 7V
All Input Voltages . . . . . −0.5 to + 7V
Supply Voltage V_{CC} . . . . . −0.5 to + 7V
Power Dissipation 1W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 ~ 70°C)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0	–	V_{CC}	V
V_{IL}	Input Low Voltage	0	–	0.8	V
V_{OH}	Output High Voltage				
	I_{Load} = −6.4mA (SD_0 ~ SD_7)	2.4	–	–	V
	I_{Load} = −3.2mA (all others)	2.4	–	–	V
V_{OL}	Output Low Voltage				
	I_{Load} = 6.4mA (SD_0 ~ SD_7)	–	–	0.4	V
	I_{Load} = 3.2mA (all others)	–	–	0.4	V

A. C. Characteristics

Symbol	Item	Min.	Max.	Unit
t_1	Address hold time	10	–	ns
t_2	$\overline{RAMW}$ time delay	–	50	ns
t_3	$\overline{RAMW}$ low to data output	–	60	ns
t_4	Data hold time	–	15	ns
t_5	$\overline{RAMR}$ time delay	–	40	ns
t_6	$\overline{RAMR}$ low to data output	–	140	ns
t_7	$\overline{RAMR}$ high to data High Z	–	60	ns
t_8	OSC to X1001 delay time	–	50	ns
t_9	X1001 to RAMCLK delay time	–	25	ns

Capacitance

Parameter	Max.	Unit
Output Capacitance		
SD0 ~ SD7	50	pF
All others	20	pF

Pin Descriptions

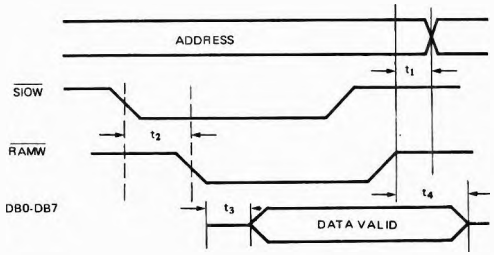
Pin No.	Symbol	I/O	Description
53, 55, 57 59, 62, 64, 66, 68	SD0-SD7	I/O	These lines provide data bus bit0-bit7 for system microprocessor.
4, 5, 6, 7 8, 9, 11, 12	DB0-DB7	I/O	These lines provide data bus bit0-bit7 for static RAM, & controller.
3	$\overline{\text{SEDRV}}$	I	This command line indicates selection of drive no, or drive head no. This signal is active low.
20	OSC	I	This signal is supported by the external oscillator. The working frequency is 30 MHz.
23 24	$\overline{\text{REQ}}$ $\overline{\text{ACK}}$	I O	These signal pins indicate that another master is requesting a local bus. The chip receiving the REQ will issue ACK as an acknowledgement in the RAM CLK clock cycle. These signals are active low.
29	$\overline{\text{SIOW}}$	I	This command line is an input control signal used by the CPU to load information into the chip. This signal is active low.
30	$\overline{\text{SIOR}}$	I	This command line is an input control signal used by the CPU to read the control signal. It is active low.
31	$\overline{\text{IO}}$	I	A "Low" on this chip enables the chip. No reading or writing will occur unless the chip is selected. This signal is active low.
33 32	SA0 SA1	I I	These inputs are normally connected to the address bus.
49	RESETDRV	I	A "High" on the input resets all control registers on the chip.
50	BUSY	I	BUSY is high when the operation is in process. The CPU can read the status of the controller used by this pin.
51	MFMSW	I	If the signal is high, it selects MFM code. Otherwise, it selects RLL code.
52	WFLT	I	When the drive encounters an error in process, it sends an error signal to the controller to indicate "Write fault". The CPU can read the error message of the controller used by this pin. It is active high.
13, 14, 15, 16	HS0, HS1 HS2, HS3	O	No. of the drive head. 16 heads are selected.
17, 18	DS0, DS1	O	No. of the disk. 4 disks are selected.
19	GATE245	O	This signal pin is optional. If the sink current of SD0-SD7 is not enough to drive the system data bus, the gate 74LS245 is directly connected by using this pin.
21	X1001	O	When MFMSW is high, X1001 is OSC/3. Otherwise, X1001 is OSC/2.
22	RAMCLK	O	When MFMSW is high. RAMCLK is OSC/9. Otherwise, RAMCLK is OSC/6.
25	IOCHRDY	O	When this signal is active high, it may use this line during a write operation if more time is needed to store the data from the bus. It also holds the data long enough for the system microprocessor to sample.
26	$\overline{\text{WRITE}}$	O	This command line indicates that the UM83C001 chip fetches read or write operation. This signal is active low.
28	$\overline{\text{HDCS}}$	O	A "Low" on this input enables the UM83C001 chip. Noreading or writing will occur unless the UM83C001 chip is selected.

Pin Descriptions (Continued)

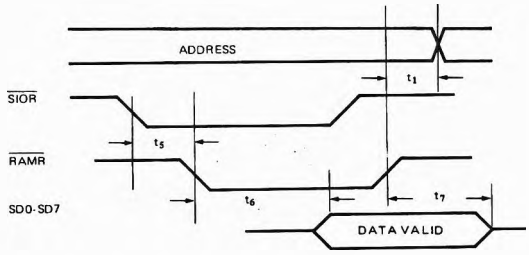
Pin No.	Symbol	I/O	Description
35	$\overline{RAMW}$	O	The command line indicates that the CPU loads information into static RAM. This signal is active low.
34	$\overline{RAMR}$	O	The command line indicates that the static RAM sends data to the data bus. This signal is active low.
48	$\overline{HRST}$	O	$\overline{HRST}$ is an active low output derived from the RESETDRV input.
36, 37, 38, 39, 40, 41, 42, 43, 45, 46, 47	RA0-RA10	O	The signals are connected to the static RAM address. The data in the static RAM is read or written by the controller.

Timing Waveforms

Write Cycle



Read Cycle



Clock Timing