

SWITCHING
 P-CHANNEL POWER MOS FET
 INDUSTRIAL USE

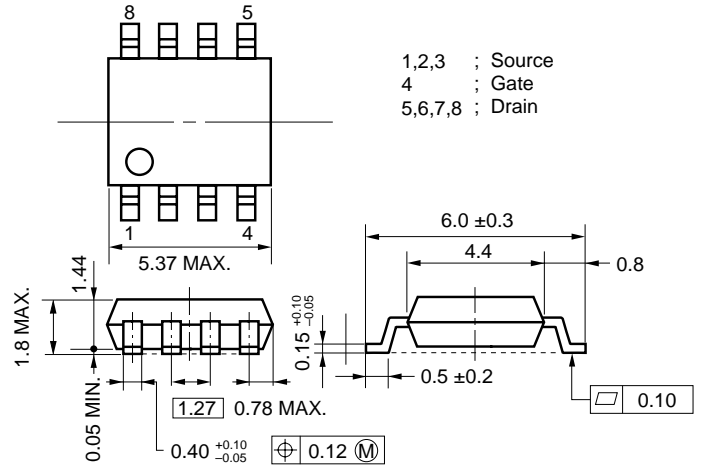
DESCRIPTION

The μ PA1717 is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 33 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -3 \text{ A)}$
 $R_{DS(on)2} = 59 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -3 \text{ A)}$
- Low C_{iss} : $C_{iss} = 830 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



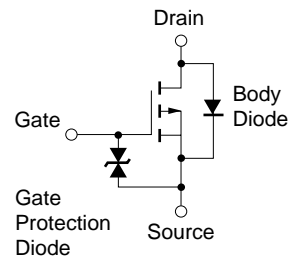
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1717G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 25	V
Drain Current (DC)	$I_{D(DC)}$	± 6	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 24	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

EQUIVALENT CIRCUIT



- Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$
 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

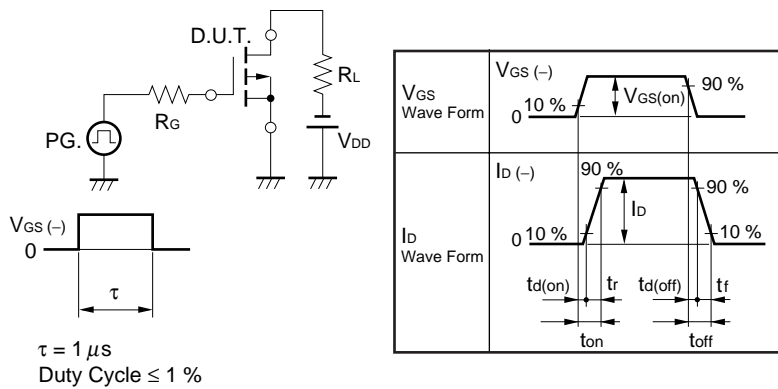
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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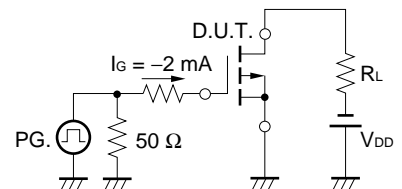
ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -3\text{ A}$		26	33	mΩ
	$R_{DS(on)2}$	$V_{GS} = -4.5\text{ V}, I_D = -3\text{ A}$		44	59	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -3\text{ A}$	3.0	7.5		S
Drain Leakage Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \mp 25\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$		830		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		330		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		130		pF
Turn-on Delay Time	$t_{d(on)}$	$I_D = -3\text{ A}$		15		ns
Rise Time	t_r	$V_{GS(on)} = -10\text{ V}$		120		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{DD} = -15\text{ V}$		70		ns
Fall Time	t_f	$R_G = 6\ \Omega$		50		ns
Total Gate Charge	Q_G	$I_D = -6\text{ A}$		15		nC
Gate to Source Charge	Q_{GS}	$V_{DD} = -24\text{ V}$		3		nC
Gate to Drain Charge	Q_{GD}	$V_{GS} = -10\text{ V}$		5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 6\text{ A}, V_{GS} = 0\text{ V}$		0.82		V
Reverse Recovery Time	t_{rr}	$I_F = 6\text{ A}, V_{GS} = 0\text{ V}$		35		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A} / \mu\text{s}$		15		nC

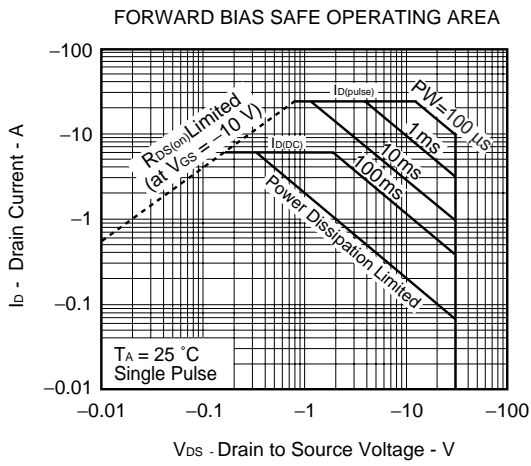
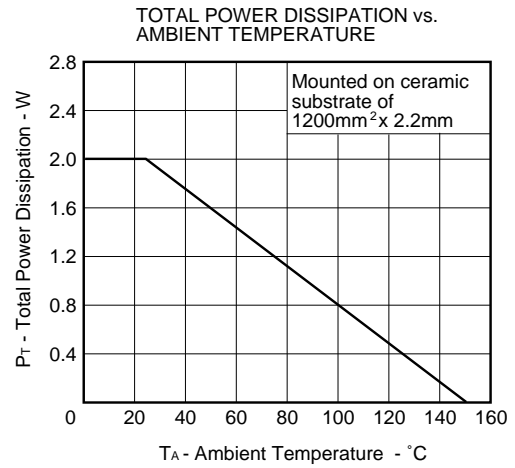
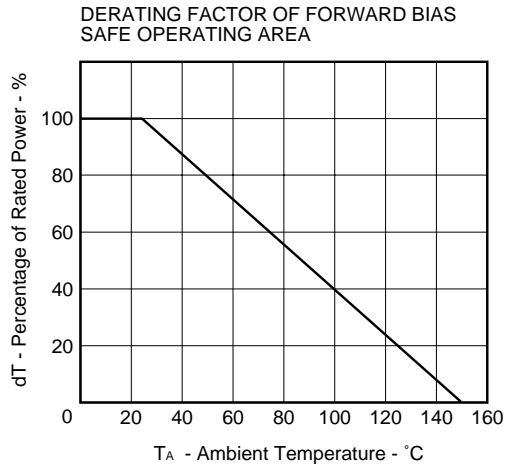
TEST CIRCUIT 1 SWITCHING TIME



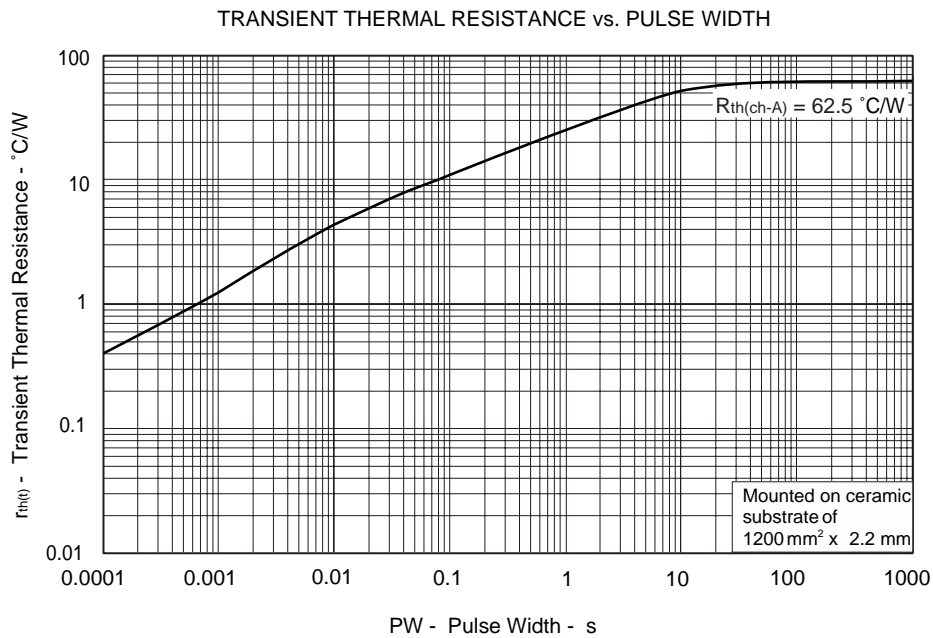
TEST CIRCUIT 2 GATE CHARGE

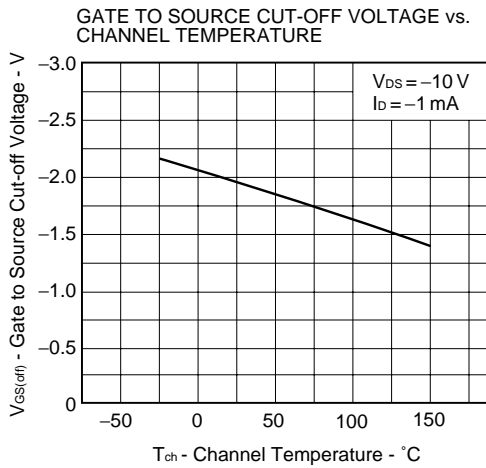
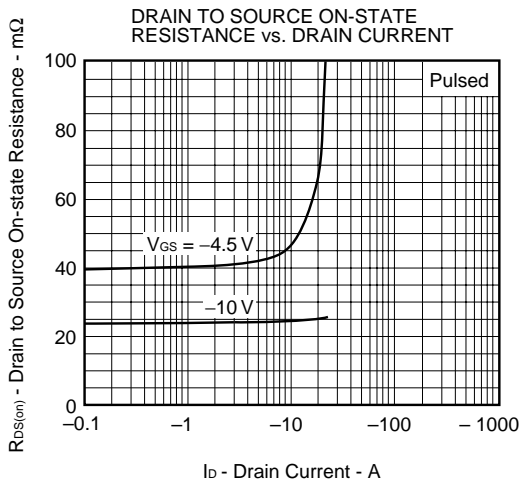
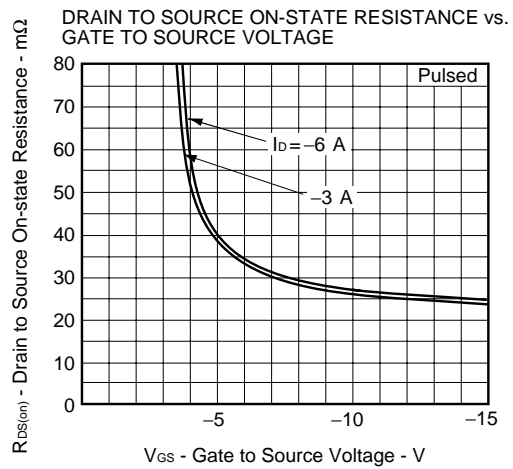
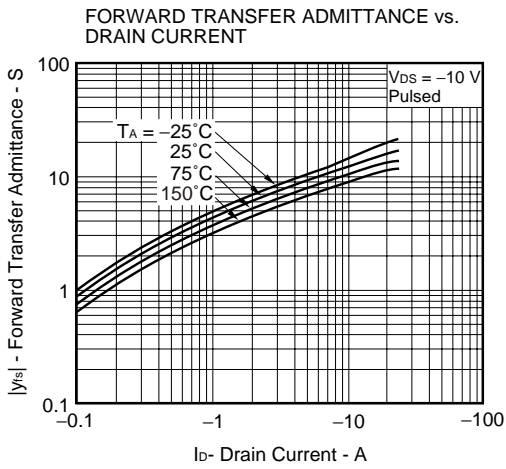
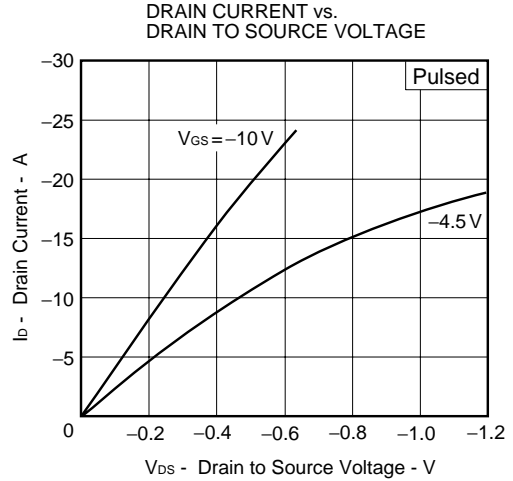
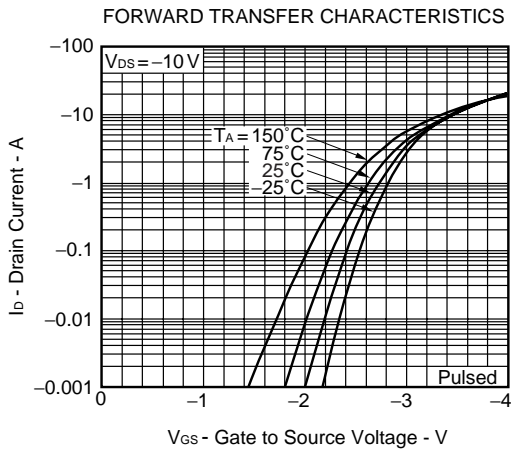


TYPICAL CHARACTERISTICS (T_A = 25 °C)

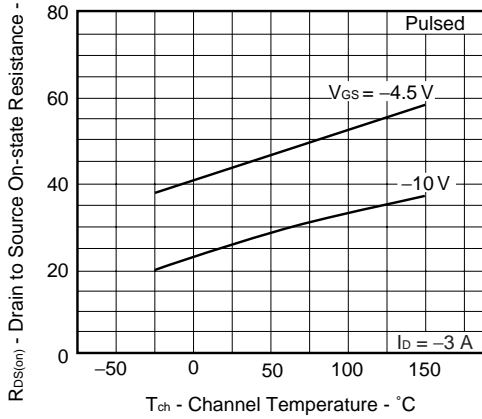


Remark Mounted on ceramic substrate of 1200 mm² x 2.2 mm

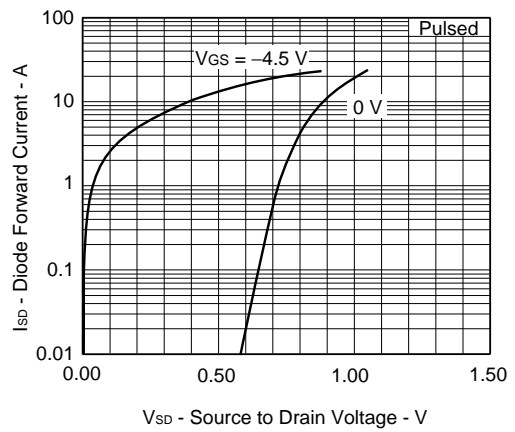




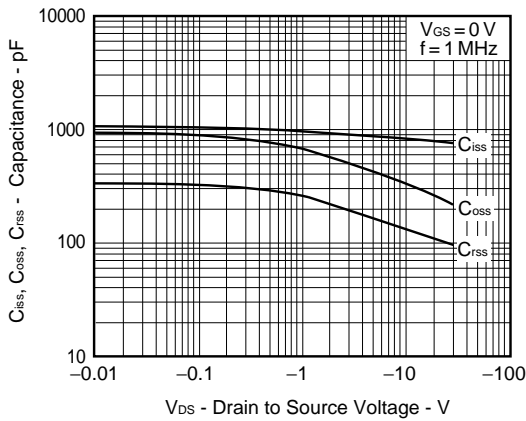
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



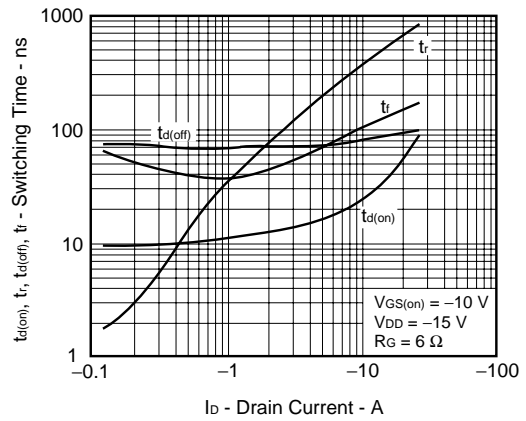
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



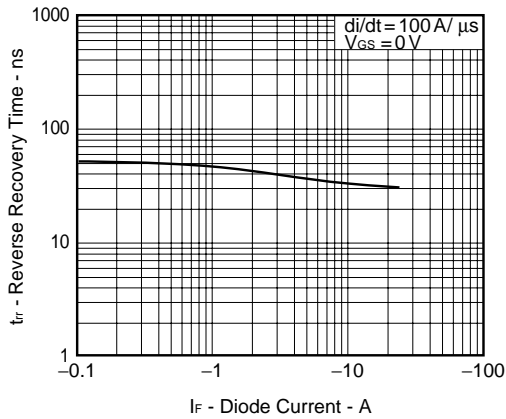
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



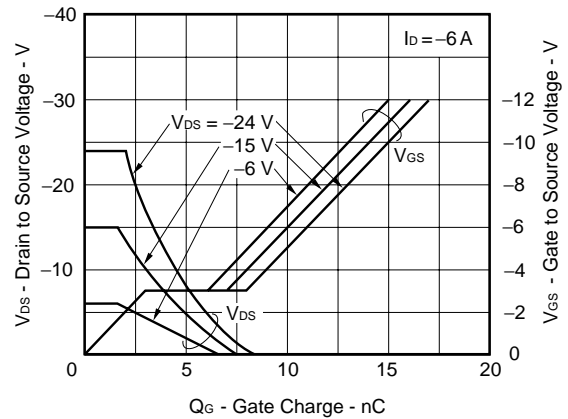
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

[MEMO]

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