NEC

# MOS FIELD EFFECT TRANSISTOR

# μPA1727

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

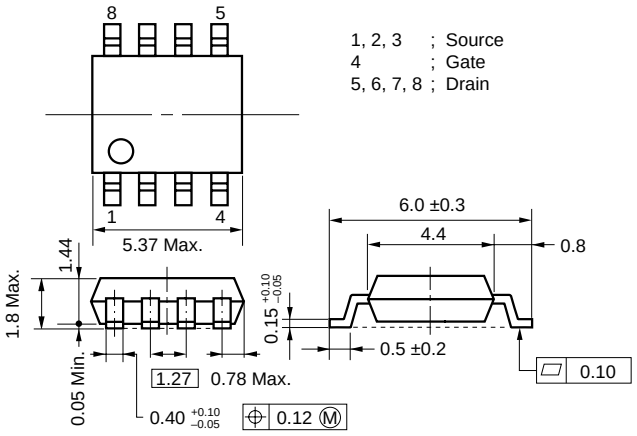
### DESCRIPTION

The μPA1727 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

### FEATURES

- Single chip type
- Low on-state resistance
  $R_{DS(on)1}$ = 14 mΩ TYP. ($V_{GS}$ = 10 V, $I_D$ = 5.0 A)
  $R_{DS(on)2}$ = 17 mΩ TYP. ($V_{GS}$ = 4.5 V, $I_D$ = 5.0 A)
  $R_{DS(on)3}$ = 19 mΩ TYP. ($V_{GS}$ = 4.0 V, $I_D$ = 5.0 A)
- Low $C_{iss}$ : $C_{iss}$ = 2400 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### PACKAGE DRAWING (Unit : mm)



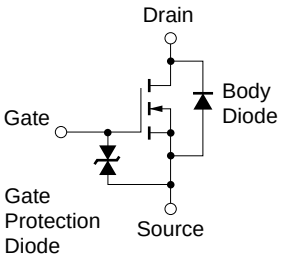

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| μPA1727 | Power SOP8 |

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, All terminals are connected.)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ±10 | A |
| Drain Current (Pulse) Note1 | $I_{D(pulse)}$ | ±40 | A |
| Total Power Dissipation ($T_A$ = 25°C) Note2 | $P_T$ | 2.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to + 150 | °C |
| Single Avalanche Current Note3 | $I_{AS}$ | 10 | A |
| Single Avalanche Energy Note3 | $E_{AS}$ | 200 | mJ |

### EQUIVALENT CIRCUIT




**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Mounted on ceramic substrate of 1200 $mm^2$ x 2.2 mm

**3.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = 30 V, $R_G$ = 25 Ω, $V_{GS}$ = 20 → 0 V

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



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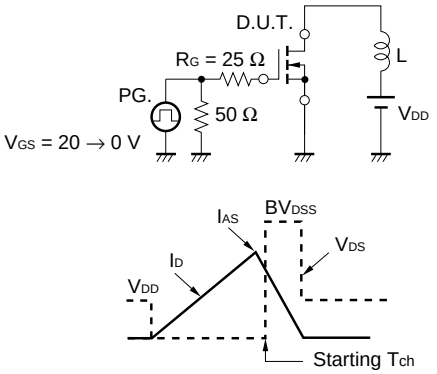
**The mark ★ shows major revised points.**

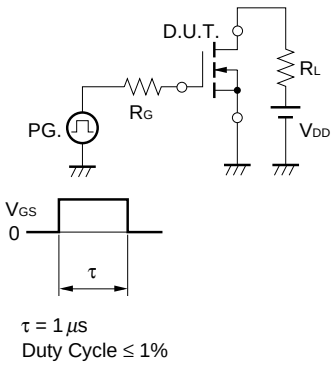
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C, All terminals are connected.)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Gate Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 1.5 | 2.0 | 2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 5.0 A | 8.0 | 14 | | S |
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 5.0 A | | 14 | 19 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4.5 V, $I_D$ = 5.0 A | | 17 | 22 | mΩ |
| | $R_{DS(on)3}$ | $V_{GS}$ = 4.0 V, $I_D$ = 5.0 A | | 19 | 25 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 2400 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 400 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 200 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $I_D$ = 5.0 A | | 24 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = 10 V | | 120 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 10 Ω | | 120 | | ns |
| Fall Time | $t_f$ | | | 70 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 48 V | | 45 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V | | 6 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 10 A | | 13 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 10 A, $V_{GS}$ = 0 V | | 0.8 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 10 A, $V_{GS}$ = 0 V | | 45 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100A/μs | | 84 | | nC |

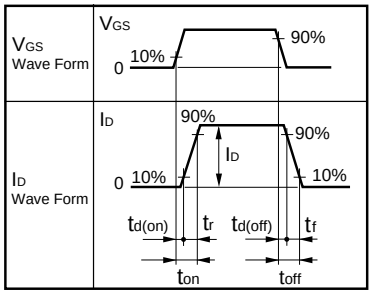
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



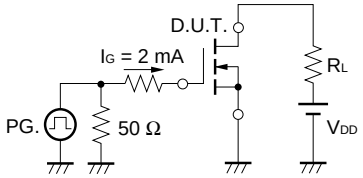

**TEST CIRCUIT 2 SWITCHING TIME**




τ = 1 μs
Duty Cycle ≤ 1%

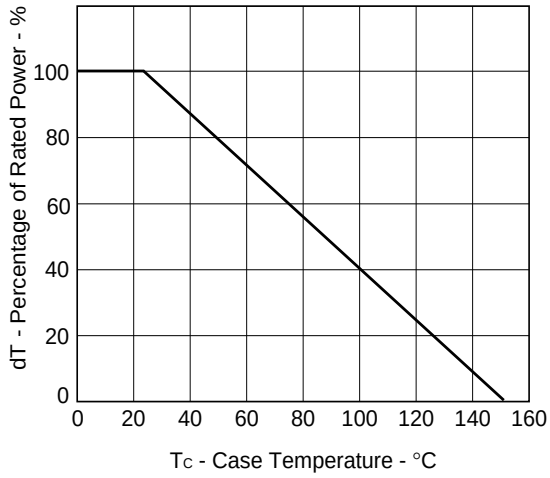



**TEST CIRCUIT 3 GATE CHARGE**

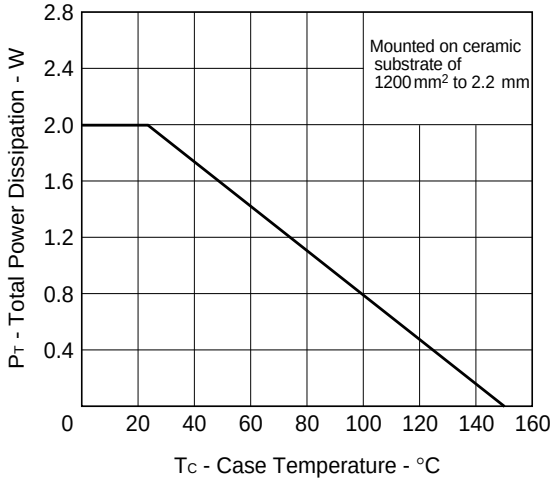


## ★ TYPICAL CHARACTERISTICS ($T_A$ = 25°C , All terminals are connected.)

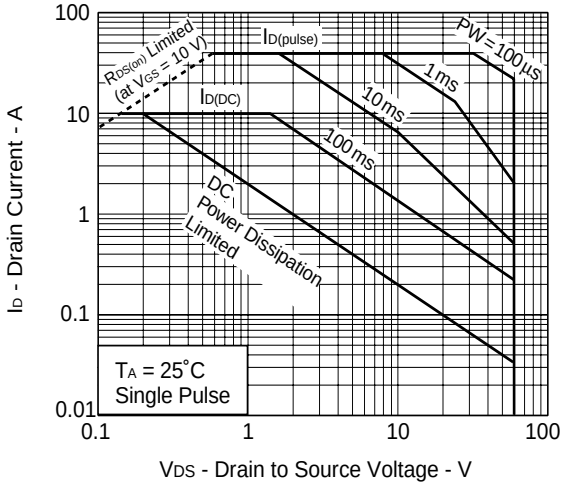
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA




TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

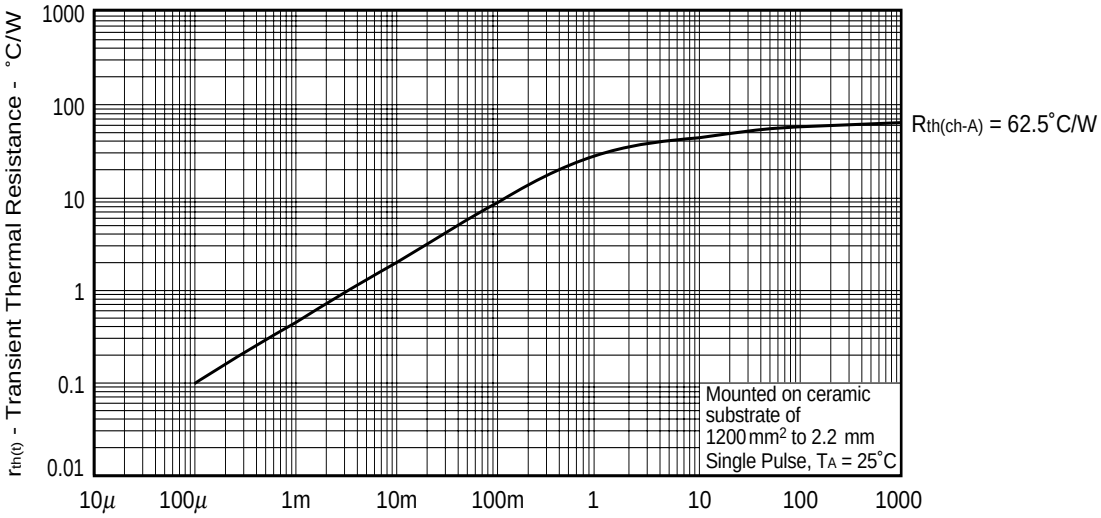



FORWARD BIAS SAFE OPERATING AREA

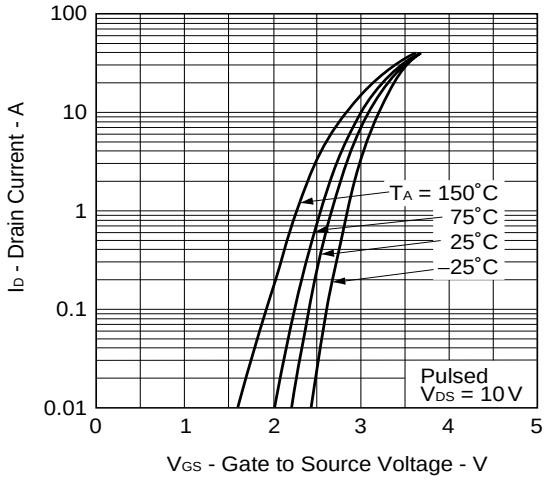



**Remark** Mounted on ceramic substrate of 1200 mm$^2$ × 2.2 mm

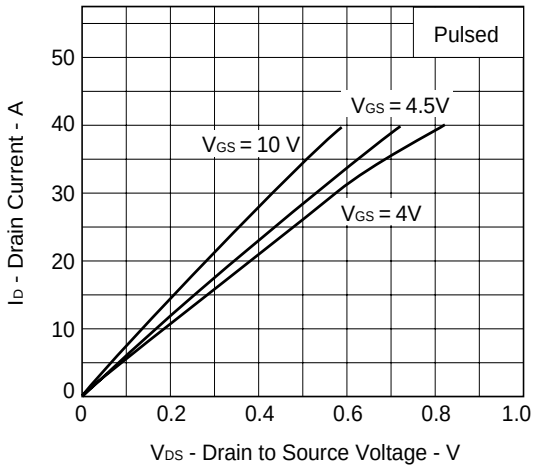
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



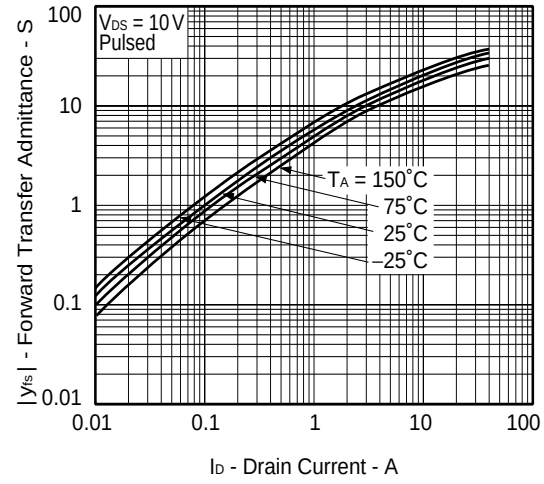
FORWARD TRANSFER CHARACTERISTICS



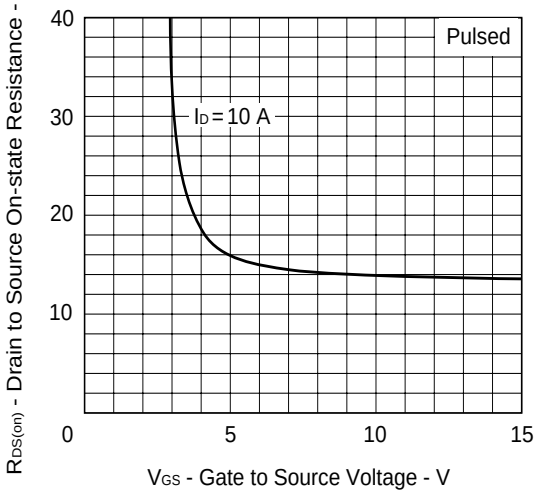

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



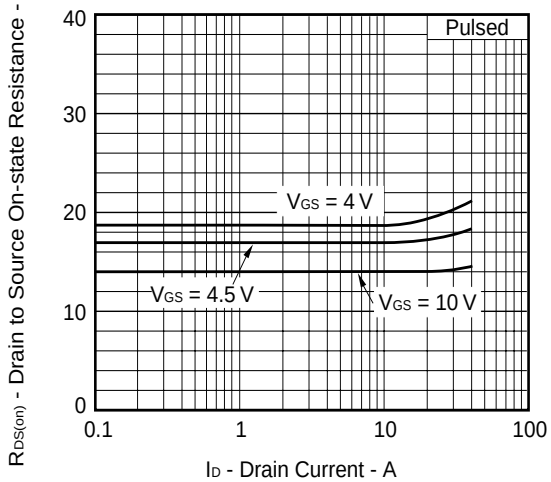

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



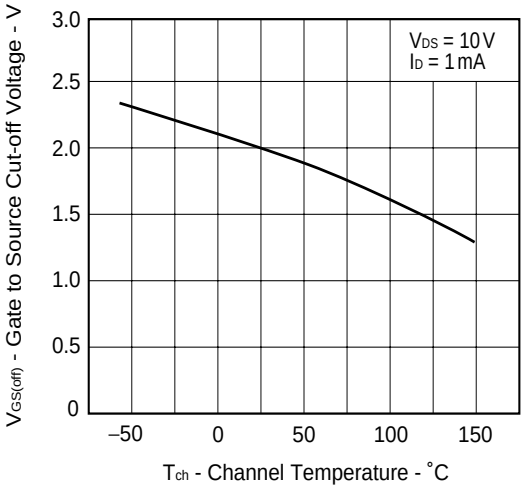

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



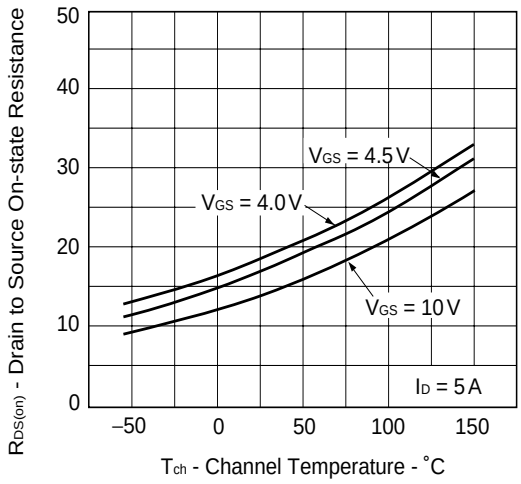

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



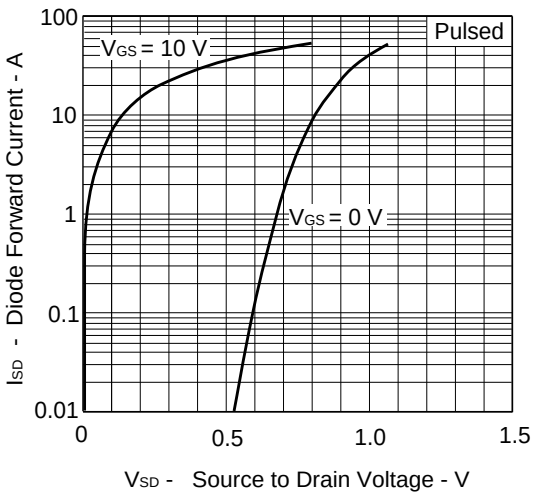

GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



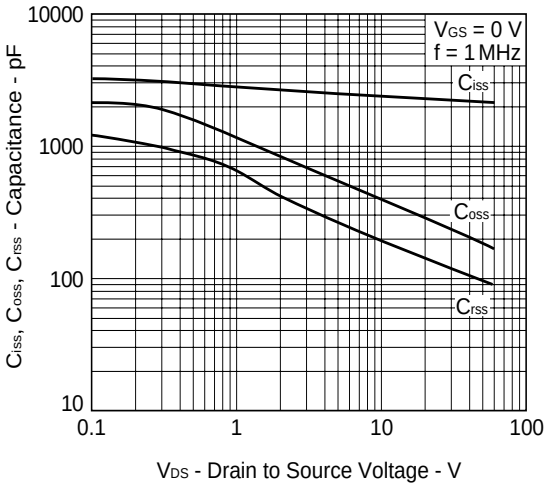
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



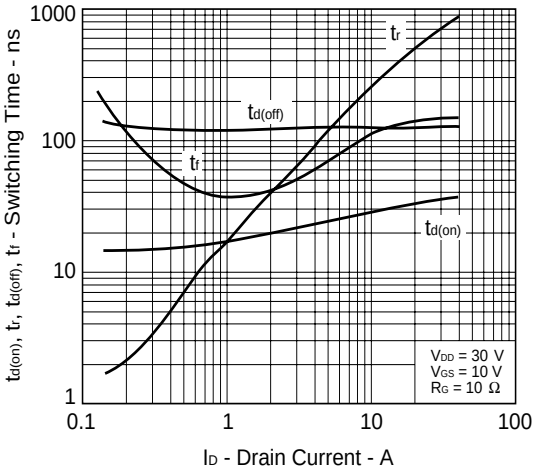

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



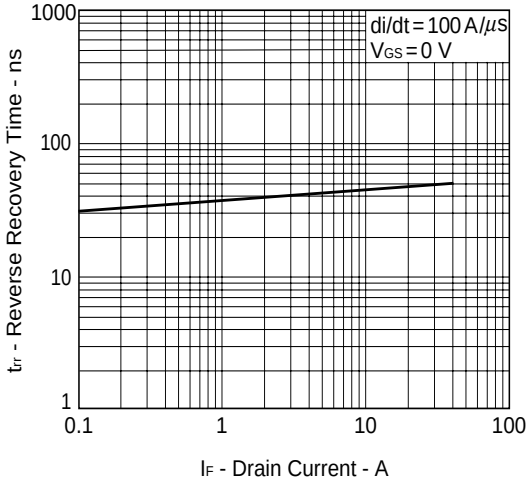

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



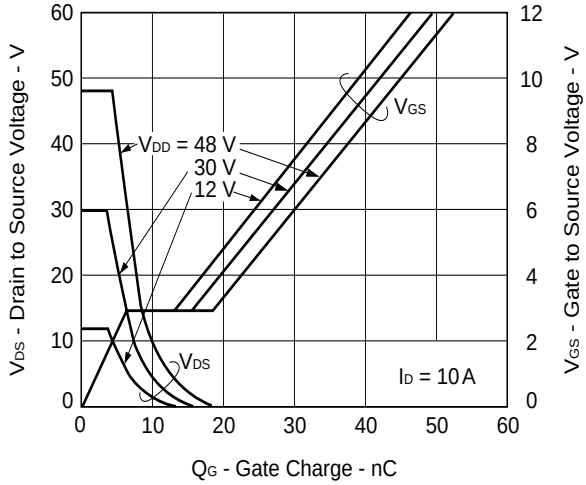

SWITCHING CHARACTERISTICS



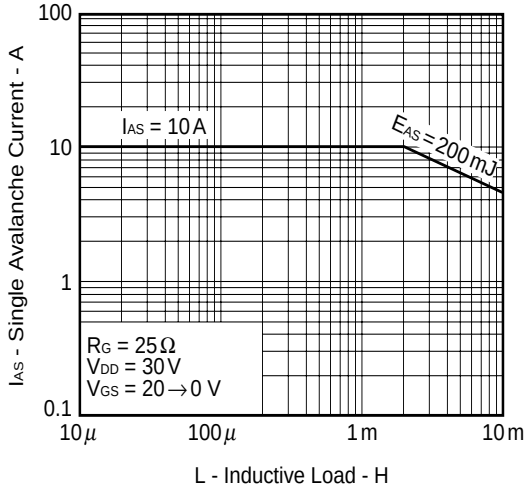

REVERSE RECOVERY TIME vs. DRAIN CURRENT



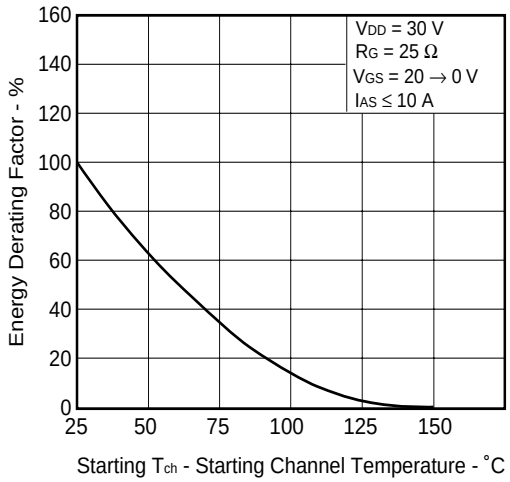

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD




SINGLE AVALANCHE ENERGY
DERATING FACTOR



**[MEMO]**

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