DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2781GR

DESCRIPTION

The μPC2781GR is Silicon monolithic IC designed for use as IQ demodulator in digital communication systems. This IC consists of AGC amplifier, dual balanced mixers (DBM), oscillator, quadrature phase shifter and I & Q output buffer amplifiers.

The package is 20-pin SSOP (shrink small outline package) suitable for high-density surface mount.

FEATURES

- On chip quadrature (90°) phase shifter
- IQ phase and amplitude balance Amplitude Balance ± 0.5 dB
  Phase Balance ± 2.0 degree
- Low distortion IM_3 40 dBc
- Supply Voltage 5 V
- Packaged in 20-pin SSOP suitable for high-density surface mount

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKAGE STYLE
μPC2781GR-E1	20-pin plastic SSOP (225 mil)	Embossed tape 12 mm wide. 2.5 k/REEL Pin 1 indicates pull-out direction of tape

For evaluation sample order, please contact your local NEC office. (Part number for sample order: μPC2781GR)

Caution: electro-static sensitive device

The information in this document is subject to change without notice.

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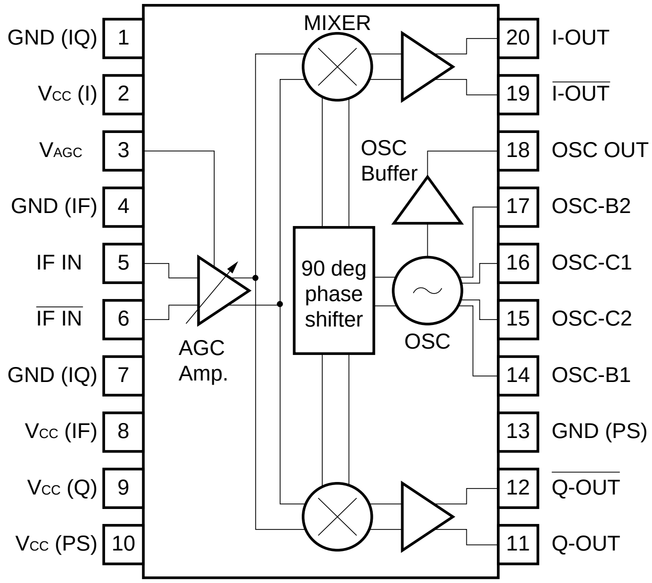
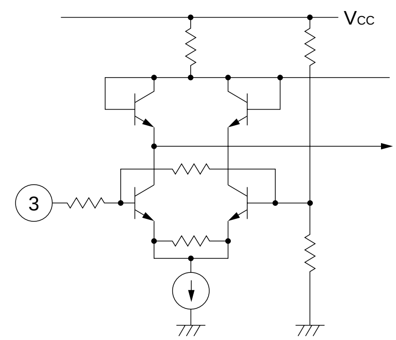
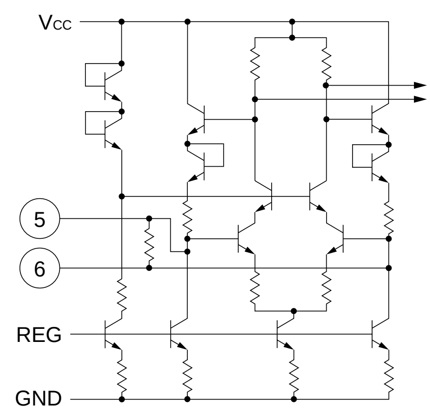
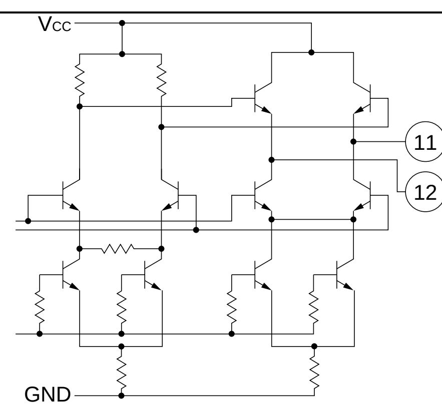
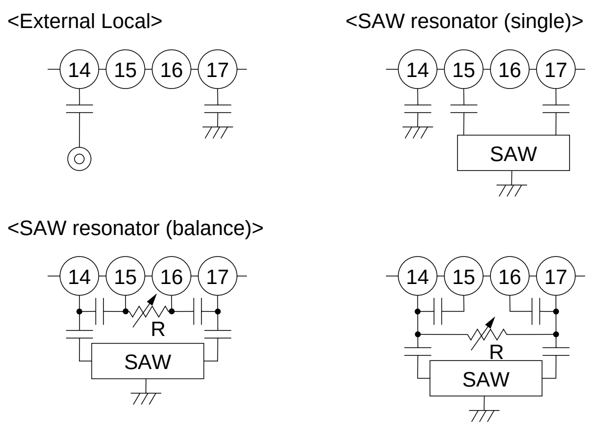
Date Published June 1998 N CP(K)
Printed in Japan

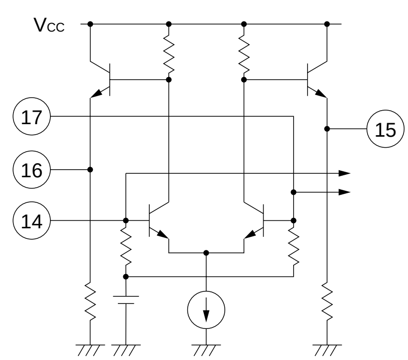
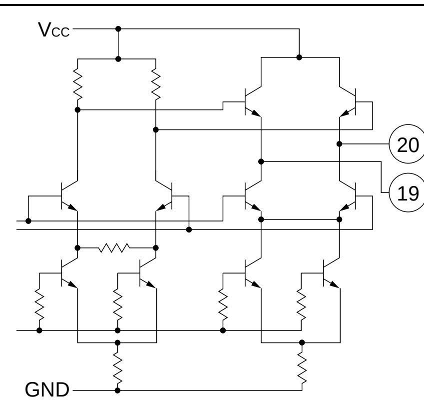
INTERNAL BLOCK DIAGRAM AND PIN CONFIGURATION (Top View)



PIN FUNCTIONS

PIN No.	PIN NAME	PIN VOLTAGE TYP. (V)	FUNCTION AND EXPLANATION	EQUIVALENT CIRCUIT
1	GND (IQ)	0.0	Ground pin of IQ outputs block.	
2	V_{CC} (I)	5.0	Power supply pin of I-output.	
3	V_{AGC}	0 to 4	Gain control pin. • @ measurement circuit 1 V_{AGC} = 0 V: Full gain V_{AGC} = 4 V: Full reduction • @ measurement circuit 2 V_{AGC} = 0 V: Full gain V_{AGC} = 5 V: Full reduction	
4	GND (IF)	0.0	Ground pin of IF, MIX, REG block.	
5	IFin	2.2	IF input pins. In case of single input, 5 pin or 6 pin should be grounded through capacitor.	
6	$\overline{\text{IFin}}$	2.2		
7	GND (IQ)	0.0	Ground pin of IQ outputs block.	
8	V_{CC} (IF)	5.0	Power supply pin of IF, MIX, REG block.	
9	V_{CC} (Q)	5.0	Power supply pin of Q-output.	
10	V_{CC} (PS)	5.0	Power supply pin of Phase Shifter block.	
11	Qout	2.7	Q-signal output pin. 11 pin and 12 pin are balance outputs.	
12	$\overline{\text{Qout}}$	2.7		

<table>
<tr><th>PIN No.</th><th>PIN NAME</th><th>PIN VOLTAGE TYP. (V)</th><th colspan="2">FUNCTION AND EXPLANATION</th><th>EQUIVALENT CIRCUIT</th></tr>
<tr><td>13</td><td>GND (PS)</td><td>0.0</td><td colspan="2">Ground pin of Phase Shifter block.</td><td></td></tr>
<tr><td></td><td colspan="2"></td><td>External local</td><td>SAW (single)</td><td>SAW (balance)</td></tr>
<tr><td>14</td><td>OSC-B1</td><td>3.1</td><td>Oscillator signal input pin.
In case of single input, 14 pin or 17 pin should be grounded through capacitor.</td><td>Grounded through 1000 pF capacitor.</td><td>Connected to SAW resonator through capacitor.</td></tr>
<tr><td>15</td><td>OSC-C2</td><td>3.7</td><td>OPEN</td><td>Connected to SAW resonator through capacitor.</td><td>Connected capacitor between 14 pin and 15 pin to oscillate with active feedback loop.</td></tr>
<tr><td>16</td><td>OSC-C1</td><td>3.7</td><td>OPEN</td><td>OPEN</td><td>Connected capacitor between 16 pin and 17 pin to oscillate with active feedback loop.</td></tr>
<tr><td>17</td><td>OSC-B2</td><td>3.1</td><td>Oscillator signal input pin.
In case of single input, 14 pin or 17 pin should be grounded through capacitor.</td><td>Connected to SAW resonator through capacitor.</td><td>Connected to SAW resonator through capacitor.</td></tr>
<tr><td></td><td colspan="4">

R: Resistor to adjust oscillator power.</td><td>
</td></tr>
<tr><td>18</td><td>OSC OUT</td><td>3.7</td><td colspan="2">Oscillator signal output pin.</td><td></td></tr>
<tr><td>19</td><td>$\overline{\text{Iout}}$</td><td>2.7</td><td colspan="2" rowspan="2">I-signal output pin. 19 pin and 20 pin are balance outputs.</td><td rowspan="2">
</td></tr>
<tr><td>20</td><td>Iout</td><td>2.7</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Supply Voltage	V_{CC}		6.0	V
Power Dissipation 1	P_D1	T_A = 75 °C, V_{CC} = 5.25 V*1	500	mW
Operating Ambient Temperature 1	T_A1		–40 to +75	°C
Storage Temperature Range	T_{stg}		–55 to +150	°C

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Supply Voltage	V_{CC}		6.0	V
Power Dissipation 2	P_D2	T_A = 80 °C, V_{CC} = 5.15 V*1	467	mW
Operating Ambient Temperature 2	T_A2		–40 to +80	°C
Storage Temperature Range	T_{stg}		–55 to +150	°C

***1** Mounted on 50 × 50 × 1.6 mm double epoxy glass board.

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage 1	$V_{CC}1$		4.75	5.0	5.25	V
Operating Ambient Temperature 1	T_A1		–40	+25	+75	°C
IF Input Level Range	P_{IF}	Vout = 1 V_{P-P}	–45	–	–25	dBm
Gain Control Voltage Range 1	$V_{AGC}1$	***1**	0.0	–	4.0	V
Gain Control Voltage Range 2	$V_{AGC}2$	***2**	0.0	–	5.0	V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage 2	$V_{CC}2$		4.75	5.0	5.15	V
Operating Ambient Temperature 2	T_A2		–40	+25	+80	°C
IF Input Level Range	P_{IF}	Vout = 1 V_{p-p}	–45	–	–25	dBm
Gain Control Voltage Range 1	$V_{AGC}1$	***1**	0.0	–	4.0	V
Gain Control Voltage Range 2	$V_{AGC}2$	***2**	0.0	–	5.0	V

***1** By measurement circuit 1 External Resistance: 100 Ω
***2** By measurement circuit 2 External Resistance: 4.7 kΩ + 22 kΩ

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5 V, Zin = 50 Ω, Zout = 1 kΩ)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Circuit Current	I_{CC}	No input signal	52.0	70.0	88.0	mA
IF Input Frequency	f_{IF}	f_{IQ} = 10 MHz, f_{IF} > f_{OSC} ***1, 2**	440	480	520	MHz
IQ Output Frequency	f_{IQ}	f_{IF} > f_{OSC}, Vout = 1 V_{P-P}, P_{OSC} = –8 dBm, CG (@f_{IQ} = 10 MHz) ±1 dB ***1, 2**	0.3	–	20	MHz
AGC Gain Control Range 1	GCR1	f_{IF} = 480 MHz, P_{IF} = –40 dBm, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, f_{IQ} = 10 MHz, V_{AGC} = 0 to 4 V ***1**	15	20	–	dB
AGC Gain Control Range 2	GCR2	f_{IF} = 480 MHz, P_{IF} = –40 dBm, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, f_{IQ} = 10 MHz, V_{AGC} = 0 to 5 V ***2**	15	20	–	dB
IQ Phase Balance	ΔΦ	f_{IF} = 480 MHz, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, f_{IQ} = 10 MHz, Vout = 1 V_{P-P} ***1, 2**	–2	0	+2	deg
IQ Amplitude Balance	ΔG	f_{IF} = 480 MHz, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, f_{IQ} = 10 MHz, Vout = 1 V_{P-P} ***1, 2**	–0.5	0	+0.5	dB
Output Voltage	Vout	f_{IQ} = 10 MHz ***1, 2**	–	1.0	–	V_{P-P}

***1** By measurement circuit 1 External Resistance: 100 Ω

***2** By measurement circuit 2 External Resistance: 4.7 kΩ + 22 kΩ

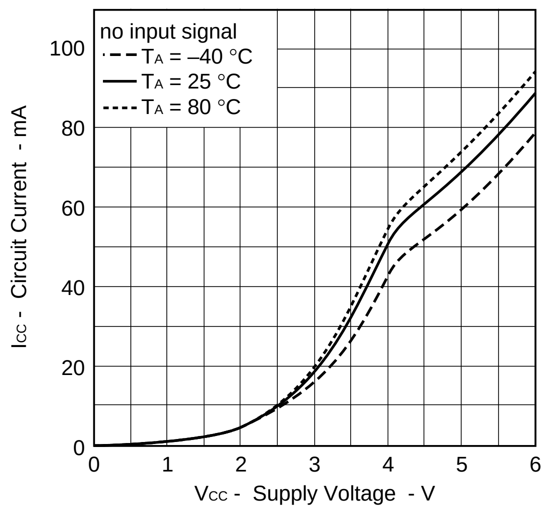
STANDARD CHARACTERISTICS (T_A = 25°C, V_{CC} = 5 V, Zin = 50 Ω, Zout = 1 kΩ)

PARAMETER	SYMBOL	TEST CONDITIONS	REFERENCE VALUE	UNIT
Conversion Gain	G_{CV}	f_{IF} = 480 MHz, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, f_{IQ} = 10 MHz, V_{AGC} = 0 V ***1, 2**	50	dB
Noise Figure (DSB)	NF	f_{IF} = 480 MHz, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, f_{IQ} = 10 MHz, V_{AGC} = 0 V ***3**	13	dB
Third Intermodulation Distortion	IM_3	$f_{IF}1$ = 480 MHz, $f_{IF}2$ = 481 MHz, f_{OSC} = 470 MHz, P_{OSC} = –8 dBm, 0.708 V_{P-P}/tone ***1, 2**	40	dBc
LO to IF Isolation	I_{SO} (LO-IF)	f_{OSC} = 440 to 520 MHz, P_{OSC} = –8 dBm ***1, 2**	50	dB
LO to IQ Isolation	I_{SO} (LO-IQ)	f_{OSC} = 440 to 520 MHz, P_{OSC} = –8 dBm ***1, 2**	20	dB
Maximum Output Power	P_O (sat)	P_{OSC} = –8 dBm, f_{IQ} = 10 MHz ***1, 2**	0	dBm
IQ Output Impedance	Z_o (IQ)	f_{IQ} = 300 kHz to 20 MHz	30	Ω
IF Input Impedance	Zin (IF)	f_{IF} = 480 MHz, no tuning	160 – j30	Ω
IF Input Return Loss	RL (IF)	f_{IF} = 480 MHz, no tuning	5	dB

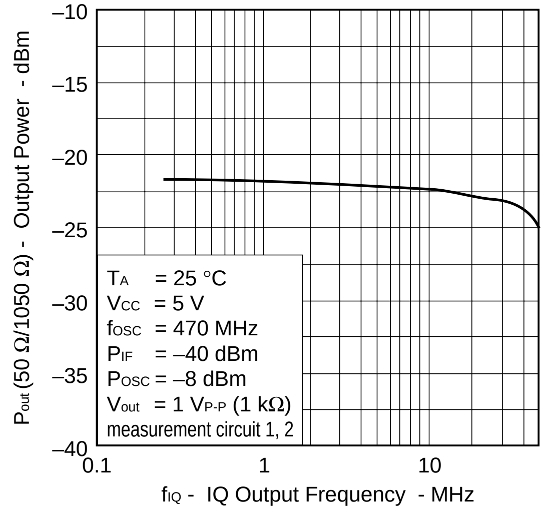
***1** By measurement circuit 1 External Resistance: 100 Ω
***2** By measurement circuit 2 External Resistance: 4.7 kΩ + 22 kΩ
***3** By measurement circuit 3

TYPICAL CHARACTERISTICS

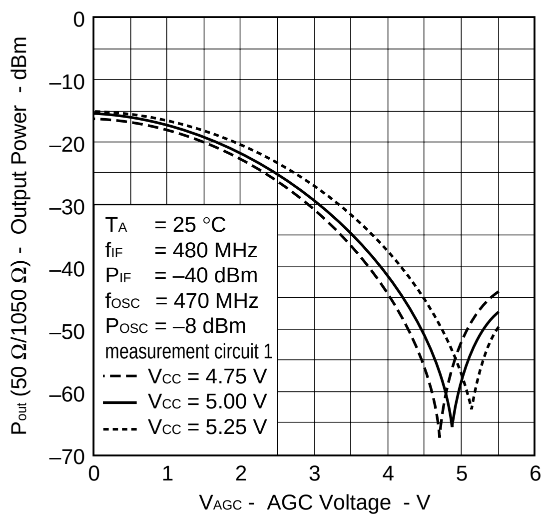
ICC vs. VCC



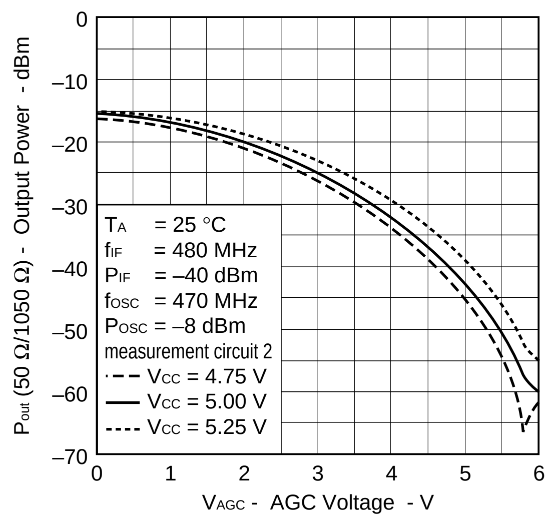
Pout vs. fIQ



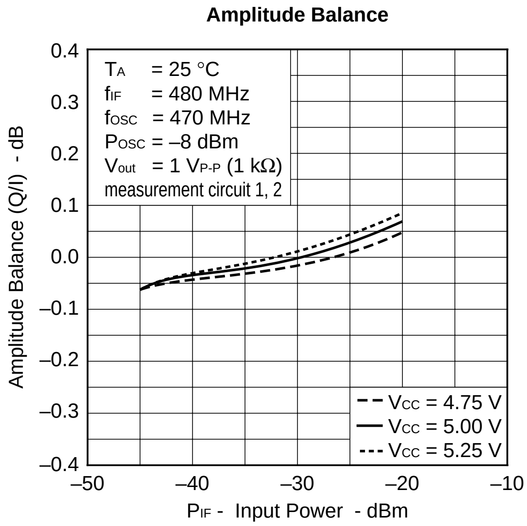
AGC Curve

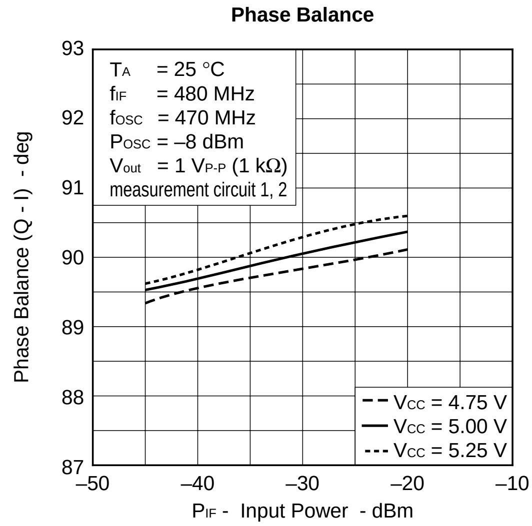


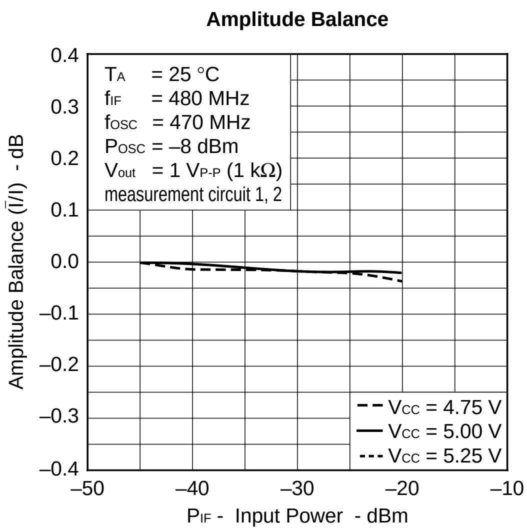
AGC Curve

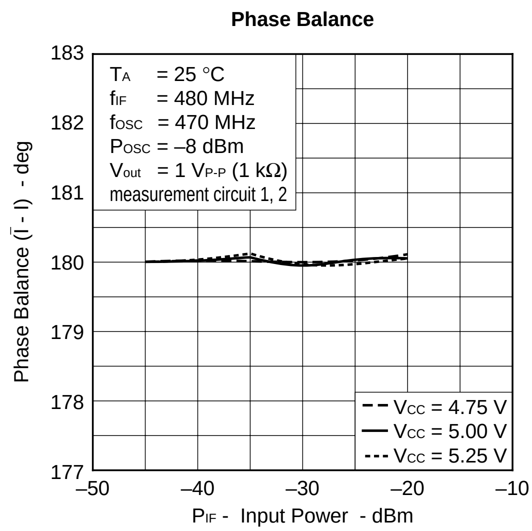


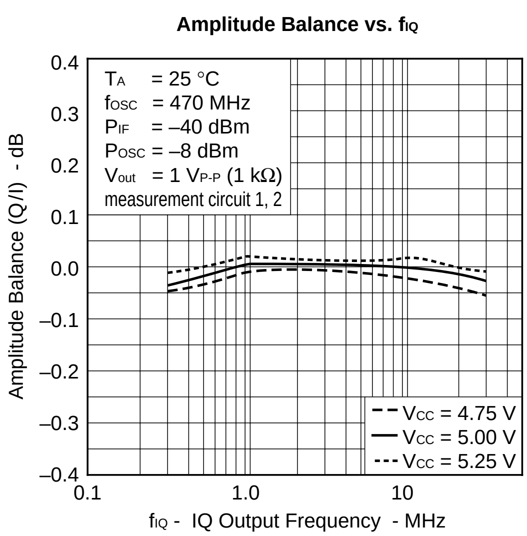
TYPICAL CHARACTERISTICS

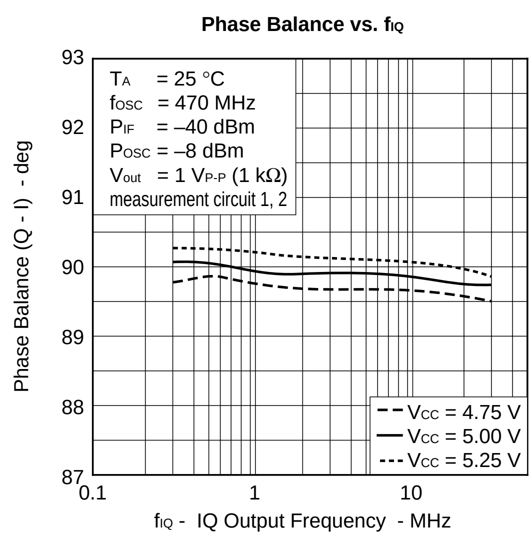






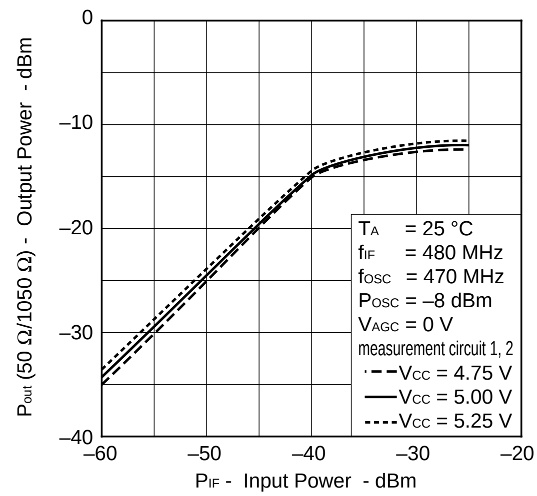




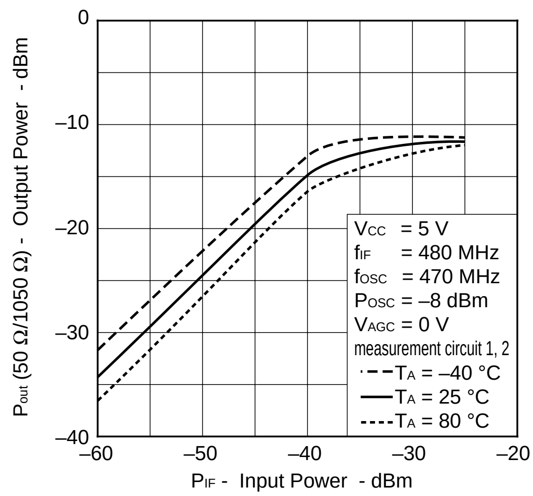


STANDARD CHARACTERISTICS

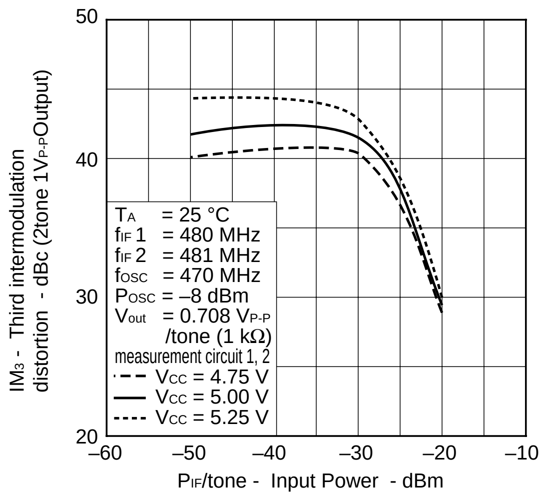
P_{out} vs. P_{in}



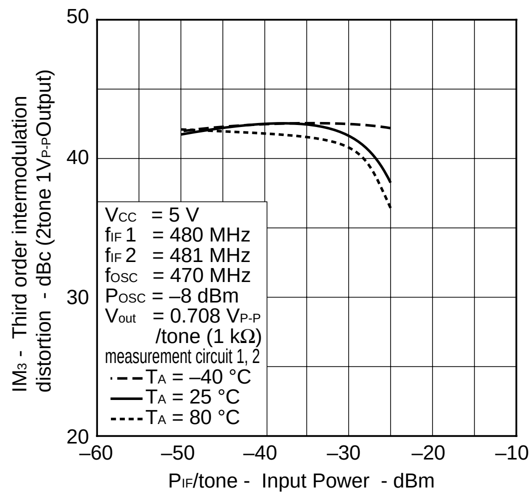
P_{out} vs. P_{in}



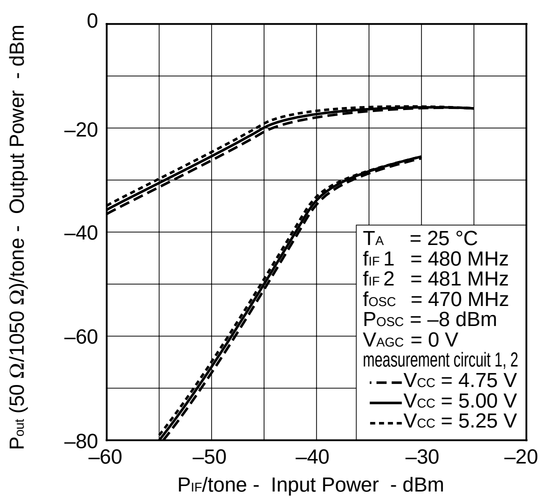
IM_3



IM_3



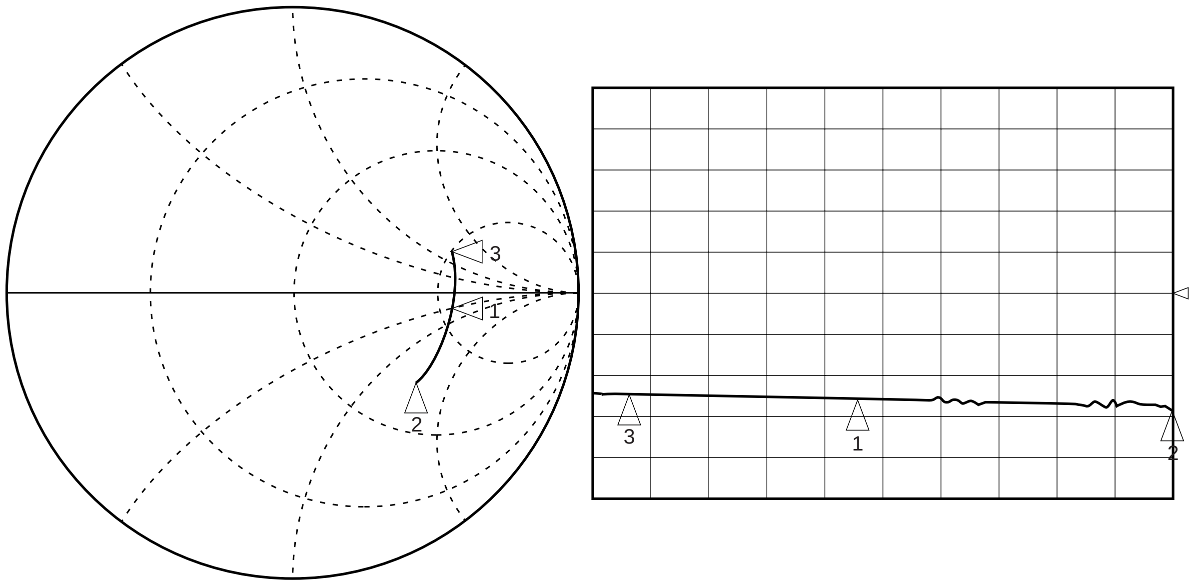
IM_3



IF INPUT IMPEDANCE

S22 Z
REF 1.0 Units
200.0 mUnits/
hp

S22 log MAG
REF 0.0 dB
△ 2.0 dB/
1 –5.1648 dB

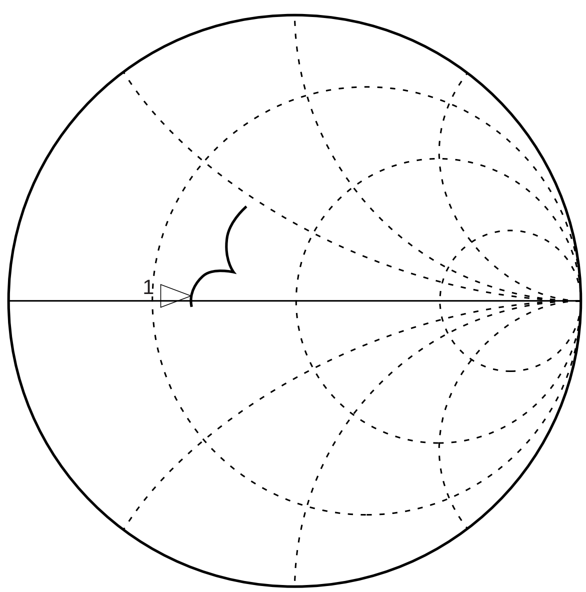


START 0.045000000 GHz
STOP 1.000000000 GHz

MARKER 1	MARKER 2	MARKER 1
479.52 MHz	1.0 GHz	102.3 MHz
166.72 Ω	86.18 Ω	157.49 Ω
–31.203 Ω	–70.629 Ω	58.977 Ω

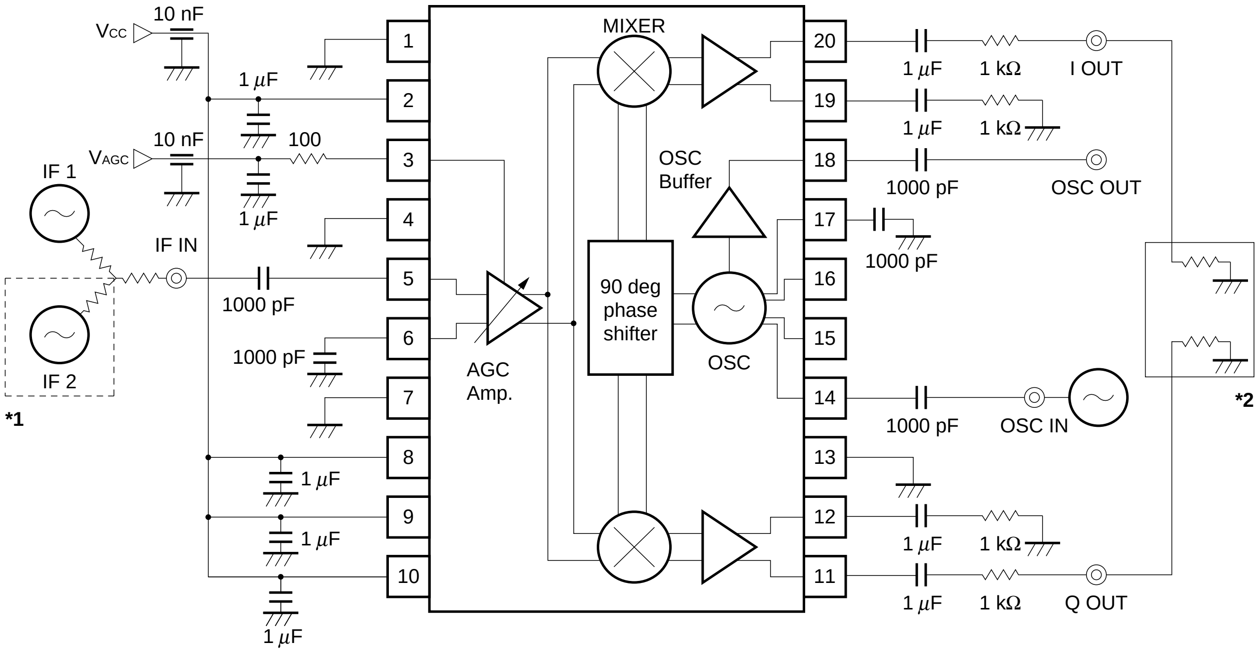
IQ OUTPUT IMPEDANCE (VCC = 5 V)

△ : 24.541 Ω 1.1425 Ω 18.185 nH
1 10.000 000 MHz



START 0.500 000 MHz STOP 1 000.000 000 MHz

MEASUREMENT CIRCUIT 1

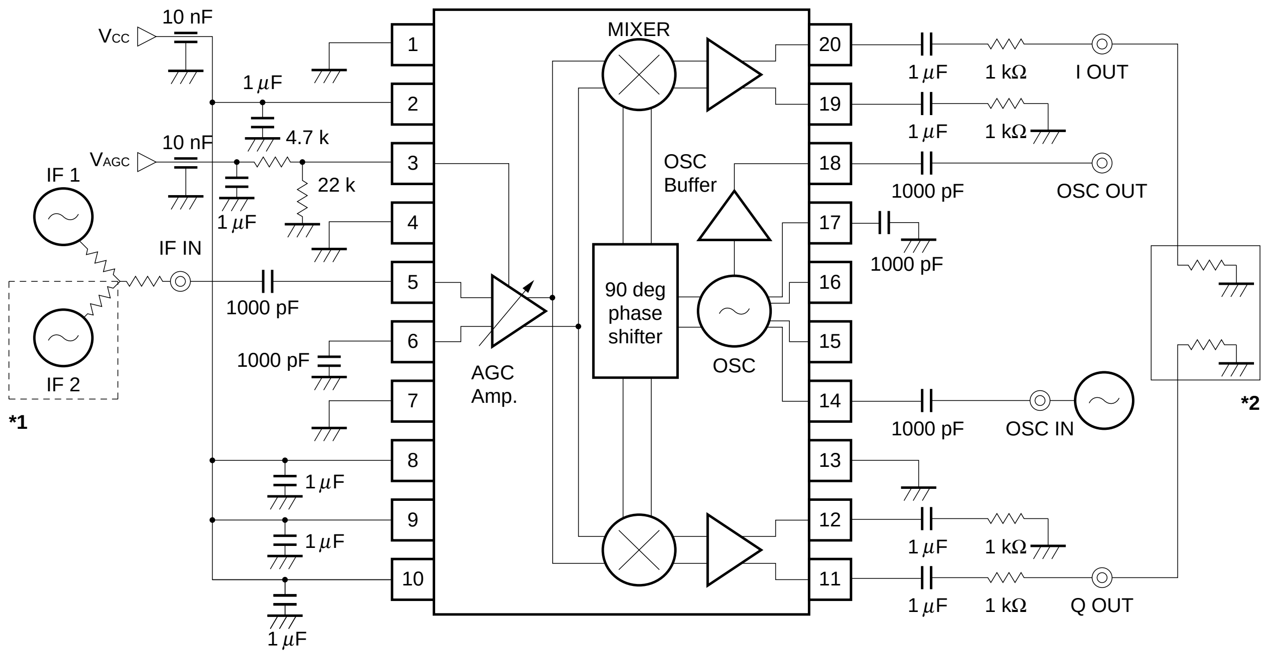


***1** In the case of measurement of IM3.

***2** • Vector Signal Analyzer or Vector Voltage Meter @ measurement of IQ phase balance and IQ amplitude balance.

• Spectrum Analyzer @ measurement of bandwidth and IM3.

MEASUREMENT CIRCUIT 2



***1** In the case of measurement of IM3.

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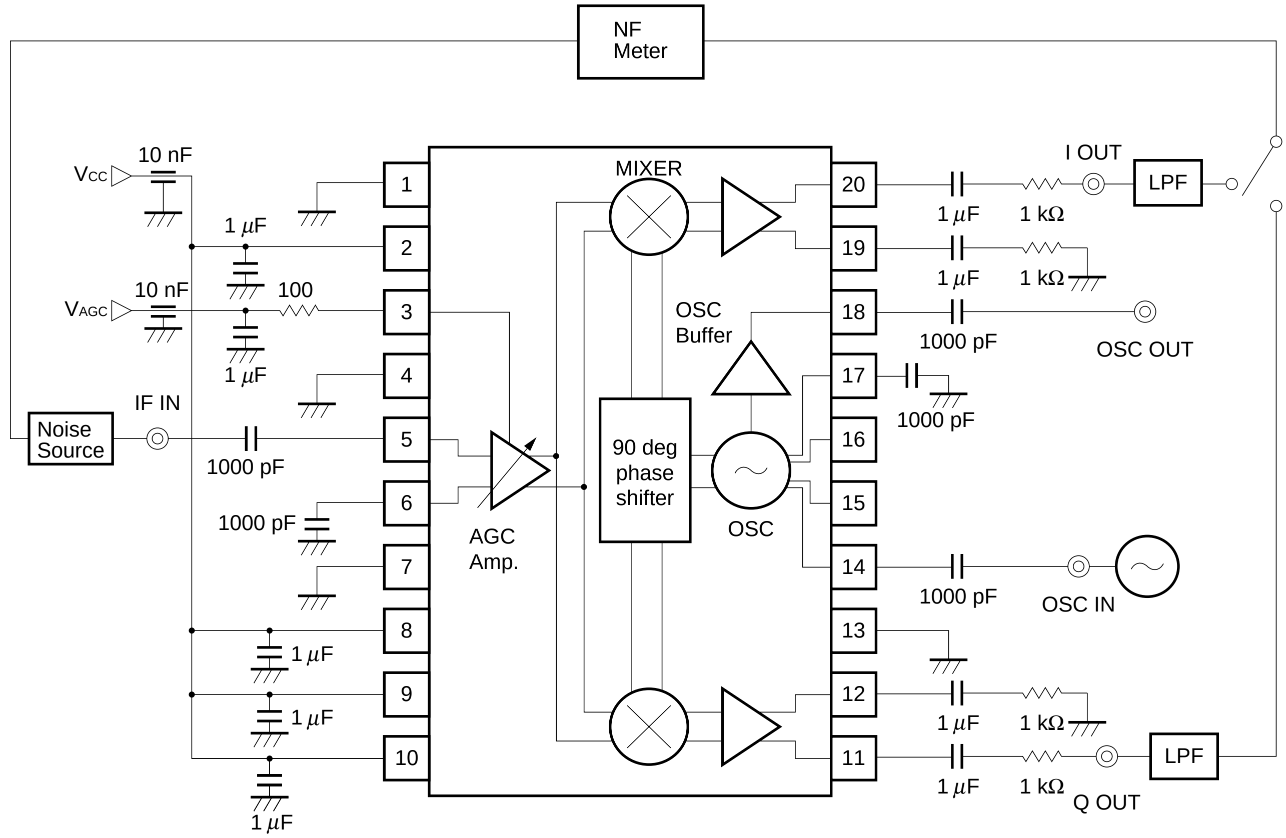
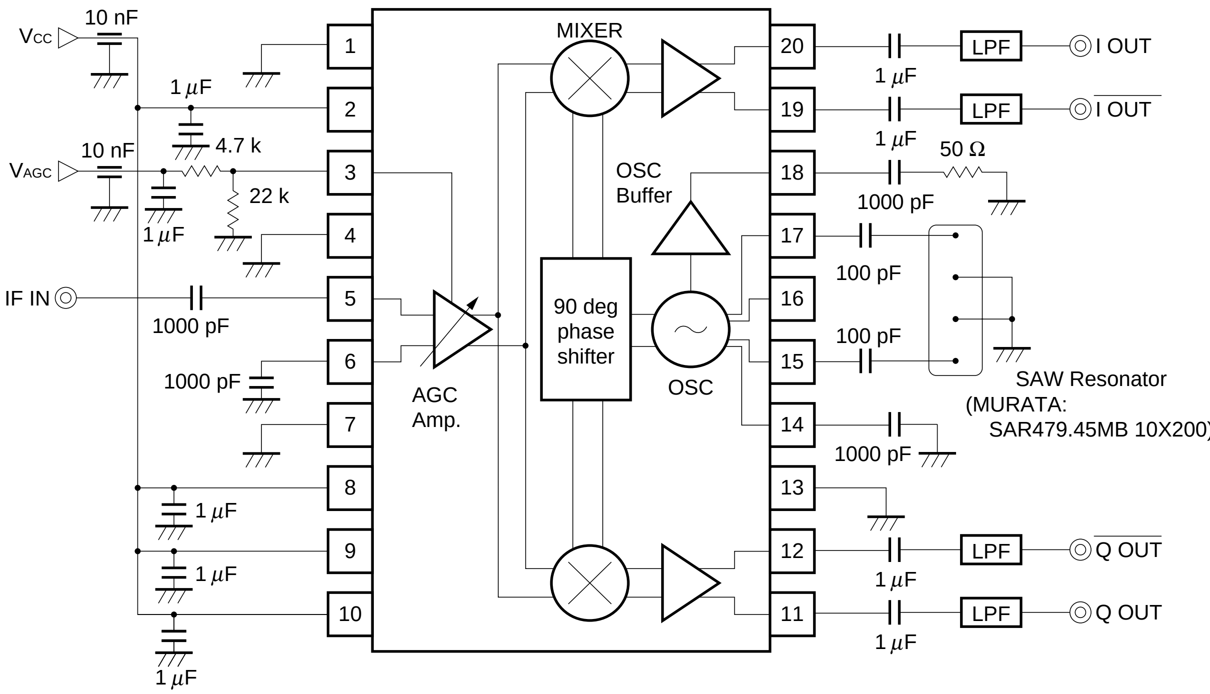
MEASUREMENT CIRCUIT 3

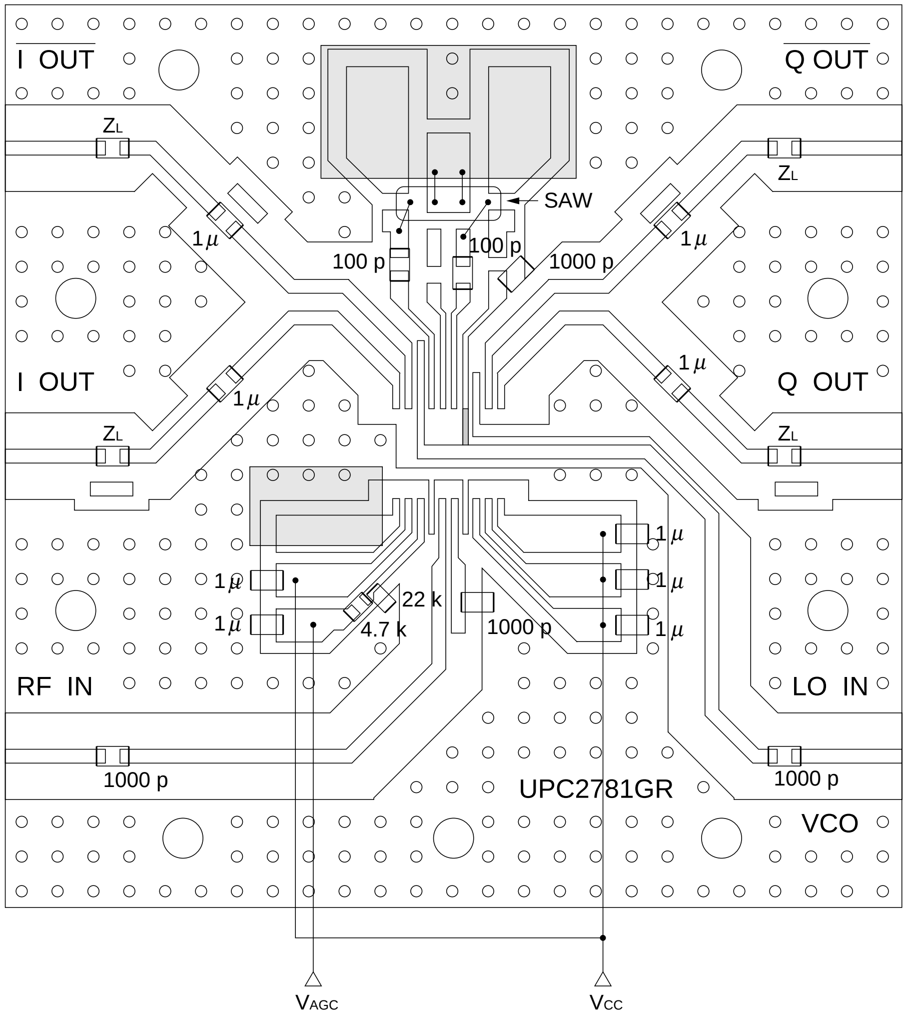


APPLICATION CIRCUIT EXAMPLE



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

ILLUSTRATION OF THE APPLICATION CIRCUIT ASSEMBLED ON EVALUATION BOARD

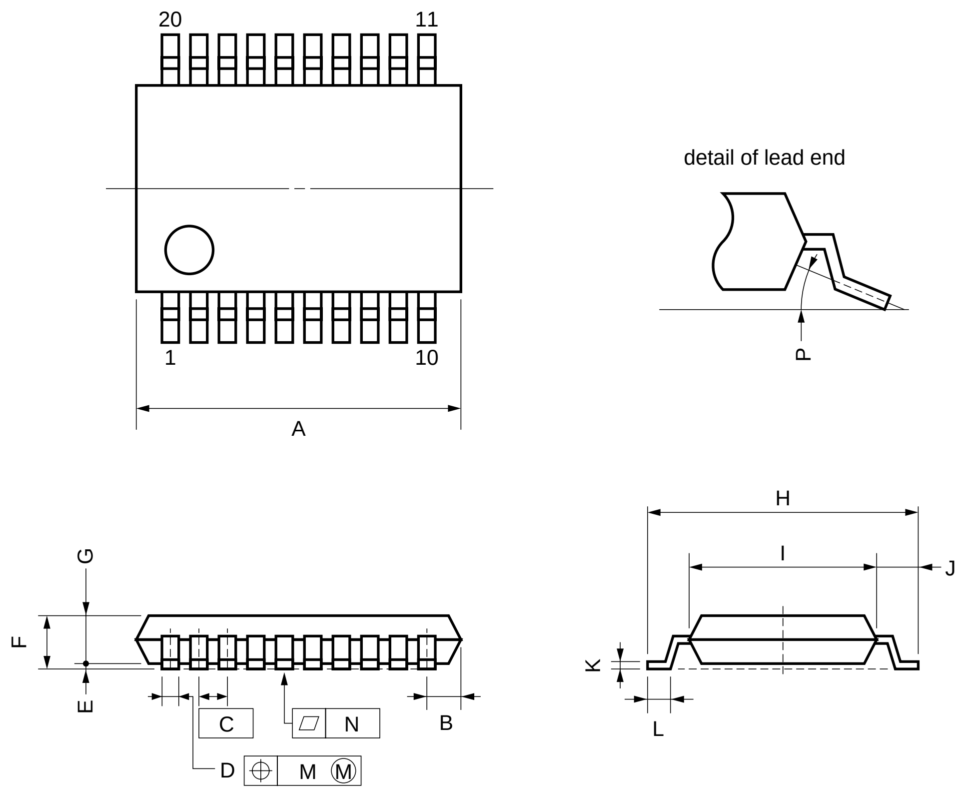


NOTES
- shows short circuited strip for ground
- Pattern should be removed on this application
- ○◯ shows through holes

PACKAGE DIMENSIONS

20 PIN PLASTIC SSOP (225 mil)

(UNIT: mm)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	7.00 MAX.	0.276 MAX.
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P)	0.026 (T.P)
D	$0.22^{+0.10}_{-0.05}$	$0.009^{+0.004}_{-0.002}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.5±0.1	0.058±0.004
H	6.4±0.2	0.253±0.008
I	4.4±0.1	0.174±0.004
J	1.0	0.040
K	$0.15^{+0.10}_{-0.05}$	$0.060^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.004}$
M	0.10	0.004
N	0.15	0.006
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales officers in case other soldering process is used or in case soldering is done under different conditions.

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL** (C10535E).

μPC2781GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Reflow time: 10 seconds or below, Number of reflow process: 1, Exposure limit[Note]: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds or below, Exposure limit[Note]: None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than single process at once, except for "Partial heating method".

[MEMO]

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