### DATA SHEET

# BIPOLAR ANALOG INTEGRATED CIRCUITS $\mu$ PC8106TB, $\mu$ PC8109TB

#### SILICON MMIC 2.0 GHz FREQUENCY UP-CONVERTER FOR CELLULAR/CORDLESS TELEPHONES

#### DESCRIPTION

The  $\mu$ PC8106TB and  $\mu$ PC8109TB are silicon monolithic integrated circuits designed as frequency up-converter for cellular/cordless telephone transmitter stage. The  $\mu$ PC8106TB features improved intermodulation and  $\mu$ PC8109TB features low current consumption. From these two version, you can chose either IC corresponding to your system design. These TB suffix ICs which are smaller package than conventional T suffix ICs contribute to reduce your system size.

The  $\mu$ PC8106TB and  $\mu$ PC8109TB are manufactured using NEC's 20 GHz fr NESAT<sup>TM</sup>III silicon bipolar process. This process uses a silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

#### FEATURES

- Recommended operating frequency : fRFout = 0.4 to 2.0 GHz, fIFin = 100 to 400 MHz
   Supply voltage : Vcc = 2.7 to 5.5 V
- Supply voltage
   High-density surface mounting
   Low current consumption
   Minimized carrier leakage
   Built-in power save function
   Vcc = 2.7 to 5.5 V
   6-pin super minimold package
   6-pin super minimold package
   1cc = 9 mA TYP. @ μPC8106TB
   Icc = 5 mA TYP. @ μPC8109TB
   Due to double balanced mixer

#### APPLICATION

• Cellular/cordless telephone up to 2.0 GHz MAX (example: PHS, PDC, DCS1800 and so on)

#### **ORDERING INFORMATION**

Part Number	Package	Marking	Supplying Form	Product Type
μPC8106TB-E3	6-pin super minimold	C2D	Embossed tape 8 mm wide.	High IP₃
μPC8109TB-E3	minimola	C2G	Pin 1, 2, 3 face the tape perforation side. Qty 3 kpcs/reel.	Low current consumption

**Remark** To order evaluation samples, please contact your local NEC sales office (Part number for sample order:  $\mu$ PC8106TB,  $\mu$ PC8109TB).

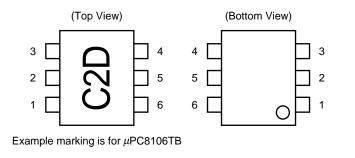
#### Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

#### CONTENTS

1.	PIN CONNECTIONS	3
2.	PRODUCT LINE-UP	3
3.	INTERNAL BLOCK DIAGRAM	3
4.	SYSTEM APPLICATION EXAMPLE	4
5.	PIN EXPLANATION	5
6.	ABSOLUTE MAXIMUM RATINGS	6
7.	RECOMMENDED OPERATING RANGE	6
8.	ELECTRICAL CHARACTERISTICS	6
9.	OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY	7
10.	APPLICATION CIRCUIT EXAMPLE CHARACTERISTICS FOR REFERENCE PURPOSES ONLY	7
11.		
11.	11.1 Test Circuit 1	8
11.	11.1 Test Circuit 1 11.2 Test Circuit 2	8 10
11.	11.1 Test Circuit 1	8 10
	<ul> <li>11.1 Test Circuit 1</li> <li>11.2 Test Circuit 2</li> <li>11.3 Application Circuit Example</li> </ul>	8 10 12
	11.1 Test Circuit 1         11.2 Test Circuit 2         11.3 Application Circuit Example         TYPICAL CHARACTERISTICS	8 10 12 14
	<ul> <li>11.1 Test Circuit 1</li> <li>11.2 Test Circuit 2</li> <li>11.3 Application Circuit Example</li> </ul>	8 10 12 14 14
12.	<ul> <li>11.1 Test Circuit 1</li> <li>11.2 Test Circuit 2</li> <li>11.3 Application Circuit Example</li> <li>TYPICAL CHARACTERISTICS</li> <li>12.1 μPC8106TB</li> </ul>	8 10 12 14 14 16
12.	11.1 Test Circuit 1         11.2 Test Circuit 2         11.3 Application Circuit Example         TYPICAL CHARACTERISTICS         12.1 μPC8106TB         12.2 μPC8109TB         S-PARAMETERS	8 10 12 14 14 16 18
12.	11.1 Test Circuit 1         11.2 Test Circuit 2         11.3 Application Circuit Example         TYPICAL CHARACTERISTICS         12.1 μPC8106TB         12.2 μPC8109TB         S-PARAMETERS         13.1 S-parameters for Each Port – μPC8106TB, μPC8109TB in common –	8 10 12 14 14 16 18 18
12.	11.1 Test Circuit 1         11.2 Test Circuit 2         11.3 Application Circuit Example         TYPICAL CHARACTERISTICS         12.1 μPC8106TB         12.2 μPC8109TB         S-PARAMETERS	8 10 12 14 14 16 18 18 19
12.	11.1 Test Circuit 1         11.2 Test Circuit 2         11.3 Application Circuit Example         TYPICAL CHARACTERISTICS         12.1 $\mu$ PC8106TB         12.2 $\mu$ PC8109TB         S-PARAMETERS         13.1 S-parameters for Each Port – $\mu$ PC8106TB, $\mu$ PC8109TB in common –         13.2 S-parameters for Matched RF Output – with test circuits 1 and 2 –	8 10 12 14 14 14 18 18 19 20
12. 13. 14.	<ul> <li>11.1 Test Circuit 1</li></ul>	8 10 12 14 14 14 16 18 19 20 21

#### **1. PIN CONNECTIONS**



#### $\mu$ PC8106TB, $\mu$ PC8109TB in common

Pin No.	Pin Name		
1	lFinput		
2	GND		
3	LOinput		
4	PS		
5	Vcc		
6	RFoutput		

#### 2. PRODUCT LINE-UP (TA = +25°C, Vcc = VPS = VRFout = 3.0 V, ZS = ZL = 50 $\Omega$ )

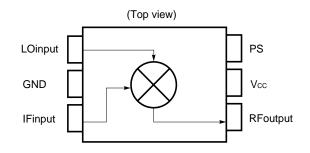
Part Number	lcc	<b>f</b> RFout	CG (dB)				
Part Number	(mA)	(GHz)	@RF 0.9 GHz <sup>Note</sup>	@RF 1.9 GHz	@RF 2.4 GHz		
μPC8106TB	9	0.4 to 2.0	9	7	_		
μPC8109TB	5	0.4 to.2.0	6	4	_		
μPC8163TB	16.5	0.8 to 2.0	9	5.5	_		
μPC8172TB	9	0.8 to 2.5	9.5	8.5	8.0		
μPC8187TB	15	0.8 to 2.5	11	11	10		

Part Number		Po(sat) (dBm)		OIP₃ (dBm)			
Part Number	@RF 0.9 GHz <sup>Note</sup>	@RF 1.9 GHz	@RF 2.4 GHz	@RF 0.9 GHz <sup>Note</sup>	@RF 1.9 GHz	@RF 2.4 GHz	
μPC8106TB	-2	-4	-	+5.5	+2.0	-	
μPC8109TB	-5.5	-7.5	_	+1.5	-1.0	_	
μPC8163TB	+0.5	-2	-	+9.5	+6.0	-	
μPC8172TB	+0.5	0	-0.5	+7.5	+6.0	+4.0	
μPC8187TB	+4	+2.5	+1	+10	+10	+8.5	

**Note**  $f_{RFout} = 0.83 \text{ GHz} @ \mu PC8163TB and \mu PC8187TB$ 

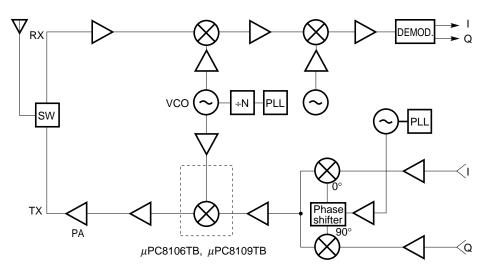
**Remark** Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail. To know the associated product, please refer to each latest data sheet.

#### 3. INTERNAL BLOCK DIAGRAM (for the $\mu$ PC8106TB and $\mu$ PC8109TB)



4. SYSTEM APPLICATION EXAMPLE (schematics of IC location in the system)

#### WIRELESS TRANSCEIVER



#### 5. PIN EXPLANATION (for the $\mu$ PC8106TB and $\mu$ PC8109TB)

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) <sup>Note</sup>	Function and Explanation	Equivalent Circuit
1	IFinput		1.3	This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contri- butes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.	
2	GND	GND	_	GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.	
3	LOinput	_	2.4	Local input pin. Recommendable input level is –10 to 0 dBm.	
5	Vcc	2.7 to 5.5	-	Supply voltage pin.	
6	RFoutput	Same bias as Vcc through external inductor	_	This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.	
4	PS	Vcc or GND	-	Power save control pin. Bias controls operation as follows.	Vcc (5)
				Pin bias Control	k karalan karal
				Vcc Operation	J
				GND Power Save	
					GND → ②

**Note** Each pin voltage is measured at Vcc = VPs = VRFout = 3.0 V.

\*

#### 6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Votage	Vcc	T <sub>A</sub> = +25°C, Pin 5 and 6	6.0	V
PS pin Input Voltage	Vps	$T_A = +25^{\circ}C$	6.0	V
Package Power Dissipation	PD	Mounted on double-sided copper-clad $50 \times 50 \times$ 1.6 mm epoxy glass PWB T <sub>A</sub> = +85°C	270	mW
Operating Ambient Temperature	TA		-40 to +85	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C
Maximum Input Power	Pin		+10	dBm

#### 7. RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	Vcc	2.7	3.0	5.5	V	The same voltage should be supplied to pin 5 and 6
Operating Ambient Temperature	TA	-40	+25	+85	°C	
Local Input Power	PLOin	-10	-5	0	dBm	$Z_s = 50 \Omega$ (without matching)
RF Output Frequency	<b>f</b> RFout	0.4	-	2.0	GHz	With external matching circuit
IF Input Frequency	fıFin	100	-	400	MHz	

#### 8. ELECTRICAL CHARACTERISTICS

(TA = +25°C, Vcc = VRFout = 3.0 V, fIFin = 240 MHz,  $P_{LOin} = -5 \text{ dBm}$ , and  $V_{PS} \ge 2.7 \text{ V}$  unless otherwise specified)

Parameter	Symbol Conditions		μΡC8106TB			μF	Unit		
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Unit
Circuit Current	Icc	No input signal	4.5	9	13.5	2.5	5	8.0	mA
Circuit Current in Power- save Mode	ICC(PS)	V <sub>PS</sub> = 0 V	-	-	10	-	-	10	μA
Conversion Gain 1	CG1	$f_{RFout} = 0.9 \text{ GHz}, P_{IFin} = -30 \text{ dBm}$	6	9	12	3	6	9	dB
Conversion Gain 2	CG2	$f_{RFout} = 1.9 \text{ GHz}, P_{IFin} = -30 \text{ dBm}$	4	7	10	1	4	7	dB
Saturated Output Power 1	Po(sat)1	$f_{RFout} = 0.9 \text{ GHz}, P_{IFin} = 0 \text{ dBm}$	-4	-2	-	-7.5	-5.5	-	dBm
Saturated Output Power 2	Po(sat)2	$f_{RFout} = 1.9 \text{ GHz}, P_{IFin} = 0 \text{ dBm}$	-6.5	-4	-	-10	-7.5	-	dBm

#### 9. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY

(TA = +25°C, Vcc = VRFout = 3.0 V, PLOin = -5 dBm, and VPs  $\ge$  2.7 V unless otherwise mentioned)

Parameter		Symbol	Condit	ions	Referen	Unit	
		0,11201			$\mu$ PC8106TB	$\mu$ PC8109TB	0
3rd Order Distortion	Output	OIP₃1	fıFin1 = 240.0 MHz	frFout = 0.9 GHz	+5.5	+1.5	dBm
Intercept Point		OIP <sub>3</sub> 2	fıFin2 = 240.4 MHz	f <sub>RFout</sub> = 1.9 GHz	+2.0	-1.0	
3rd Order Intermodu Distortion 1	3rd Order Intermodulation Distortion 1		fıFin1 = 240.0 MHz fıFin2 = 240.4 MHz	f <sub>RFout</sub> = 0.9 GHz	-31	-29	dBc
3rd Order Intermodu Distortion 2	3rd Order Intermodulation Distortion 2		Pı⊧in = −20 dBm	freFout = 1.9 GHz	-30	-28	dBc
SSB Noise Figure		SSB • NF	fRFout = 0.9 GHz, fIFin = 240 MHz		8.5	8.5	dB
Power Save	Rise time	TPS(rise)	Vps: $\text{GND} \rightarrow \text{Vcc}$		2.0	2.0	μs
Response Time	Fall time	TPS(fall)	Vps: Vcc $\rightarrow$ GND		2.0	2.0	μs

#### 10. APPLICATION CIRCUIT EXAMPLE CHARACTERSISTICS FOR REFERENCE PURPOSES ONLY (TA = +25°C, Vcc = VPs = VRFout = 3.0 V, fIFin = 130 MHz, fLOin = 1 630 MHz, PLOin = -5 dBm)

Demenden	Deremeter Symbol Conditio		Reference Value	l la it	
Parameter	Symbol	Conditions	μPC8106TB	Unit	
Conversion Gain	CG	f <sub>RFout</sub> = 1.5 GHz, with application circuit example	7	dB	
Saturated Output Power	Po(sat)	f <sub>RFout</sub> = 1.5 GHz, with application circuit example	-3.5	dBm	

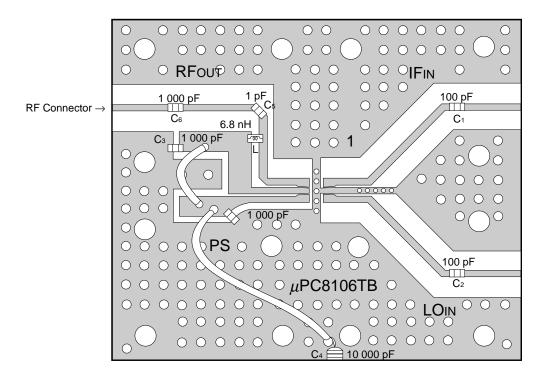
#### 11. TEST CIRCUIT

#### RF = 900 MHz, matched Signal Generator Spectrum Analyzer 100 pF 1000 pF 1 pF 50 Ω 50 Ω 6 Ηŀ RFoutput IFinput ┨┠ -^^/ $\Lambda M$ L. 6.8 nH 5 $C_6$ C5 C1 TT $C_4$ 2 GND Vcc Signal Generator 10 000 777 100 pF pF 50 Ω C<sub>3</sub> 4 3 LOinput łŀ Vcc PS -WW-1 000 pF $C_2$ TT $P_{Loin} = -5 \text{ dBm}$ TT $\Pi$ $\Pi$ TT

11.1 Test Circuit 1 (freeut = 900 MHz, for the  $\mu$ PC8106TB and  $\mu$ PC8109TB)

\* In case of unstable operation, please connect capacitor 100 pF between 4 pin and 5 pin and adjust the matching circuit.

#### EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



#### **COMPONENT LIST**

Form	Symbol	Value	
Chip capacitor	C1, C2	100 pF	
	C3, C6	1 000 pF	
	C₅	1 pF	
Through capacitor	C4	10 000 pF	
Chip inductor	L	6.8 nH <sup>∾œ</sup>	

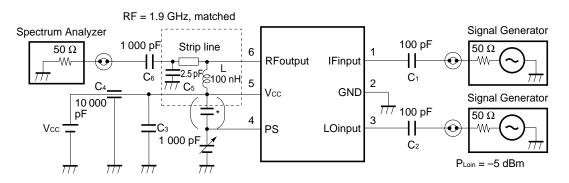
Note 6.8 nH: Murata Mfg. Co., Ltd. LQP31A6N8J04

#### **EVALUATION BOARD CHARACTERS**

- (1) Double-sided copper clad  $35 \times 42 \times 0.4$  mm polyimide board
- (2) Back side: GND pattern
- (3) Solder plated patterns
- (4)  $\bigcirc\bigcirc\bigcirc$ : Through holes
- (5)  $C_6$  is for RF short on the board pattern

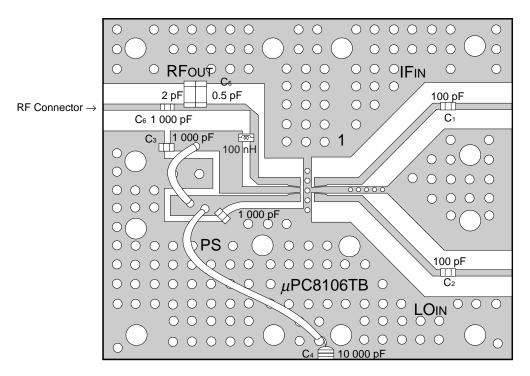
#### 11.2 Test Circuit 2 (freeut = 1.9 GHz, for the $\mu$ PC8106TB and $\mu$ PC8109TB)

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\* In case of unstable operation, please connect capacitor 100 pF between 4 pin and 5 pin and adjust the matching circuit.

#### **\*** EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



#### **COMPONENT LIST**

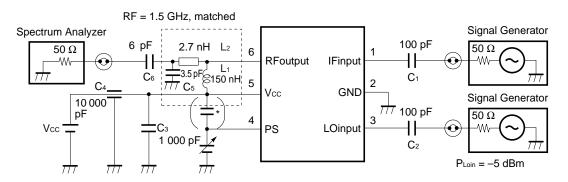
Form	Symbol	Value	
Chip capacitor	C1, C2	100 pF	
	C3, C6	1 000 pF	
	C₅	2.5 pF (2.0 pF, 0.5 pF parallel)	
Through capacitor	C4	10 000 pF	
Chip inductor	L	100 nH <sup>№te</sup>	

Note 100 nH: Murata Mfg. Co., Ltd. LQN1AR10J(K)04

#### **EVALUATION BOAD CHARACTERS**

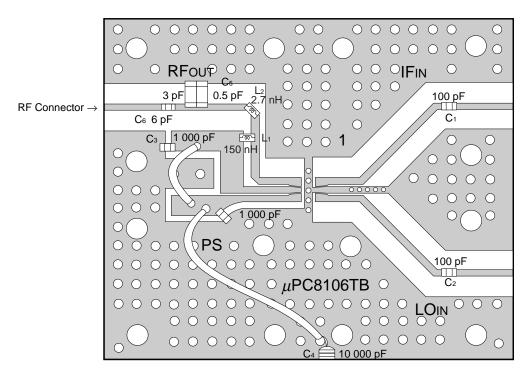
- (1) Double-sided copper clad  $35 \times 42 \times 0.4$  mm polyimide board
- (2) Back side: GND pattern
- (3) Solder plated patterns
- (4)  $\circ \circ \circ \circ$ : Through holes

#### 11.3 Application Circuit Example (free for the $\mu$ PC8106TB and $\mu$ PC8109TB)



\* In case of unstable operation, please connect capacitor 100 pF between 4 pin and 5 pin and adjust the matching circuit.

#### EXAMPLE OF APPLICATION CIRCUIT ASSEMBLED ON EVALUATION BOARD



#### **COMPONENT LIST**

Form	Symbol	Value	
Chip capacitor	C1, C2	100 pF	
	C₃	1 000 pF	
	C₅	3.5 pF (3.0 pF, 0.5 pF parallel)	
	C <sub>6</sub>	6 pF	
Through capacitor	C4	10 000 pF	
Chip inductor	L1	150 nH <sup>Note 1</sup>	
	L2	2.7 nH <sup>№te 2</sup>	

Notes 1. 150 nH: TOKO Co., Ltd. LL2012-FR15

2. 2.7 nH : TOKO Co., Ltd. LL2012-F2N7S

#### **EVALUATION BOARD CHARACTERS**

- (1) Double-sided copper clad  $35 \times 42 \times 0.4$  mm polyimide board
- (2) Back side: GND pattern
- (3) Solder plated patterns
- (4)  $\circ \circ \circ \circ$ : Through holes

#### Caution

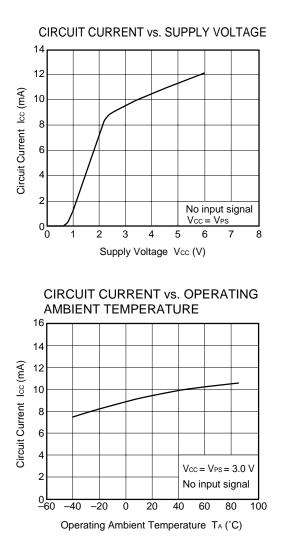
The test circuits and board pattern on data sheet are for performance evaluation use only. (They are not recommended circuits.) In the case of actual design-in, matching circuit should be determined using S parameter of desired frequency in accordance to actual mounting pattern.

For external circuits of the ICs, following Application Note is also available.

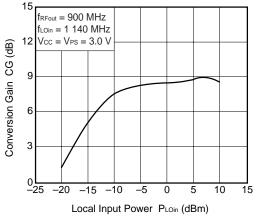
• μPC8106, μPC8109, μPC8163 Application Note (Document No. P13683E)

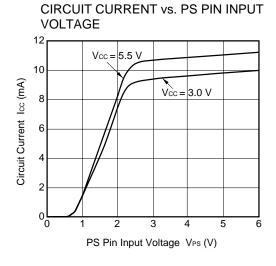
12. TYPICAL CHARACTERISTICS (TA = +25°C, Vcc = VRFout, with test circuit 1 or 2, according to the operating frequency, unless otherwise specified)

#### 12.1 µPC8106TB

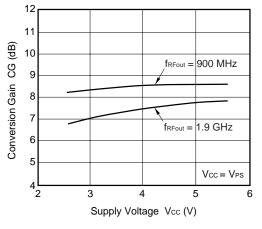


CONVERSION GAIN vs. LOCAL INPUT POWER

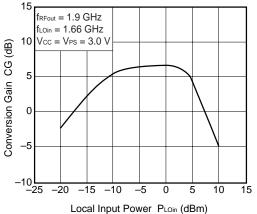


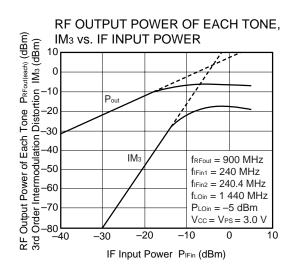


CONVERSION GAIN vs. SUPPLY VOLTAGE



CONVERSION GAIN vs. LOCAL INPUT POWER





RF OUTPUT POWER OF EACH TONE.

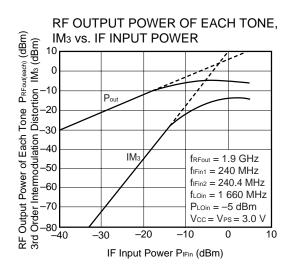
IM<sub>3</sub> vs. IF INPUT POWER

Pout

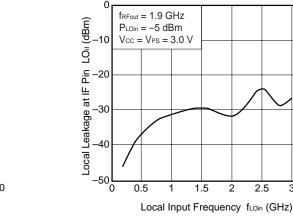
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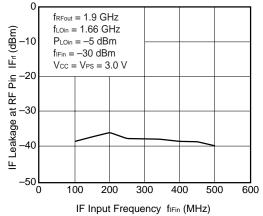
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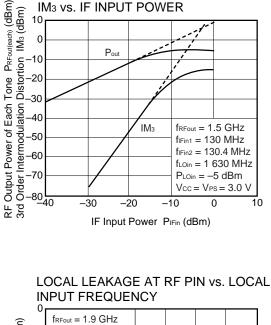


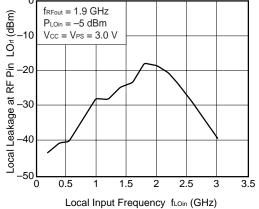
LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT FREQUENCY



IF LEAKAGE AT RF PIN vs. IF INPUT FREQUENCY



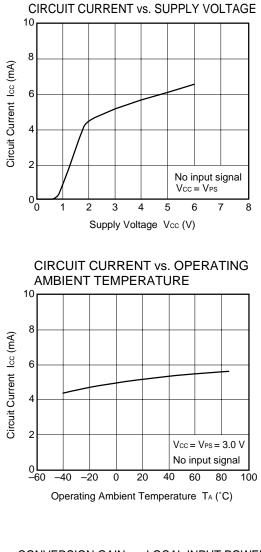


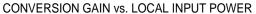


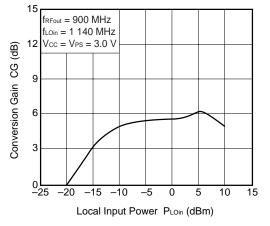
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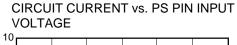
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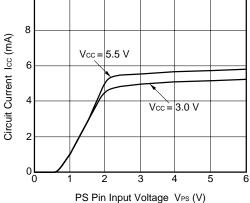
#### 12.2 µPC8109TB



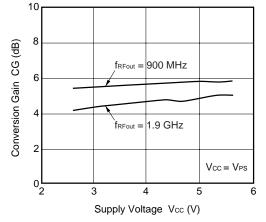


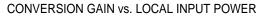


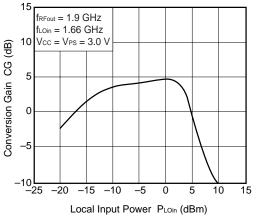


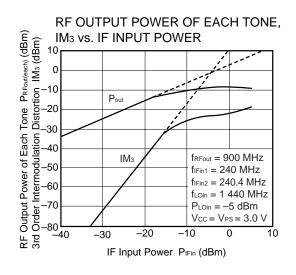


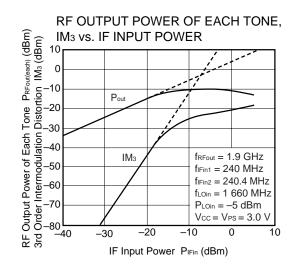
CONVERSION GAIN vs. SUPPLY VOLTAGE

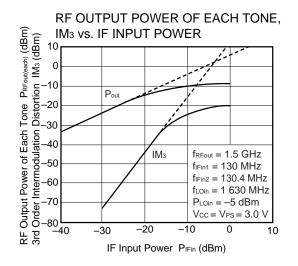






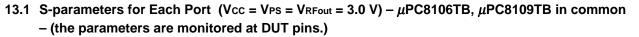


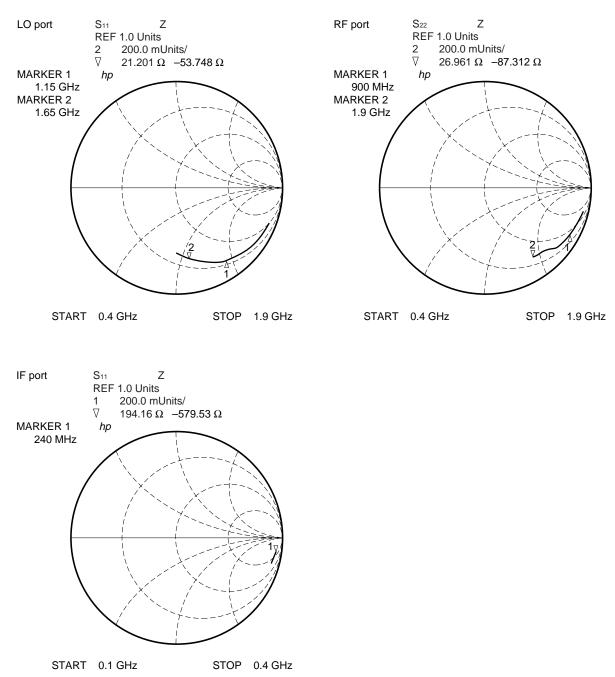




Remark The graphs indicate nominal characteristics.

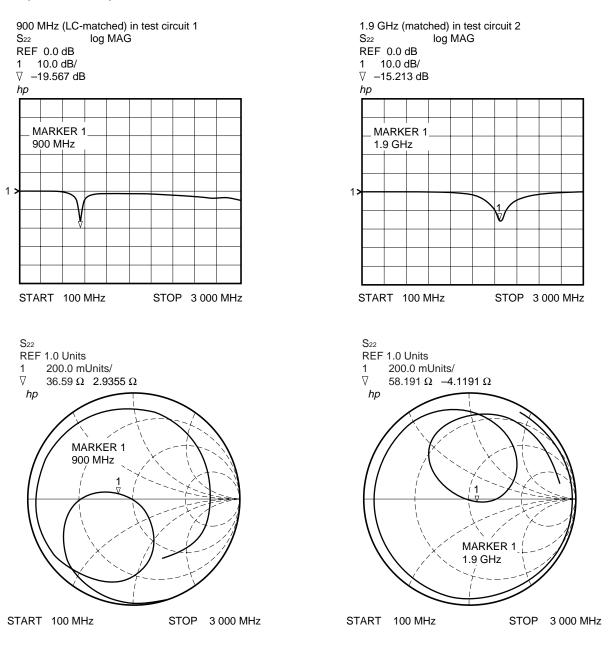
#### 13. S-PARAMETERS





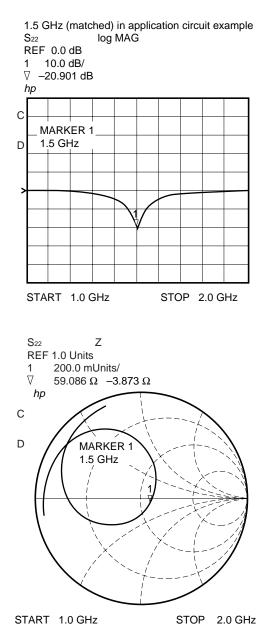
## 13.2 S-parameters for Matched RF Output (Vcc = VPs = V<sub>RFout</sub> = 3.0 V) – with test circuits 1 and 2 ( $\mu$ PC8106TB, $\mu$ PC8109TB in common) – (S<sub>22</sub> data are monitored at RF connector on board.)

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Data Sheet P12770EJ3V0DS00

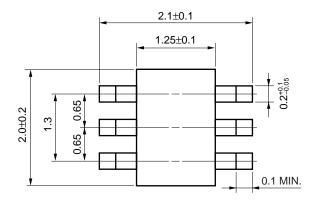
13.3 S-parameters for Matched RF Output (Vcc = VPs = VRFout = 3.0 V) – with application circuit example – (S22 data are monitored at RF connector on board.)

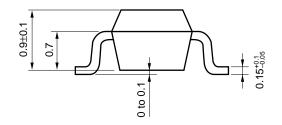


NEC

#### ★ 14. PACKAGE DIMENSIONS

#### 6-PIN SUPER MINIMOLD (UNIT: mm)





#### **15. NOTE ON CORRECT USE**

- (1) Observe precutions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Keep the wiring length of the ground pins as short as possible.
- (4) Connect a bypass capacitor to the Vcc pin.
- (5) Connect a matching circuit to the RF output pin.

#### **16. RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None <sup>Note</sup>	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None <sup>Note</sup>	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None <sup>Note</sup>	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None <sup>Note</sup>	_

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

#### Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]



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