

**POWER SUPPLY FOR TFT-LCD DRIVER**
**DESCRIPTION**

The  $\mu$ PD161660 is a power supply IC for TFT-LCD driver. This ICs can generate the levels which TFT-LCD driver need, from 2.7 V.

**FEATURES**

- To generate 3 levels from single voltage input
- To integrate regulator circuit for source and gate driver

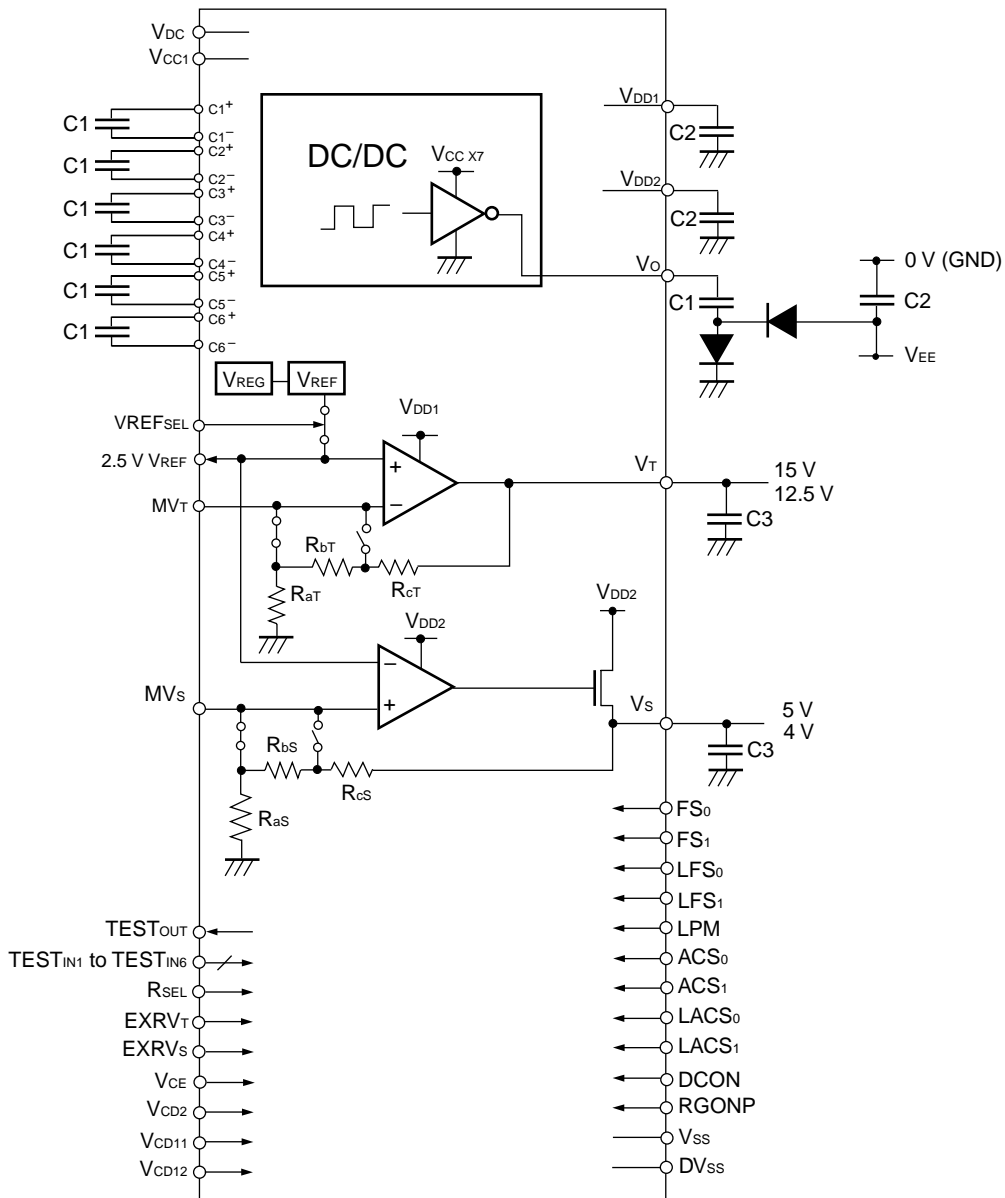
**ORDERING INFORMATION**

	Part number	Package
★	$\mu$ PD161660P	Chip

**Remark** Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM/SYSTEM DIAGRAM

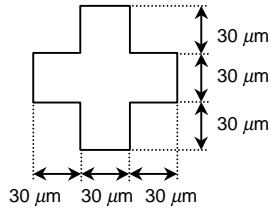


2. PIN CONFIGURATION (Pad Layout)

Chip size: X = 4.20 mm, Y = 4.35 mm

Pad size : 100 x 100 μm<sup>2</sup>

(1) Alignment mark



(2) Arrangement

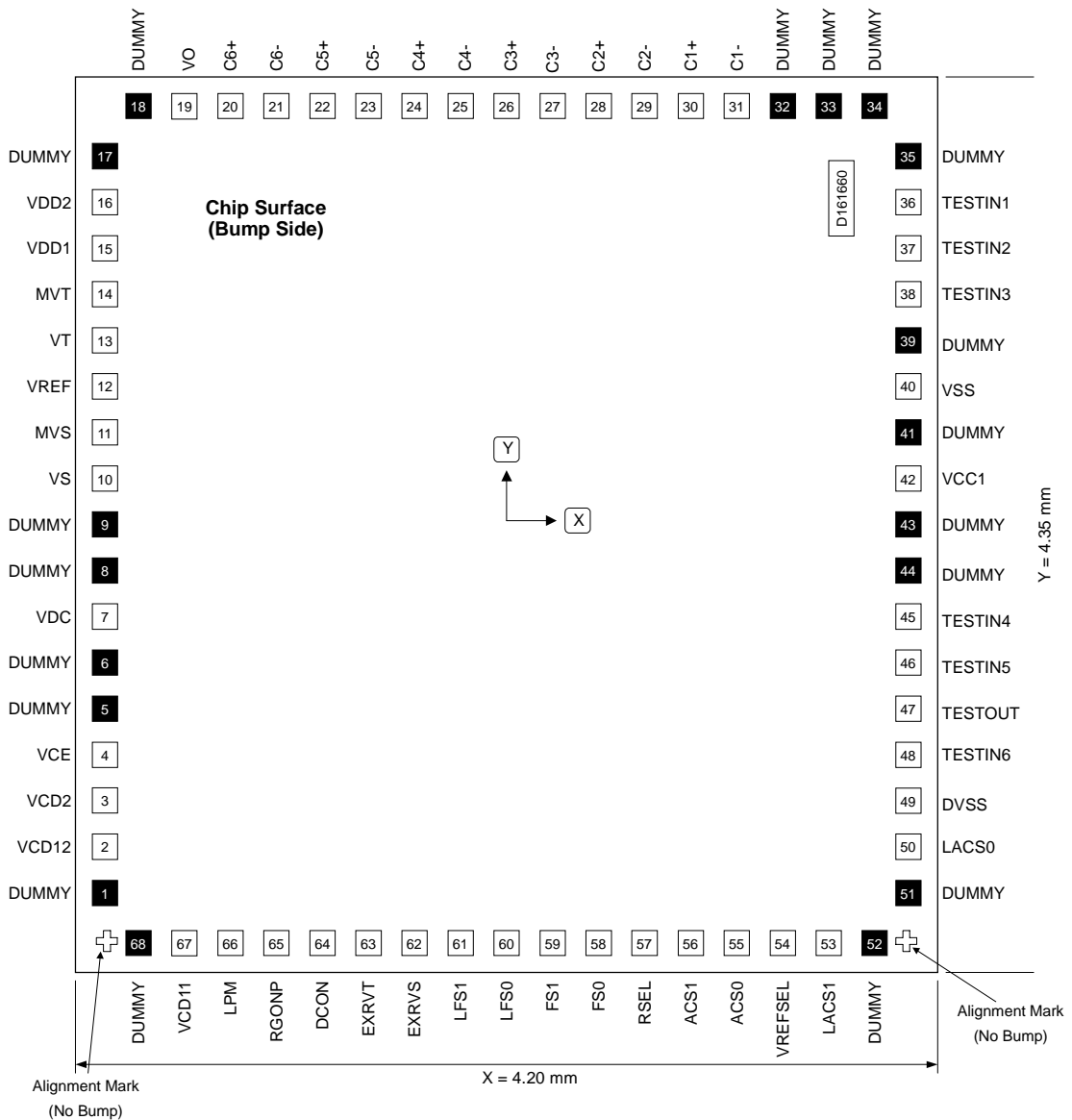


Table 2-1. Pad Layout

Pad No.	Pad name	X[mm]	Y[mm]
1	DUMMY	-1950	-1800
2	VCD12	-1950	-1575
3	VCD2	-1950	-1350
4	VCE	-1950	-1125
5	DUMMY	-1950	-900
6	DUMMY	-1950	-675
7	VDC	-1950	-450
8	DUMMY	-1950	-225
9	DUMMY	-1950	0
10	Vs	-1950	225
11	MVs	-1950	450
12	VREF	-1950	675
13	Vt	-1950	900
14	MVt	-1950	1125
15	VDD1	-1950	1350
16	VDD2	-1950	1575
17	DUMMY	-1950	1800
18	DUMMY	-1800	2025
19	Vo	-1575	2025
20	C6 <sup>+</sup>	-1350	2025
21	C6 <sup>-</sup>	-1125	2025
22	C5 <sup>+</sup>	-900	2025
23	C5 <sup>-</sup>	-675	2025
24	C4 <sup>+</sup>	-450	2025
25	C4 <sup>-</sup>	-225	2025
26	C3 <sup>+</sup>	0	2025
27	C3 <sup>-</sup>	225	2025
28	C2 <sup>+</sup>	450	2025
29	C2 <sup>-</sup>	675	2025
30	C1 <sup>+</sup>	900	2025
31	C1 <sup>-</sup>	1125	2025
32	DUMMY	1350	2025
33	DUMMY	1575	2025
34	DUMMY	1800	2025
35	DUMMY	1950	1800
36	TESTIN1	1950	1575
37	TESTIN2	1950	1350
38	TESTIN3	1950	1125
39	DUMMY	1950	900
40	VSS	1950	675

Pad No.	Pad name	X[mm]	Y[mm]
41	DUMMY	1950	450
42	VCC1	1950	225
43	DUMMY	1950	0
44	DUMMY	1950	-225
45	TESTIN4	1950	-450
46	TESTIN5	1950	-675
47	TESTOUT	1950	-900
48	TESTIN6	1950	-1125
49	DVSS	1950	-1350
50	LACS0	1950	-1575
51	DUMMY	1950	-1800
52	DUMMY	1800	-2025
53	LACS1	1575	-2025
54	VREFSEL	1350	-2025
55	ACS0	1125	-2025
56	ACS1	900	-2025
57	RSEL	675	-2025
58	FS0	450	-2025
59	FS1	225	-2025
60	LFS0	0	-2025
61	LFS1	-225	-2025
62	EXRVS	-450	-2025
63	EXRVT	-675	-2025
64	DCON	-900	-2025
65	RGONP	-1125	-2025
66	LPM	-1350	-2025
67	VCD11	-1575	-2025
68	DUMMY	-1800	-2025
	Alignment mark	-1950	-2025
	Alignment mark	1950	-2025

3. PIN FUNCTIONS

(1/2)

Symbol	Pin Name	Pad No.	I/O	Description
V <sub>DC</sub>	Power supply	7	–	Power supply for DC/DC converter.
V <sub>CC1</sub>	Power supply	42	–	Power supply for logic circuit.
V <sub>SS</sub>	Ground	40	–	Ground.
DV <sub>SS</sub>	Ground	49	–	Ground (for control pin pull-down)
V <sub>DD1</sub>	DC/DC converter output	15	–	Boost voltage of DC/DC converter (x4, x5, x6 or x7). The capacitors required for each boost level are shown below. <ul style="list-style-type: none"> <li>• x4 boost: C1, C2, C6 (C3, C4, and C5 are not required)</li> <li>• x5 boost: C1, C2, C3, C6 (C4, and C5 are not required)</li> <li>• x6 boost: C1, C2, C3, C4, C6 (C5 is not required)</li> <li>• x7 boost: C1, C2, C3, C4, C5, C6</li> </ul>
V <sub>DD2</sub>	DC/DC converter output	16	–	Boost voltage of DC/DC converter (x2 or x3). The boost steps for V <sub>DD2</sub> is selected by V <sub>CD2</sub> pin. The capacitors required for each boost level are shown below. <ul style="list-style-type: none"> <li>• x2 boost: C1</li> <li>• x3 boost: C1, C2,</li> </ul>
V <sub>O</sub>	Rectangle signal output for negative boost	19	–	Rectangle signal output for negative boost. The V <sub>O</sub> voltage range is selected by V <sub>CE</sub> pin. The capacitors required for each boost level are shown below. <V <sub>CE</sub> = L> <ul style="list-style-type: none"> <li>• x3 boost: C1, C2</li> <li>• x4 boost: C1, C2, C3</li> <li>• x5 boost: C1, C2, C3, C4</li> <li>• x6 boost: C1, C2, C3, C4, C5</li> </ul> <V <sub>CE</sub> = H> <ul style="list-style-type: none"> <li>• x4 boost: C1, C2, C6</li> <li>• x5 boost: C1, C2, C3, C6</li> <li>• x6 boost: C1, C2, C3, C4, C6</li> <li>• x7 boost: C1, C2, C3, C4, C5, C6</li> </ul>
V <sub>T</sub>	Regulator output	13	–	15 V/12.5 V regulator output for gate driver.
V <sub>S</sub>	Regulator output	10	–	5 V/4 V regulator output for source driver.
V <sub>REF</sub>	Reference voltage input/output	12	I/O	The gate driver includes reference voltage for V <sub>B</sub> regulator. When V <sub>REFSEL</sub> = H, external reference voltage can be input. Reference voltage input/output pin of V <sub>T</sub> , V <sub>S</sub> regulator.
DCON	DC/DC converter control	64	I	DC/DC converter ON/OFF control. Connect to DCON pin of source driver.
RGONP	Regulator control	65	I	Regulator ON/OFF control. Connect to RGONP pin of source driver.
EXRV <sub>T</sub>	V <sub>T</sub> regulating resistor selection	63	I	To select internal/external resistor for V <sub>T</sub> regulator.
EXRV <sub>S</sub>	V <sub>S</sub> regulating resistor selection	62	I	To select internal/external resistor for V <sub>S</sub> regulator.

(2/2)

Symbol	Pin Name	Pad No.	I/O	Description
V <sub>CD11</sub>	V <sub>DD1</sub> booster selection	67	I	To select x4/x5/x6/x7 boost for V <sub>DD1</sub> . Connect to V <sub>CD11</sub> pin of source driver.
V <sub>CD12</sub>	V <sub>DD1</sub> booster selection	2	I	To select x4/x5/x6/x7 boost for V <sub>DD1</sub> . Connect to V <sub>CD12</sub> pin of source driver.
V <sub>CD2</sub>	V <sub>DD2</sub> booster selection	3	I	To select x2/x3 boost for V <sub>DD2</sub> . Connect to V <sub>CD2</sub> pin of source driver.
V <sub>CE</sub>	V <sub>O</sub> level selection	4	I	To select x3/x4/x5/x6/x7 boost for V <sub>O</sub> top voltage level. Connect to V <sub>CE</sub> pin of source driver.
LPM	Low power mode signal	66	I	Control signal for low power mode. When this pin is high level, it comes to be low power mode. LPM = H: LACS <sub>0</sub> , LACS <sub>1</sub> , LFS <sub>0</sub> , LFS <sub>1</sub> are enabled. LPM = L: ACS <sub>0</sub> , ACS <sub>1</sub> , FS <sub>0</sub> , FS <sub>1</sub> are enabled. Connect to LPMP pin of source driver.
ACS <sub>0</sub> , ACS <sub>1</sub>	Amp. current selection	55, 56	I	To select Amp. current when in scanning.
LACS <sub>0</sub> , LACS <sub>1</sub>	Amp. current selection	50, 53	I	To select Amp. current in low power mode.
MV <sub>T</sub>	V <sub>T</sub> regulator input	14	–	EXRV <sub>T</sub> = H: Connect to external resistor. EXRV <sub>T</sub> = L: Leave it open.
MV <sub>S</sub>	V <sub>S</sub> regulator input	11	–	EXRV <sub>S</sub> = H: Connect to external resistor. EXRV <sub>S</sub> = L: Leave it open.
TEST <sub>IN1</sub> - TEST <sub>IN6</sub>	Test	36-38, 45, 46, 48	I	Test pins. Normally leave it open.
TEST <sub>OUT</sub>	Test output	47	O	Test pin. Normally leave them open.
FS <sub>0</sub> , FS <sub>1</sub>	OSC frequency selection	58, 59	I	To select OSC frequency for DC/DC converter when in scanning.
LFS <sub>0</sub> , LFS <sub>1</sub>	OSC frequency selection	60, 61	I	To select OSC frequency for DC/DC capacitor when in scanning.
R <sub>SEL</sub>	Internal resistor selection for regulator	57	I	To select internal resistor for regulator.
VREF <sub>SEL</sub>	Regulator reference voltage input selection	54	I	To select external or internal reference voltage of V <sub>T</sub> , V <sub>S</sub> regulator.
C <sub>1</sub> <sup>+</sup> , C <sub>1</sub> <sup>-</sup> C <sub>2</sub> <sup>+</sup> , C <sub>2</sub> <sup>-</sup> C <sub>3</sub> <sup>+</sup> , C <sub>3</sub> <sup>-</sup> C <sub>4</sub> <sup>+</sup> , C <sub>4</sub> <sup>-</sup> C <sub>5</sub> <sup>+</sup> , C <sub>5</sub> <sup>-</sup> C <sub>6</sub> <sup>+</sup> , C <sub>6</sub> <sup>-</sup>	Capacitor connect pin for boost	30, 31 28, 29 26, 27 24, 25 22, 23 20, 21	–	To connect external capacitor for DC/DC converter. The capacitance and tolerance of each capacitor are shown below. Capacitance : 1 μF Withstanding voltage: 10 V

**4. MODE DESCRIPTION**

**(1) DC/DC converter control**

DCON	H	DC/DC converter ON
	L	DC/DC converter OFF

**(2) Regulator control**

RGONP	H	Regulator ON
	L	Regulator OFF ( $V_T$ , $V_S$ = High impedance)

**(3)  $V_T$  regulating resistor**

EXRV <sub>T</sub>	H	External resistor
	L	Internal resistor

**(4)  $V_S$  regulating resistor**

EXRV <sub>S</sub>	H	External resistor
	L	Internal resistor

**(5)  $V_{DD2}$  booster selection**

V <sub>CD2</sub>	H	x3 booster
	L	x2 booster

**(6)  $V_T$ ,  $V_S$  regulator selection**

		$V_T$	$V_S$
R <sub>SEL</sub>	H	15.0 V	5.0 V
	L	12.5 V	4.0 V

**(7) Regulator reference voltage input selection**

VREF <sub>SEL</sub>	H	V <sub>REF</sub> : External reference voltage input
	L	V <sub>REF</sub> : Internal reference voltage output

**(8) V<sub>DD1</sub> and V<sub>o</sub> high-level booster selection**

V <sub>CD12</sub>	V <sub>CD11</sub>	V <sub>CE</sub>	V <sub>DD1</sub> booster	V <sub>o</sub> high level
H	H	H	x7 V <sub>DC</sub>	x7 V <sub>DC</sub>
H	H	L	x7 V <sub>DC</sub>	x6 V <sub>DC</sub>
H	L	H	x6 V <sub>DC</sub>	x6 V <sub>DC</sub>
H	L	L	x6 V <sub>DC</sub>	x5 V <sub>DC</sub>
L	H	H	x5 V <sub>DC</sub>	x5 V <sub>DC</sub>
L	H	L	x5 V <sub>DC</sub>	x4 V <sub>DC</sub>
L	L	H	x4 V <sub>DC</sub>	x4 V <sub>DC</sub>
L	L	L	x4 V <sub>DC</sub>	x3 V <sub>DC</sub>

**(9) Amp. current selection**

		V <sub>T</sub>			V <sub>s</sub>		
ACS <sub>0</sub> <sup>Note</sup> (LACS <sub>0</sub> )	ACS <sub>1</sub> <sup>Note</sup> (LACS <sub>1</sub> )	Source current	Sink current	Amp. current	Source current	Sink current	Amp. current
L	L	1 mA >	0.5 μA	1 μA	3 mA >	0.5 μA	1 μA
L	H	1 mA >	1 μA	2 μA	3 mA >	1 μA	2 μA
H	L	1 mA >	2.5 μA	5 μA	3 mA >	2.5 μA	5 μA
H	H	1 mA >	5 μA	10 μA	3 mA >	5 μA	10 μA

**Note** ACS<sub>0</sub>, ACS<sub>1</sub> : Current selection in scanning time  
 LACS<sub>0</sub>, LACS<sub>1</sub>: Current selection in low power mode

**(10) OSC frequency selection**

FS <sub>1</sub> , LFS <sub>1</sub> <sup>Note</sup>	FS <sub>0</sub> , LFS <sub>0</sub> <sup>Note</sup>	OSC
L	L	f <sub>osc</sub> /8
L	H	f <sub>osc</sub> /2
H	L	f <sub>osc</sub> /32
H	H	f <sub>osc</sub> /256

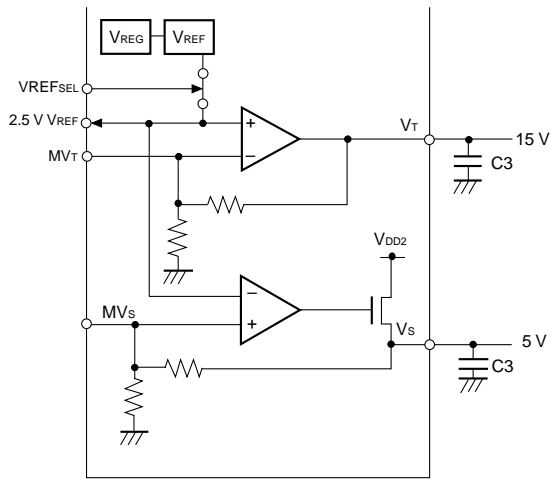
**Note** FS<sub>0</sub>, FS<sub>1</sub> : Current selection when in scanning  
 LFS<sub>0</sub>, LFS<sub>1</sub>: Current selection in low power mode

**(11) Low power mode selection**

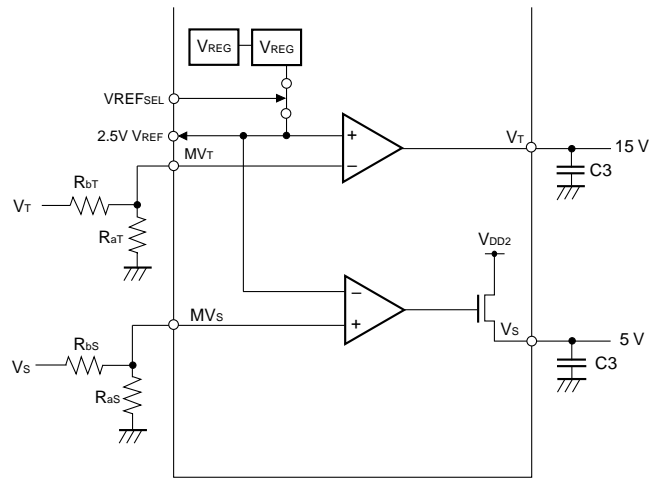
LPM	H	Low power mode LACS <sub>0</sub> , LACS <sub>1</sub> , LFS <sub>0</sub> , LFS <sub>1</sub> are enable.
	L	Normal mode ACS <sub>0</sub> , ACS <sub>1</sub> , FS <sub>0</sub> , FS <sub>1</sub> are enable.



Figure 4-1. Example of Internal/External resistor for the regulator



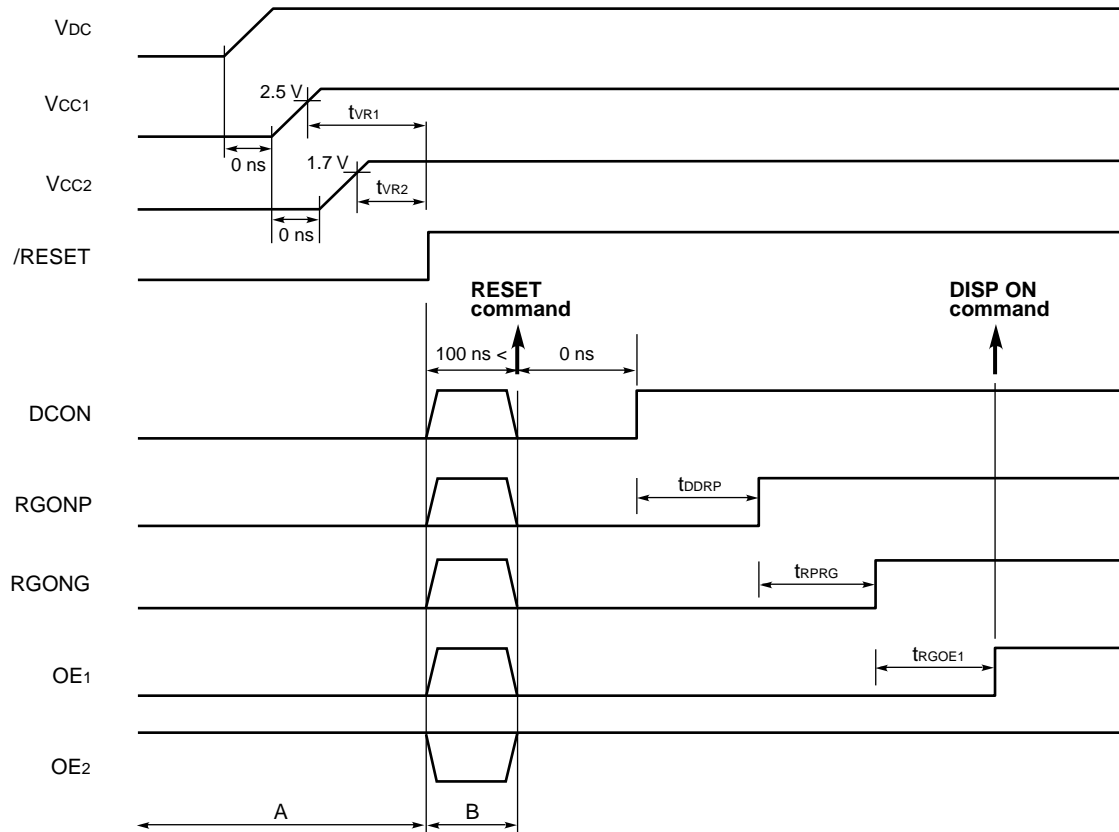
Internal Resistor Mode  
 EXRV<sub>T</sub> = L  
 EXRV<sub>S</sub> = L



External Resistor Mode  
 EXRV<sub>T</sub> = H  
 EXRV<sub>S</sub> = H  
 $V_T = (1 + \frac{R_{bT}}{R_{aT}}) V_{REF}$   
 $V_S = (1 + \frac{R_{bS}}{R_{aS}}) V_{REF}$

5. POWER ON/OFF SEQUENCE

5.1 Power ON sequence



t<sub>VR1</sub>, t<sub>VR2</sub> = 100 ns MIN.

**Remarks 1.** /xxx indicates active low signal.

2. OE<sub>1</sub>, OE<sub>2</sub>, /RESET, RGONG, RGONP, V<sub>CC2</sub> are signals from source driver.

① All three power supplies, V<sub>DC</sub>, V<sub>CC1</sub>, and V<sub>CC2</sub>, can be on at the same time.

② The pins are fixed to the following levels by the source driver during the period of /RESET = L (A period).

Note that the gate output is fixed to the V<sub>B</sub> level, and the DC/DC converter and the regulators are off.

DCON, RGONG, RGONP, OE<sub>1</sub>: L (low level)

OE<sub>2</sub>: H (high level)

③ The /RESET pin can be made high at the end of both t<sub>VR1</sub>, which starts from the rising edge of V<sub>CC1</sub>, and t<sub>VR2</sub>, which starts from the rising edge of V<sub>CC2</sub>.

④ The wait time between when the /RESET signal rises and when the RESET command is acknowledged must be at least 100 ns.

⑤ The logical status of the DCON, RGONG, RGONP, OE<sub>1</sub>, and OE<sub>2</sub> pins in the period between when the /RESET signal rises and when the RESET command (↑part) is acknowledged (B period) is undefined. Be aware, therefore,

that the gate output may be undefined and the DC/DC converter and the regulators may be on. If the B period is sufficiently short however, it is unlikely that the display will be affected. Note that the gate output MAX value in the B period must be determined separately as a specification of the LCD module.

The pins are re-fixed to the following levels by the source driver when the RESET command is input.

Note that the gate output is fixed to the  $V_B$  level, and the DC/DC converter and the regulators are off.

DCON, RGONG, RGONP, OE<sub>1</sub>: L (low level)

OE<sub>2</sub>: H (high level)

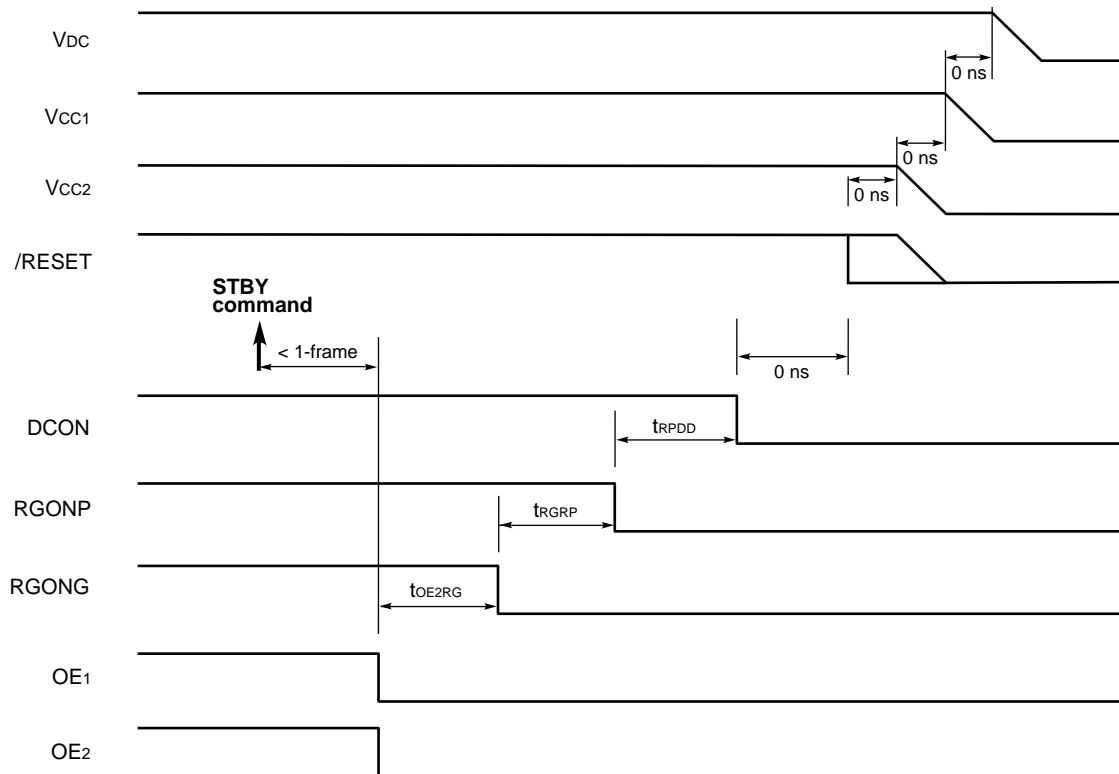
- ⑦ Set a timing that ensures the DCON, RGONP, and RGONG pins are shifted to high level in that order after the RESET command is input. At this time, the DC/DC converter and the regulators are on. Before that, the booster level must have been set up (by BGRS,  $V_{CE}$ ,  $V_{CD2}$ , PVCOM of R32 register and R34 register of the  $\mu$ PD161620). Note that the target timing of  $t_{DDRP}$  and  $t_{RPRG}$  (while the DC/DC converter output and regulator output is stable) is  $t_{DDRP} = \text{approx. } 50 \text{ ms}$  and  $t_{RPRG} = \text{approx. } 20 \text{ ms}$ , but users are requested to set the final timing after sufficiently evaluating the  $\mu$ PD161660 in the LCD module.

- ⑧ Input the DISPON command ( $\uparrow$ part) after ensuring that all the power supplies are high level.

The source driver will start display with OE<sub>1</sub> = H.

The target is  $t_{RGOE1} = \text{approx. } 1 \text{ ms}$ , but users are requested to set the final timing after sufficiently evaluating the  $\mu$ PD161660 in the LCD module.

5.2 Power OFF sequence



**Remark** OE1, OE2, /RESET, RGONG, RGONP, VCC2 are the signals from driver.

① Input the STBY command (↑part).

The source driver sets the status of the OE1 and OE2 pins to low level within one frame.

The gate output is fixed to VT.

② Set a timing that ensures the RGONG, RGONP, and DCON pins are shifted to low level in that order after the panel load has been sufficiently discharged (tOE2RG timing; Secure an amount of time equivalent to one frame after executing the standby command). At this time, the DC/DC converter and the regulators are off.

Note that a timing of 0 ns for tRGRP and tRPDD causes no problems on the device side, but users are requested to set the final timing after sufficiently evaluating the μPD161660 in the LCD module.

③ Although it is unnecessary to input the RESET command to the source driver, for designs in which the system is reset when the power supply is turned off, make settings that ensure /RESET = L at DCON = L and subsequent timings.

④ All three power supplies, VDC, VCC1, and VCC2, can be off at the same time.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>CC1</sub>	-0.5 to +6.0	V
Supply voltage	V <sub>DC</sub>	-0.5 to +6.0	V
Input voltage	V <sub>I</sub>	-0.5 to V <sub>CC1</sub> + 0.5	V
Input current	I <sub>I</sub>	±10	mA
Output voltage	V <sub>DD1</sub>	-0.5 to +40	V
Output current	I <sub>O</sub>	±10	mA
Output current	I <sub>O2</sub>	±10	mA
Operating ambient temperature	T <sub>A</sub>	-40 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T<sub>A</sub> = -40 to +85°C, V<sub>SS</sub> = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC1</sub>	2.5	2.7	3.6	V
Supply voltage	V <sub>DC</sub>	2.5		3.6	V
Input voltage	V <sub>I</sub>	0		V <sub>CC1</sub>	V

Electrical Characteristics (Unless otherwise specified, T<sub>A</sub> = -40 to +85°C, V<sub>CC1</sub> = 2.5 to 3.6 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V <sub>IH</sub>		0.8 V <sub>CC1</sub>			V
Low level input voltage	V <sub>IL</sub>				0.2 V <sub>CC1</sub>	V
Boost voltage	V <sub>DD1</sub>	I <sub>DD1</sub> = 300 μA, 7 x Boost	6 V <sub>DC</sub>		7 V <sub>DC</sub>	V
Boost voltage	V <sub>DD1</sub>	I <sub>DD1</sub> = 300 μA, 6 x Boost	5 V <sub>DC</sub>		6 V <sub>DC</sub>	V
Boost voltage	V <sub>DD1</sub>	I <sub>DD1</sub> = 300 μA, 5 x Boost	4 V <sub>DC</sub>		5 V <sub>DC</sub>	V
Boost voltage	V <sub>DD1</sub>	I <sub>DD1</sub> = 300 μA, 4 x Boost	3 V <sub>DC</sub>		4 V <sub>DC</sub>	V
Boost voltage	V <sub>DD2</sub>	V <sub>CD2</sub> = L, I <sub>DD2</sub> = 1 mA	1.8 V <sub>DC</sub>		2 V <sub>DC</sub>	V
Boost voltage	V <sub>DD2</sub>	V <sub>CD2</sub> = H, I <sub>DD2</sub> = 1 mA	2.7 V <sub>DC</sub>		3 V <sub>DC</sub>	V
Output voltage	V <sub>T</sub>	R <sub>SEL</sub> = H	13.5	15	16.5	V
Output voltage	V <sub>T</sub>	R <sub>SEL</sub> = L	11.25	12.5	13.75	V
Output voltage	V <sub>S</sub>	R <sub>SEL</sub> = H	4.5	5	5.5	V
Output voltage	V <sub>S</sub>	R <sub>SEL</sub> = L	3.6	4	4.4	V
★ V <sub>CC1</sub> static current	I <sub>VCC1d</sub>	V <sub>CC1</sub> = 2.7 V, DCON, RGONG, RGONP = L			5	μA
★ V <sub>DC</sub> static current	I <sub>VDCd</sub>	V <sub>DC</sub> = 2.5 V, DCON, RGONG, RGONP = L			5	μA
V <sub>REF</sub> voltage			2.25	2.5	2.75	V

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of May, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
  - No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
  - NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
  - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
  - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
  - NEC semiconductor products are classified into the following three quality grades:  
"Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
    - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
    - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
    - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
- (Note)
- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  - (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).