

## 120-/128-OUTPUT TFT-LCD GATE DRIVER

The  $\mu$ PD16650 is a TFT-LCD gate driver. Provided with a level shift circuit at the logic input, this chip can output a high gate scan voltage for a CMOS-level input. The  $\mu$ PD16650 has an output change-over function for switching from the 120-output mode to the 128-output mode, and vice versa, thereby supporting the VGA, SVGA, and XGA panels. Its output enable function ( $\overline{OE}$ ) enables installing the driver on either side.

## FEATURES

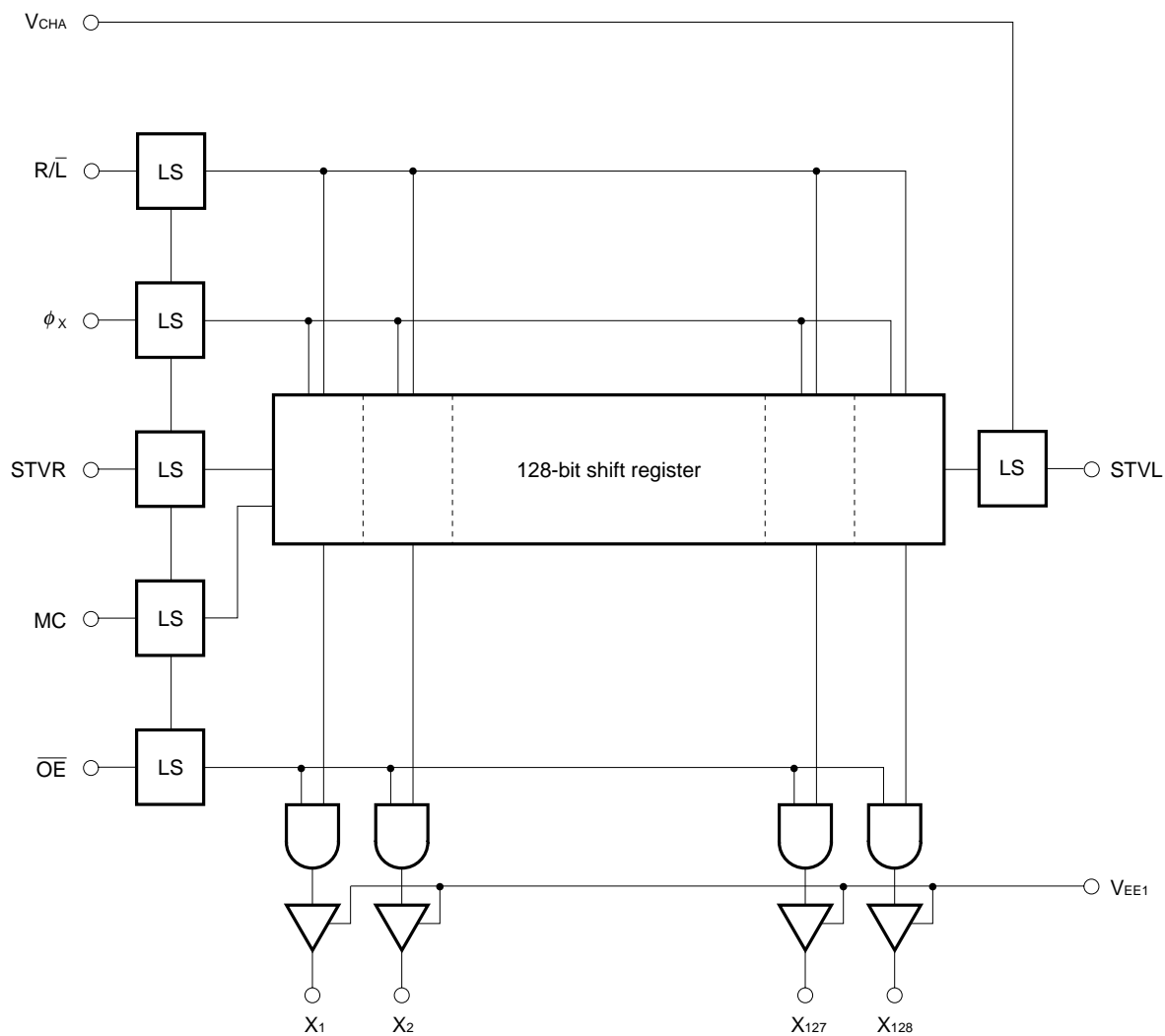
- Output with high dielectric strength (on/off range:  $V_{DD} - V_{EE1} = 40 V_{MAX.}$ )
- Built-in shift direction change-over function
- Shiftable negative supply voltage ( $V_{EE1}$ ) level (shift range:  $|V_{EE1} - V_{EE2}| = 10 V$ )
- Two acceptable CMOS input levels (3.3 and 5 V)
- Output enable function
- MC-selectable output count (MC = high: 120-output mode)  
(MC = low : 128-output mode)
- Slim TCP

## ORDERING INFORMATION

Part number	Package
$\mu$ PD16650N-xxx	TCP (TAB package)
$\mu$ PD16650N-xxx	Standard TCP (OL pitch = 220 $\mu$ m)

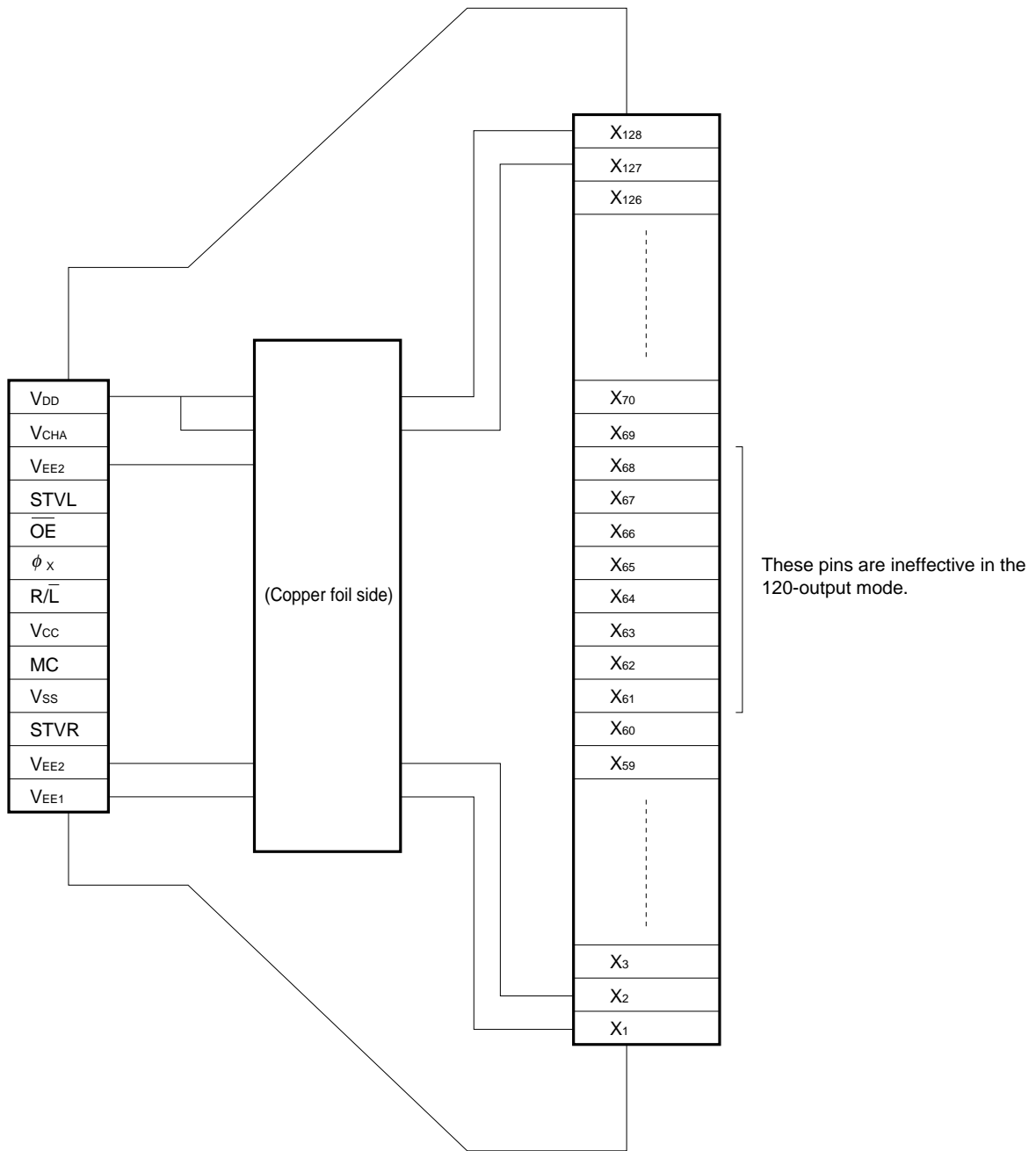
**Remark** When ordering, the customer can specify the external form of the TCP. Call one of our sales representatives for more information.

BLOCK DIAGRAM



**Remark** LS (level shifter): Interfaces the 5 V CMOS level with the  $V_{DD}$ - $V_{EE2}$  level.

PIN CONNECTION DIAGRAM (μPD16650N-xxx)



**Caution** The V<sub>CHA</sub> pin should be connected to the V<sub>DD</sub> or V<sub>EE2</sub> pin on the TCP. (This method eliminates the necessity to provide the V<sub>CHA</sub> input pin on the TCP, resulting in a reduction in the number of required input pins.)

## PIN DESCRIPTION

Pin symbol	Pin name	Description of function
X <sub>1</sub> to X <sub>128</sub>	Driver output	Output scan signals to drive the TFT-LCD gate electrodes. The output changes when the shift clock $\phi_x$ rises. The amplitude of the driver output is $V_{DD} - V_{EE1}$ . See the timing charts shown later for details of how to switch between the 120-output mode and 128-output mode.
MC	Output count change-over input	Receives a signal that changes the number of outputs. For the 120-output mode, this pin must be supplied with a high level ( $V_{CC}$ ). For the 128-output mode, it must be supplied with a low level ( $V_{SS}$ or $V_{EE2}$ ).
V <sub>CHA</sub>	Logic voltage change-over input	Must be supplied with the $V_{EE2}$ level when the logic supply voltage is 3.3 V, and with the $V_{DD}$ level when the logic supply voltage is 5.0 V.
STVR STVL	Start pulse input/output	Receives an input to the internal shift register. The input data is loaded on the shift register at the positive-going edge of the shift clock $\phi_x$ . The scan signals are output from X <sub>1</sub> to X <sub>128</sub> . The input/output level is the CMOS level.  Outputs a start pulse to the next stage if a cascade connection is used. In the 120-output mode, the start pulse is output at the negative-going edge of the 120th shift clock $\phi_x$ pulse, and cleared at the negative-going edge of the 121st pulse. In the 128-output mode, the start pulse is output at the negative-going edge of the 128th shift clock $\phi_x$ pulse, and cleared at the negative-going edge of the 129th pulse.
R/L	Shift direction change-over input	R/L = high (for shift right): STVR → X <sub>1</sub> → X <sub>128</sub> → STVL R/L = low (for shift left) : STVL → X <sub>128</sub> → X <sub>1</sub> → STVR
$\phi_x$	Shift clock input	Receives a shift clock pulse for the internal shift register. A shift occurs at the positive-going edge of the shift clock pulse.
$\overline{OE}$	Output enable input	When this pin is at a high level, the driver output is fixed at a low level. The shift register is not cleared, however. The internal logic circuit operates even when the pin is at a high level. The signal supplied to this pin is not synchronized with the clock.
V <sub>DD</sub>	Driver positive supply voltage	Receives the supply voltage for both the logic circuit and driver.
V <sub>CC</sub>	Reference voltage	5 ±0.5 V/3.3 ±0.3 V Reference voltage for the LS1 and LS2 level shifters.
V <sub>SS</sub>	Ground	Must be connected to the system ground.
V <sub>EE1</sub>	Driver negative supply voltage	V <sub>EE1</sub> (for the driver)
V <sub>EE2</sub>	Driver negative supply voltage	V <sub>EE2</sub> (for the logic circuit)

**CAUTIONS FOR USE**

1) Power-on sequence

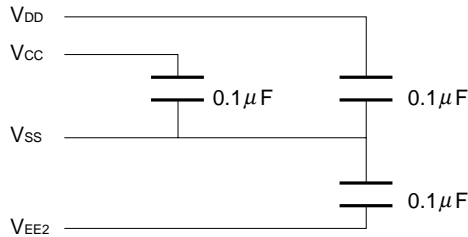
To prevent latch-up disruption, the power must be switched on in the order:

$V_{CC} \rightarrow V_{EE1} \rightarrow V_{EE2} \rightarrow V_{DD} \rightarrow$  Logic input

When switching off, reverse the order. This order must be observed also during transition.

2) Insertion of bypass capacitors

The internal logic circuit operates at a high voltage. To make  $V_{IH}$  and  $V_{IL}$  immune to noise, use capacitors of  $0.1 \mu\text{F}$  or so between supply voltages as shown below.



3) Negative voltage level shift

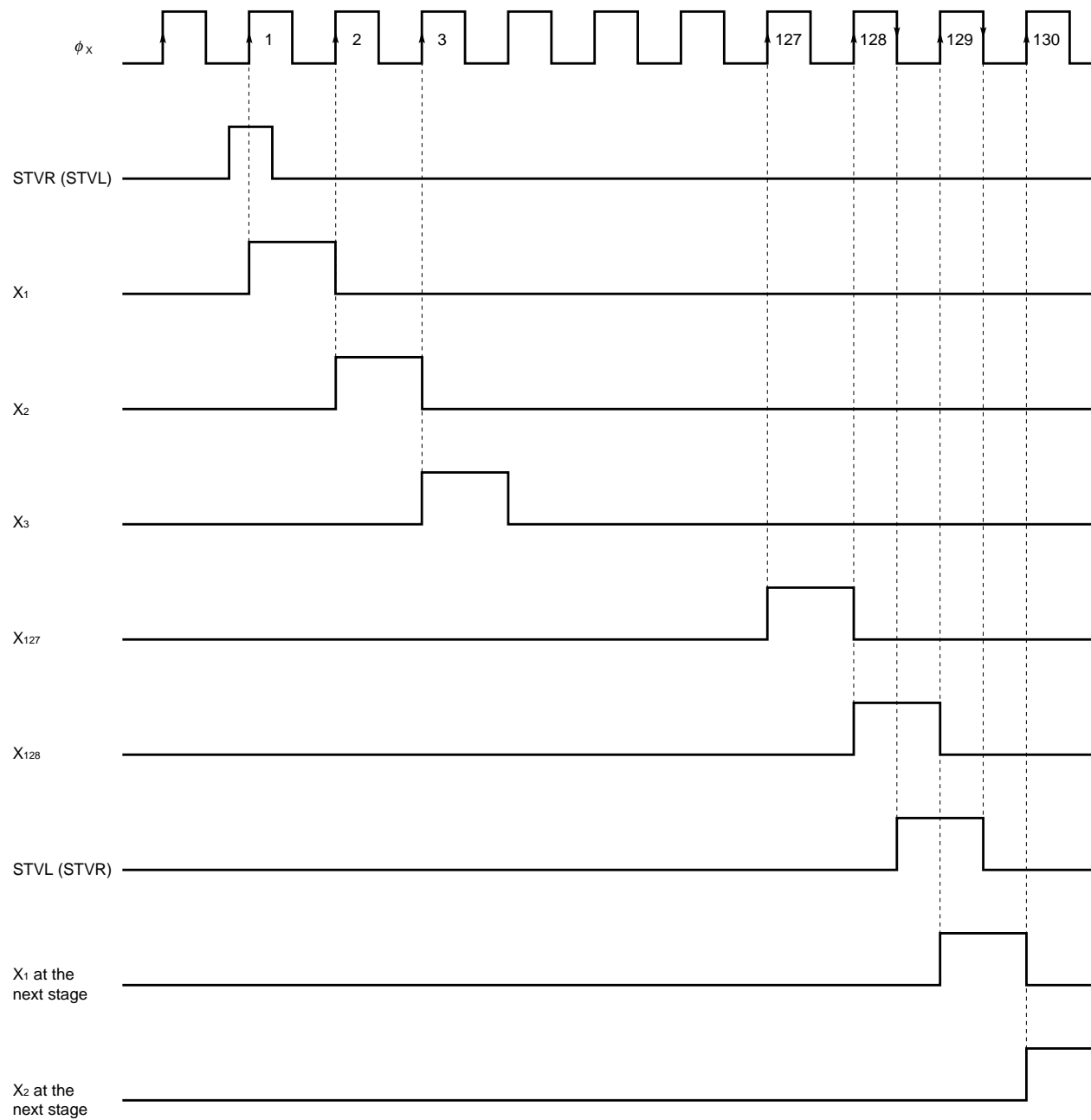
If it is necessary to shift the level of a negative supply voltage, shift the  $V_{EE1}$  (driver supply voltage) level. The shift should be limited to within:  $V_{EE2} \leq V_{EE1} \leq V_{EE2} + 10 \text{ V}$

Note that shifting the  $V_{EE1}$  level results in the ON-state output resistance and output fall time ratings being changed.

4) Handling the  $V_{EE1}$  and  $V_{EE2}$  driver negative supply voltage pins

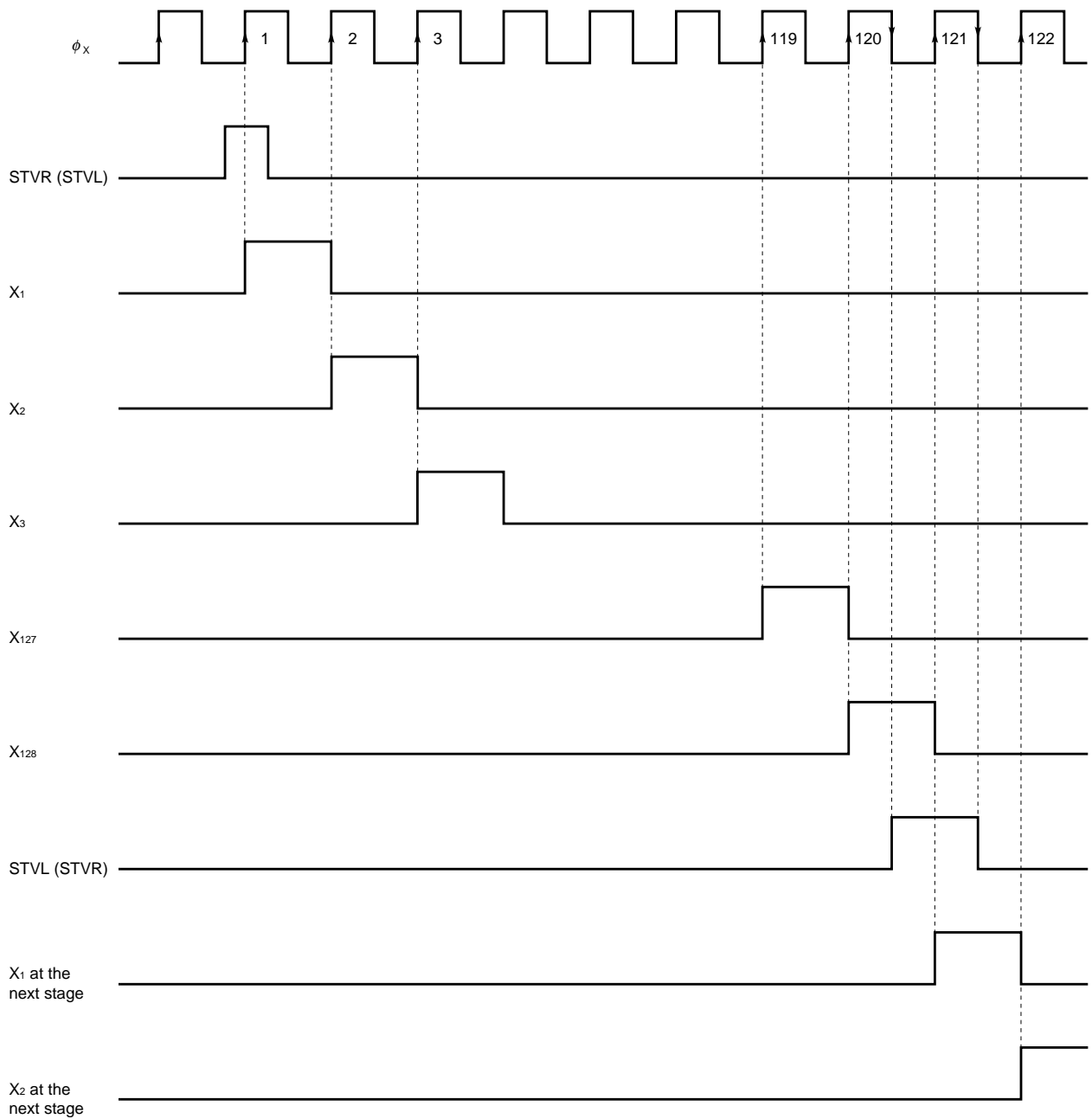
For applications in which a negative supply voltage level is not shifted, connect the  $V_{EE1}$  pin (driver supply voltage) to the  $V_{EE2}$  pin (logic supply voltage) outside the TCP. Fix all unused input pins to the  $V_{EE2}$  level.

**TIMING CHART (MC = V<sub>SS</sub>, 128-OUTPUT MODE, AND R/L = V<sub>CC</sub>)**



**Caution** Do not change all outputs simultaneously, because such a sequence may result in malfunction.

**TIMING CHART (MC = V<sub>CC</sub>, 120-OUTPUT MODE, AND R/L = V<sub>CC</sub>)**



**Cautions** 1. Do not change all outputs simultaneously, because such a sequence may result in malfunction.

2. The output sequence in the 120-output mode is as follows:

STVR (STVL) → X<sub>1</sub> → X<sub>2</sub> ... X<sub>60</sub> → X<sub>69</sub> ... X<sub>127</sub> → X<sub>128</sub> → STVL (STVR)

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	Rated value	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +28	V
Supply voltage	V <sub>CC</sub>		-0.5 to +7	V
Supply voltage	V <sub>DD</sub> -V <sub>EE1</sub> V <sub>DD</sub> -V <sub>EE2</sub>		-0.5 to +42	V
Supply voltage	V <sub>EE1</sub> , V <sub>EE2</sub>		-22 to +0.5	V
Input voltage	V <sub>I</sub>		V <sub>EE2</sub> - 0.5 to V <sub>DD2</sub> + 0.5	V
Input current	I <sub>I</sub>		±10	mA
Output current	I <sub>O</sub>		±10	mA
Operating temperature range	T <sub>A</sub>		-20 to +85	°C
Storage temperature range	T <sub>stg.</sub>		-55 to +125	°C

**RECOMMENDED OPERATING RANGES (T<sub>A</sub> = -20 °C to +70 °C, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>		16		25	V
Supply voltage	V <sub>EE1</sub>		V <sub>EE2</sub>		V <sub>EE2</sub> + 10	V
Supply voltage	V <sub>EE2</sub>		-20		0	V
Supply voltage	V <sub>DD</sub> -V <sub>EE1</sub> V <sub>DD</sub> -V <sub>EE2</sub>		20		40	V
Supply voltage	V <sub>CC</sub>	For the 3.3 V logic input	3.0	3.3	3.6	V
Supply voltage	V <sub>CC</sub>	For the 5.0 V logic input	4.5	5.0	5.5	V

**Remark** When shifting the level of V<sub>EE1</sub> (driver supply voltage), satisfy the condition:

$$V_{EE2} \leq V_{EE1} \leq V_{EE2} + 10 \text{ V}$$

Note that shifting the V<sub>EE1</sub> level results in the ON-state output resistance and output fall time ratings being changed.

**ELECTRICAL CHARACTERISTICS**

(T<sub>A</sub> = -20 °C to +70 °C, V<sub>DD</sub> = 20 V, V<sub>EE1</sub> = V<sub>EE2</sub> = -20 V, V<sub>CC</sub> = 3.3 ±0.3 V or 5.0 ±0.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V <sub>IH</sub>	Other than V <sub>CHA</sub>	0.7V <sub>CC</sub>		V <sub>CC</sub>	V
Input low voltage	V <sub>IL</sub>	Other than V <sub>CHA</sub>	V <sub>EE2</sub>		0.3V <sub>CC</sub>	V
Output high voltage	V <sub>OH</sub>	STVR(STVL), I <sub>OH</sub> = -40 μA	V <sub>CC</sub> - 0.4		V <sub>CC</sub>	V
Output low voltage	V <sub>OL</sub>	STVR(STVL), I <sub>OL</sub> = 40 μA	V <sub>SS</sub>		V <sub>SS</sub> + 0.4	V
Output high current	I <sub>XOH</sub>	X <sub>n</sub> , V <sub>X</sub> = V <sub>DD</sub> - 1 V			-1.5	mA
Output low current	I <sub>XOL</sub>	X <sub>n</sub> , V <sub>X</sub> = V <sub>EE1</sub> + 1 V	1.5			mA
ON-state output resistance	R <sub>ON1</sub>	V <sub>X</sub> = V <sub>EE1</sub> + 1 V or V <sub>DD</sub> - 1 V			660	Ω
Input leakage current	I <sub>IL</sub>	V <sub>I</sub> = 0 V, 5.0 V, or 3.3 V			±1.0	μA
Dynamic drain current	I <sub>DD</sub>	V <sub>DD</sub> , f <sub>φX</sub> = 31.5 kHz		0.5	1.0	mA
	I <sub>EE</sub>	V <sub>EE1/2</sub> , f <sub>φX</sub> = 31.5 kHz		-0.5	-1.0	mA
	I <sub>CC</sub>	V <sub>CC</sub> , f <sub>φX</sub> = 31.5 kHz		50	100	μA



**SWITCHING CHARACTERISTICS**

( $T_A = -20\text{ °C to }+70\text{ °C}$ ,  $V_{DD} = 20\text{ V}$ ,  $V_{EE1} = V_{EE2} = -20\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{CC} = 3.3 \pm 0.3\text{ V or }5.0 \pm 0.5\text{ V}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STVR and STVL output delay	$t_{PHL1}$	$C_L = 20\text{ pF}$			600	ns
	$t_{PLH1}$	CLK → STVR(STVL)			600	ns
Driver output delay	$t_{PHL2}$	$C_L = 220\text{ pF}$			700	ns
	$t_{PLH2}$	CLK → $X_n$			700	ns
	$t_{d1}$	$C_L = 220\text{ pF}$ , $\overline{OE}$ : L → H			700	ns
	$t_{d2}$	$C_L = 220\text{ pF}$ , $\overline{OE}$ : H → L			700	ns
Output rise time	$t_{THL}$	$C_L = 220\text{ pF}$			300	ns
Output fall time	$t_{TLH}$	$C_L = 220\text{ pF}$			300	ns
Input capacitance	$C_i$	$T_A = 25\text{ °C}$			15	pF
Maximum clock frequency	$f_{\phi x}$	For cascade connection	100			kHz

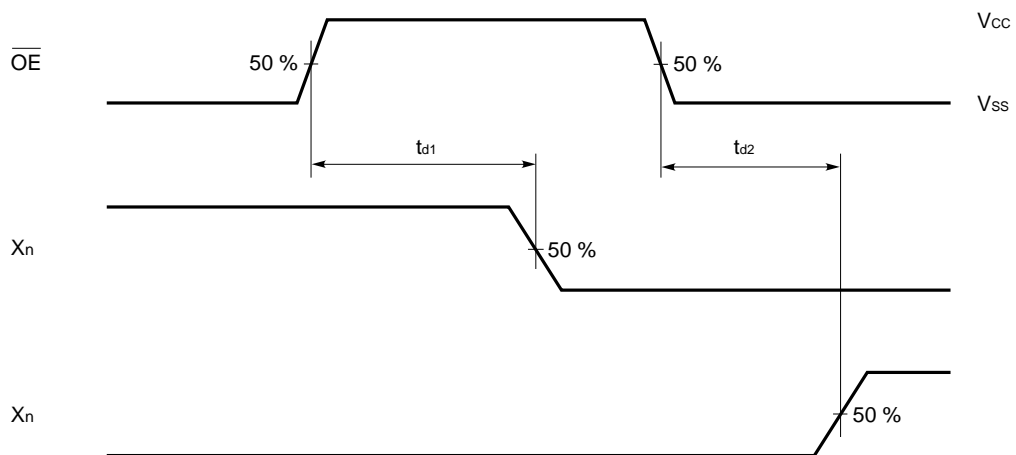
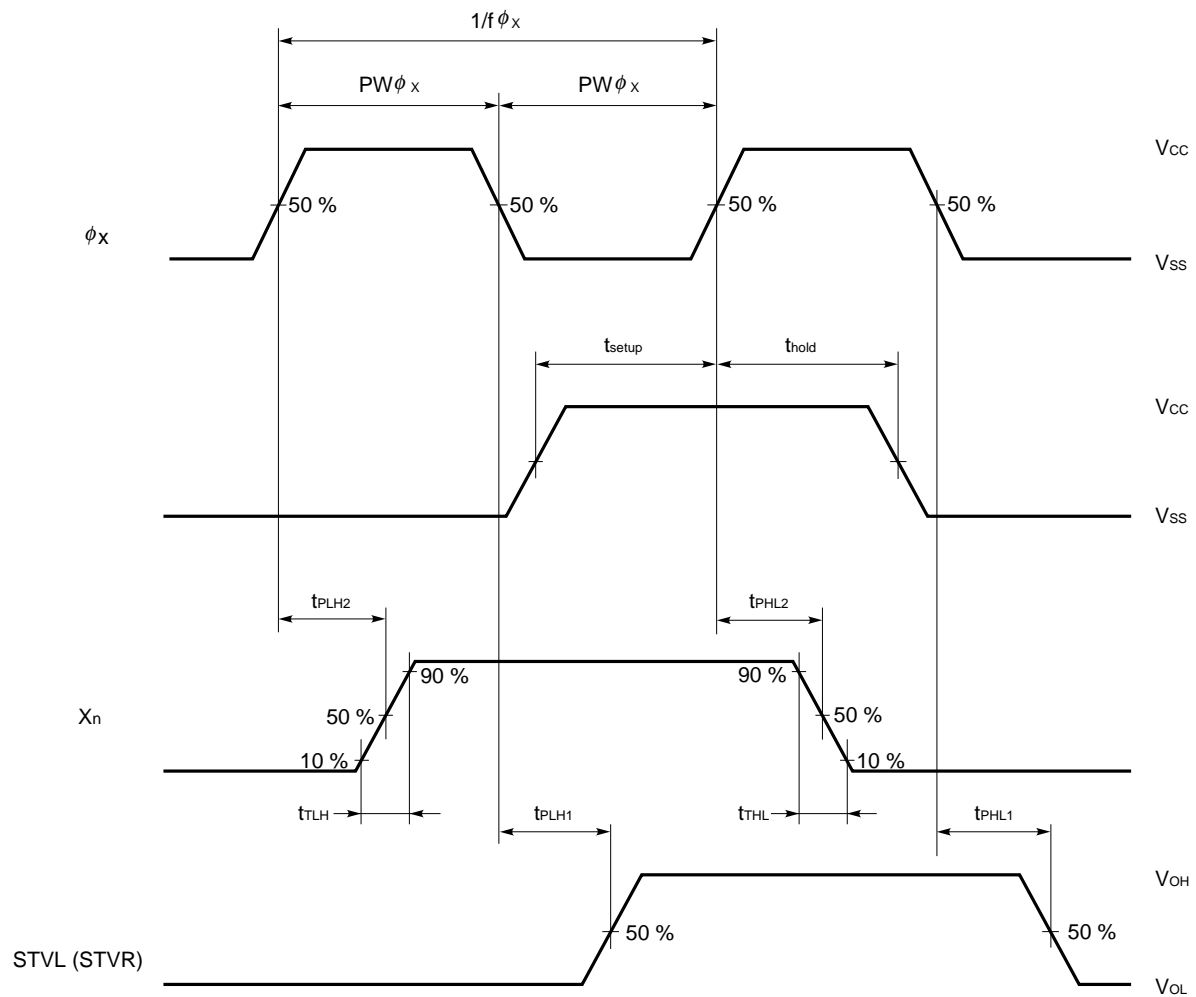
**TIMING REQUIREMENTS**

( $T_A = -20\text{ °C to }+70\text{ °C}$ ,  $V_{DD} = 20\text{ V}$ ,  $V_{EE1} = V_{EE2} = -20\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{CC} = 3.3 \pm 0.3\text{ V or }5.0 \pm 0.5\text{ V}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse high width	$PW_{\phi x(H)}$	Duty = 50 %	500			ns
Clock pulse low width	$PW_{\phi x(L)}$	Duty = 50 %	500			ns
Data setup time	$t_{setup}$	STVR(STVL) ↑ → CLK ↑	100			ns
Data hold time	$t_{hold}$	CLK ↑ → STVR(STVL) ↓	100			ns

**Remark** The logic input rise time ( $t_r$ ) and fall time ( $t_f$ ) must be within 20 ns (between 10 % and 90 % of the peak amplitude of the input).

SWITCHING CHARACTERISTIC WAVEFORM (R/L = HIGH)



**RECOMMENDED MOUNTING CONDITIONS**

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

**μPD16650N-xxx**

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF (Sheet-shape bonding agent)	Temporary bonding 70 to 100 °C; pressure 3 to 8 kg/cm <sup>2</sup> ; time 3 to 5 secs. Real bonding 165 to 180 °C; pressure 25 to 45 kg/cm <sup>2</sup> ; time 30 to 40 secs. (when using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

**Caution** To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

**Reference**

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grades to NEC's Semiconductor Devices (IEI-1209)

## [MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customer must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

“Standard”, “Special”, and “Specific”. The Specific quality grade applies only to devices developed based on a customer designated “quality assurance program” for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in “Standard” unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.