

mos integrated circuit $\mu PD16667$

160-OUTPUT LCD ROW DRIVER

The μ PD16667 is a row (common) driver which contains a RAM capable of full-dot LCD display. With 160 outputs, this driver can be combined with a column (segment) driver, μ PD16662, which contains a RAM to display 240 \times 160 pixels to 480 \times 320 pixels.

With a built-in display RAM, the column driver can reduce the current consumption, thus making it most suitable for the display block of a PDA or portable terminal.

FEATURES

LCD-driven voltage: 20 to 36 V

• Duty: 1/160

Driving type: 2 lines selected simultaneously

• Output count: 160 outputs

• Capable of gray scale display: 4 gray scales

ORDERING INFORMATION

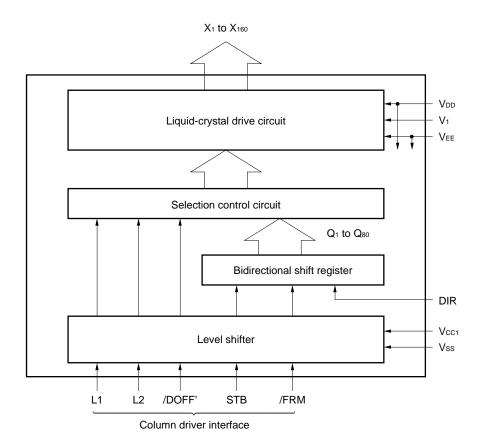
Part No.	Package			
μPD16667N-XXX	TCP (TAB)			
μPD16667N-051	Standard TCP (OLB: 0.2 mm pitch, folding)			

The external shape of the TCP is custom-made, so please contact an NEC sales representative with your shape requirements.

*



BLOCK DIAGRAM



Remark /xxx indicates active low signal.

BLOCK FUNCTION

1. Liquid-crystal drive circuit

This circuit selects and outputs the level for liquid-crystal driving.

One of V_{DD} , V_{EE} , and V_1 is selected by the output of the selection control circuit.

2. Selection control circuit

This circuit creates the signal which will select the level of the output signal, based on the output of the shift register circuit and the driving level power selection signals L1 and L2

3. Bidirectional shift register circuit

This refers to the 80-bit bidirectional shift register circuit. The DIR signal can be used to switch over the shift direction.

The data that has been entered from the /FRM pin is shifted by the low drive signal strobe (STB).

4. Level shifter circuit

This circuit transforms the 5-V signals to the high-voltage signals for liquid-crystal driving.



PIN FUNCTIONS

Classification	Pin Name	Input/Output	Pad No.	Function
Power suuply	Vcc1 Vss VDD VEE V1			5 V power for level shifter GND for level shifter Power for logic, liquid-crystal drive level power Power for logic, liquid-crystal drive level power (GND) Liquid-crystal drive level power
Liquid-crystal display timing	STB /FRM /DOFF' L1 L2 DIR	 		Row drive signal strobe Frame signal Display OFF signal Drive level power selection symbol (1st line) Drive level power selection symbol (2nd line) Shift direction selection symbol: when L (DIR = V_{EE}), $X_1 \rightarrow X_{160}$ when H (DIR = V_{DD}), $X_{160} \rightarrow X_{1}$
Liquid-crystal drive output	X1 to X160	0		Liquid-crystal drive output Selects and outputs one of VDD, VEE, and V1.

DETAILS OF PIN FUNCTIONS

• STB (input)

Input pin of the row drive strobe signal

The bidirectional shift register is shifted at STB's rising edge.

/FRM (input)

Input pin of the frame signal

The shift register data is read at STB's rising edge.

DIR (input)

Input pin of the drive output's shift direction selection signal

When the shift direction selection signal (DIR) is "L", the shift data (selection signal) is shifted from the drive output X_1 to the X_{160} direction. When "H", it is shifted from the X_{160} to the X_1 direction.

• /DOFF' (input)

Input pin of the display OFF signal

It is placed in the display OFF status (all outputs at V_1) at the "L" level. In the mean time, it reads the frame signal and returns to the normal display status at the "H" level.

L1 and L2 (input)

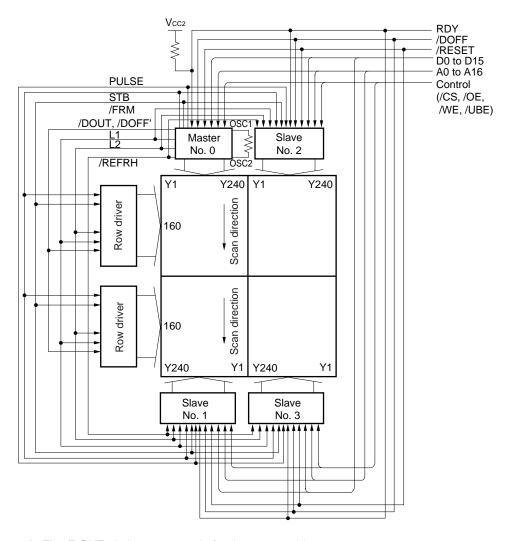
Input pins of the drive level power selection signal

In the case of the liquid-crystal drive output, the two lines are selected simultaneously by the shift register. L1 selects the first line, and L2 selects the second line. Both lines select V_{DD} at "H", and V_{EE} at "L".

* SYSTEM CONFIGURATION EXAMPLE

This example shows configuration of a liquid-crystal panel of half-VGA size (480 x 320 oblong) using four column drivers and two row drivers.

- Each column driver sets the LSI No. with PL0 and PL1 pins.
- The DIR pins of each column driver are all set to low level.
- Only one of the column drivers is set to the master, all the others are set to the slave. Signals are supplied from the master column driver to the slave column driver and the row driver.
- Connect an oscillator resistor to the OSC1 and OSC2 pins of the master, and leave the slave open.
- Inputs signals from the system (D0 to D15, A0 to A16, /CS, /OE, /WE, /UBE, RDY, /RESET, /DOFF') in parallel to all of the column driver. Connect a pull-up resistor to the RDY signal.
- The TEST pin is used to test the LSI, and is open or GND when the system is configured.



Remark The /DOUT pin is an output pin for the column driver.

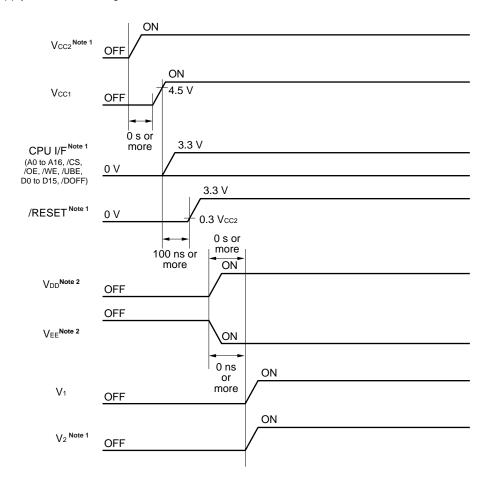


* POWER SUPPLY SEQUENCE OF CHIP SET

It is recommended to apply power in the following sequence.

 $Vcc2 \rightarrow Vcc1 \rightarrow input \rightarrow Vdd, Vee \rightarrow V1, V2$

Be sure to apply LCD drive voltages V1 and V2 last.



Notes 1. Vcc2, CPU I/F, /RESET, and V2 are column driver power supply pins or input pins.

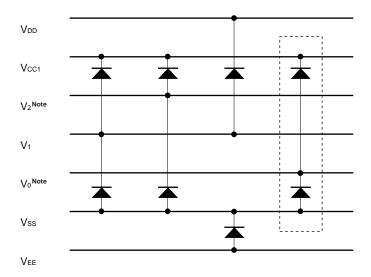
2. V_{DD} and V_{EE} do not need to be turned ON at the same time.

Caution Turn off the power to the chip set in the reverse order of the power application sequence.



EXAMPLE OF CONNECTING INTERNAL SCHOTTKY BARRIER DIODE OF MODULE TO REINFORCE POWER SUPPLY PROTECTION

(Use a schottky barrier diode with $V_f = 0.5 \text{ V}$ or less.)



Connect the diodes enclosed in the dotted line ($[\ \]\]$) when V_0 is not 0 V (GND)

Note V_0 and V_2 are column driver liquid-crystal power supplies.



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, Vss = 0 V)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	Vcc1		-0.5 to +6.5	V
	V _{DD} – V _{EE}	Vcc1 ≤ Vdd, Vee ≤ Vss	40	
	V ₁		VEE - 0.5 to VDD + 0.5	
Input voltage	VI1	Other than the DIR pin	-0.5 to Vcc1 + 0.5	
	Vı2	DIR pin	VEE - 0.5 to VDD + 0.5	
Output voltage	Vo		VEE - 0.5 to VDD + 0.5	
Operating temperature	TA		-20 to +70	°C
Storage temperature	T _{stg}		-40 to +125	

* Recommended Operating Range ($T_A = -20 \text{ to } +70 \text{ °C}, \text{ Vss} = 0 \text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc1		4.75		5.25	V
	V _{DD} - V ₁		10		18	
	V1 – VEE		10		18	
	V ₁		0		3	
Input voltage	Vıı	Other than DIR pin	0		Vcc1	
	V ₁₂	DIR pin	VEE		V _{DD}	

DC Characteristics (unless otherwise specified, $V_{CC1} = 4.75$ to 5.25 V, $V_{DD} - (V_{EE}) = 20$ to 31 V, $V_{CC1} \le V_{DD}$, $V_{EE} \le V_{SS}$, $V_1 = 0$ to 3 V, $V_{SS} = 0$ V, $V_{CC1} = 4.75$ to $V_{CC1} = 4.75$

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V _{IH1}	Other than the DIR pin	0.8 Vcc1			V
	V _{IH2}	DIR pin	V _{DD} - 0.3 (V _{DD} - V _{EE})			
Low-level input voltage	VIL1	Other than the DIR pin			0.2 Vcc1	
	VIL2	DIR pin			VEE+0.3 (VDD- VEE)	
Driver ON resistance	Ron	Load current = 100 μA		1.0	2.0	kΩ
Input leakage current	I _{IH1}	V _{IN} = V _{CC} , other than the DIR pin			1.0	μΑ
	I _{IH2}	VIN = VDD, DIR pin			25	
	l _{IL1}	$V_{IN} = 0 V$, other than the DIR pin			-1.0	
	I _{IL2}	VIN = VEE, DIR pin			-25	
Current consumption	Icc1	Operating frame frequency at		200	320	μΑ
	IDD	70 Hz		40	100	

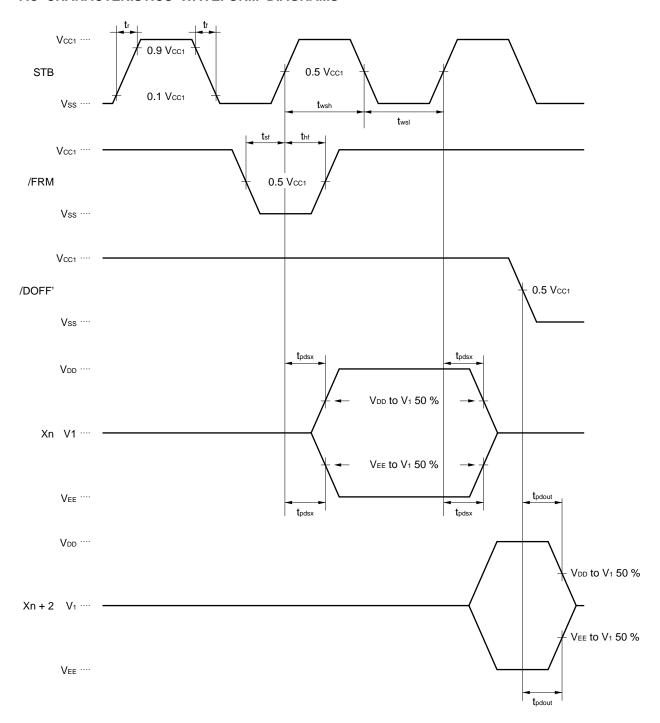


AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
STB high-level width	twsh		500			ns
STB low-level width	twsl		500			
/FRM setup time	t sf		100			
/FRM hold time	t hf		100			
STB rising time	t r				150	
STB falling time	t f				150	
Output delay time	t pdsx	Output no-load			300	
	tpdout				200	



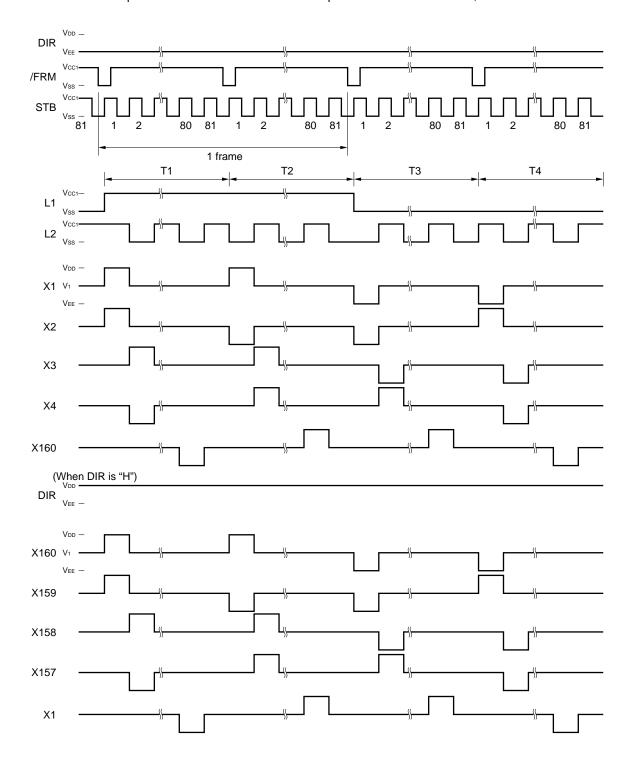
AC CHARACTERISTICS WAVEFORM DIAGRAMS





LEVEL SELECTION TIMING OF LIQUID-CRYSTAL DRIVE OUTPUT

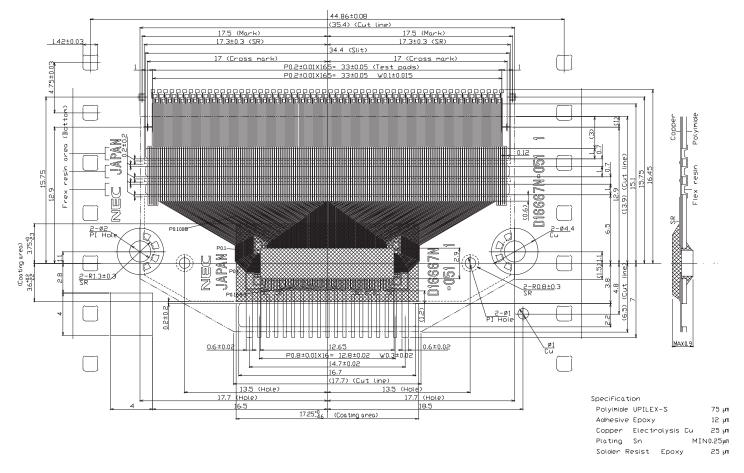
The /FRM is input twice in one frame. The STB is input 81 times in half a frame, and 162 times in one frame.



Remark When /DOFF' is "L", the X output becomes V₁ level. Afterward, if /DOFF' becomes "H", the level of the X output is output with the above timing.

Caution When the time difference between the STB, L1, and L2 signals is large, hazards may occur in output.

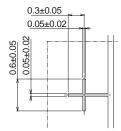
STANDARD TCP PACKAGE (µPD16667N-051)



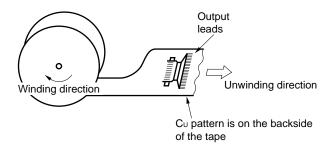
This products is Frex resin type
This Figure is shown by Copper side
over Polyimide
SSprocket holes(23.75 mm)for 1 Pattern
Corner radius is 0.30 mm Max.
All tolerances unless otherwise
specified 0.05 mm.



Detail of cross mark

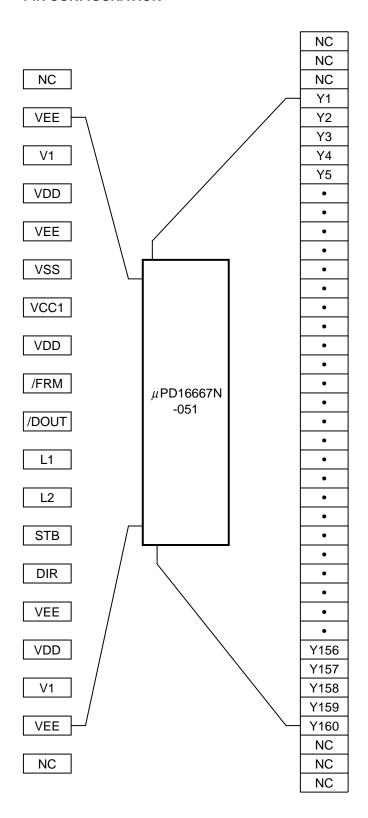


TCP tape winding direction





PIN CONFIGURATION



NEC μ PD16667

[MEMO]

NEC μ PD16667

[MEMO]



No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.