## 160-OUTPUT LCD ROW DRIVER

The $\mu$ PD16667 is a row (common) driver which contains a RAM capable of full-dot LCD display. With 160 outputs, this driver can be combined with a column (segment) driver, $\mu$ PD16662, which contains a RAM to display $240 \times 160$ pixels to $480 \times 320$ pixels.

With a built-in display RAM, the column driver can reduce the current consumption, thus making it most suitable for the display block of a PDA or portable terminal.

## FEATURES

- LCD-driven voltage: 20 to 36 V
- Duty: $1 / 160$
- Driving type: 2 lines selected simultaneously
- Output count: 160 outputs
- Capable of gray scale display: 4 gray scales


## ORDERING INFORMATION

| Part No. | Package |
| :--- | :--- |
| $\mu$ PD16667N-XXX | TCP (TAB) |
| $\mu$ PD16667N-051 | Standard TCP (OLB: 0.2 mm pitch, folding) |

The external shape of the TCP is custom-made, so please contact an NEC sales representative with your shape requirements.

## BLOCK DIAGRAM



Remark /xxx indicates active low signal.

## BLOCK FUNCTION

## 1. Liquid-crystal drive circuit

This circuit selects and outputs the level for liquid-crystal driving.
One of $\mathrm{V}_{\mathrm{dd}}$, $\mathrm{V}_{\mathrm{Ee}}$, and $\mathrm{V}_{1}$ is selected by the output of the selection control circuit
2. Selection control circuit

This circuit creates the signal which will select the level of the output signal, based on the output of the shift register circuit and the driving level power selection signals L1 and L2
3. Bidirectional shift register circuit

This refers to the 80-bit bidirectional shift register circuit. The DIR signal can be used to switch over the shift direction

The data that has been entered from the /FRM pin is shifted by the low drive signal strobe (STB).
4. Level shifter circuit

This circuit transforms the 5-V signals to the high-voltage signals for liquid-crystal driving.

## PIN FUNCTIONS

| Classification | Pin Name | Input/Output | Pad No. | Function |
| :---: | :---: | :---: | :---: | :---: |
| Power suuply | Vcc1 <br> Vss <br> VD <br> $V_{\text {Ee }}$ <br> $V_{1}$ |  |  | 5 V power for level shifter GND for level shifter Power for logic, liquid-crystal drive level power Power for logic, liquid-crystal drive level power (GND) Liquid-crystal drive level power |
| Liquid-crystal display timing | STB <br> /FRM <br> /DOFF <br> L1 <br> L2 <br> DIR | i |  | Row drive signal strobe <br> Frame signal <br> Display OFF signal <br> Drive level power selection symbol (1st line) <br> Drive level power selection symbol (2nd line) <br> Shift direction selection symbol:when $L$ (DIR $=V_{\text {EE }}$ ), $X_{1} \rightarrow \mathrm{X}_{160}$ when $H$ (DIR = VDD), $\mathrm{X}_{160} \rightarrow \mathrm{X}_{1}$ |
| Liquid-crystal drive output | $\mathrm{X}_{1}$ to $\mathrm{X}_{160}$ | 0 |  | Liquid-crystal drive output Selects and outputs one of $\mathrm{V}_{\mathrm{dD}}, \mathrm{V}_{\mathrm{EE}}$, and $\mathrm{V}_{1}$. |

## DETAILS OF PIN FUNCTIONS

- STB (input)

Input pin of the row drive strobe signal
The bidirectional shift register is shifted at STB's rising edge.

- /FRM (input)

Input pin of the frame signal
The shift register data is read at STB's rising edge.

- DIR (input)

Input pin of the drive output's shift direction selection signal
When the shift direction selection signal (DIR) is "L", the shift data (selection signal) is shifted from the drive output $\mathrm{X}_{1}$ to the $\mathrm{X}_{160}$ direction. When " H ", it is shifted from the $\mathrm{X}_{160}$ to the $\mathrm{X}_{1}$ direction.

- /DOFF' (input)

Input pin of the display OFF signal
It is placed in the display OFF status (all outputs at $\mathrm{V}_{1}$ ) at the " L " level. In the mean time, it reads the frame signal and returns to the normal display status at the "H" level.

- L1 and L2 (input)

Input pins of the drive level power selection signal
In the case of the liquid-crystal drive output, the two lines are selected simultaneously by the shift register. L1 selects the first line, and L2 selects the second line. Both lines select Vdd at "H", and Vee at "L".

## * SYSTEM CONFIGURATION EXAMPLE

This example shows configuration of a liquid-crystal panel of half-VGA size ( $480 \times 320$ oblong) using four column drivers and two row drivers.

- Each column driver sets the LSI No. with PL0 and PL1 pins.
- The DIR pins of each column driver are all set to low level.
- Only one of the column drivers is set to the master, all the others are set to the slave. Signals are supplied from the master column driver to the slave column driver and the row driver.
- Connect an oscillator resistor to the OSC1 and OSC2 pins of the master, and leave the slave open.
- Inputs signals from the system (D0 to D15, A0 to A16, /CS, /OE, /WE, /UBE, RDY, /RESET, /DOFF') in parallel to all of the column driver. Connect a pull-up resistor to the RDY signal.
- The TEST pin is used to test the LSI, and is open or GND when the system is configured.


Remark The /DOUT pin is an output pin for the column driver.

## ^ POWER SUPPLY SEQUENCE OF CHIP SET

It is recommended to apply power in the following sequence.
$\mathrm{VCC}_{2} \rightarrow \mathrm{VCC}_{1} \rightarrow$ input $\rightarrow \mathrm{V}_{\mathrm{DD}}, \mathrm{V}_{\mathrm{EE}} \rightarrow \mathrm{V}_{1}, \mathrm{~V}_{2}$
Be sure to apply LCD drive voltages $\mathrm{V}_{1}$ and $\mathrm{V}_{2}$ last.


Notes 1. $V_{c c 2}, C P U I / F, / R E S E T$, and $V_{2}$ are column driver power supply pins or input pins.
2. Vdd and Vee do not need to be turned ON at the same time.

Caution Turn off the power to the chip set in the reverse order of the power application sequence.

EXAMPLE OF CONNECTING INTERNAL SCHOTTKY BARRIER DIODE OF MODULE TO REINFORCE POWER SUPPLY PROTECTION
(Use a schottky barrier diode with $\mathrm{V}_{\mathrm{f}}=0.5 \mathrm{~V}$ or less.)


Connect the diodes enclosed in the dotted line $\binom{----1}{1-\cdots--1}$ when $\mathrm{V}_{0}$ is not 0 V (GND)

Note $\mathrm{V}_{0}$ and $\mathrm{V}_{2}$ are column driver liquid-crystal power supplies.

## ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, $\mathrm{Vss}=0 \mathrm{~V}$ )

| Parameter | Symbol | Condition | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Supply voltage | Vcc1 |  | -0.5 to +6.5 | V |
|  | $\mathrm{V}_{\mathrm{dd}}$ - $\mathrm{V}_{\text {EE }}$ | $\mathrm{V}_{\text {CC1 }} \leq \mathrm{V}_{\text {dD }}, \mathrm{V}_{\text {EE }} \leq \mathrm{V}_{\text {SS }}$ | 40 |  |
|  | $\mathrm{V}_{1}$ |  | $\mathrm{V}_{\text {EE }}-0.5$ to $\mathrm{VdD}+0.5$ |  |
| Input voltage | $V_{11}$ | Other than the DIR pin | -0.5 to $\mathrm{Vcc} 1+0.5$ |  |
|  | $\mathrm{V}_{12}$ | DIR pin | $\mathrm{V}_{\text {EE }}-0.5$ to $\mathrm{VdD}^{\text {d }}+0.5$ |  |
| Output voltage | Vo |  | $\mathrm{V}_{\text {EE }}-0.5$ to V dD +0.5 |  |
| Operating temperature | TA |  | -20 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | $\mathrm{T}_{\text {stg }}$ |  | -40 to +125 |  |

$\star \quad$ Recommended Operating Range ( $\mathrm{T}_{\mathrm{A}}=-20$ to $+70^{\circ} \mathrm{C}$, $\mathrm{Vss}=0 \mathrm{~V}$ )

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage | Vcc1 |  | 4.75 |  | 5.25 | V |
|  | VDD - $\mathrm{V}_{1}$ |  | 10 |  | 18 |  |
|  | $\mathrm{V}_{1}-\mathrm{V}_{\text {EE }}$ |  | 10 |  | 18 |  |
|  | $\mathrm{V}_{1}$ |  | 0 |  | 3 |  |
| Input voltage | $\mathrm{V}_{11}$ | Other than DIR pin | 0 |  | Vcc1 |  |
|  | $\mathrm{V}_{12}$ | DIR pin | Vee |  | VDD |  |

DC Characteristics (unless otherwise specified, $\mathrm{Vcc}_{\mathrm{Cl}}=4.75$ to 5.25 V , $\mathrm{V}_{\mathrm{dd}}-\left(\mathrm{V}_{\mathrm{Ee}}\right)=20$ to $\mathbf{3 1} \mathrm{V}, \mathrm{V}_{\mathrm{cc} 1} \leq \mathrm{V}_{\mathrm{dd}}, \mathrm{V}_{\mathrm{EE}}$ $\leq \mathrm{V}_{\mathrm{ss}}, \mathrm{V}_{1}=0$ to $3 \mathrm{~V}, \mathrm{~V}_{\mathrm{ss}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-20$ to $+70^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| High-level input voltage | $\mathrm{V}_{1+1}$ | Other than the DIR pin | 0.8 Vcc 1 |  |  | V |
|  | V $\mathrm{H}_{2}$ | DIR pin | $\begin{aligned} & V_{D D}-0.3\left(V_{D D}-\right. \\ & \left.V_{E E}\right) \end{aligned}$ |  |  |  |
| Low-level input voltage | VIL1 | Other than the DIR pin |  |  | $0.2 \mathrm{Vcc1}$ |  |
|  | VIL2 | DIR pin |  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{EE}}+0.3(\mathrm{VDD}- \\ & \left.\mathrm{V}_{\mathrm{EE}}\right) \end{aligned}$ |  |
| Driver ON resistance | Ron | Load current $=100 \mu \mathrm{~A}$ |  | 1.0 | 2.0 | k $\Omega$ |
| Input leakage current | Інн | $\mathrm{V}_{\mathrm{IN}}=\mathrm{Vcc}$, other than the DIR pin |  |  | 1.0 | $\mu \mathrm{A}$ |
|  | lıн2 | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{DD}}$, DIR pin |  |  | 25 |  |
|  | \|L1 | $\mathrm{VIN}=0 \mathrm{~V}$, other than the DIR pin |  |  | -1.0 |  |
|  | lı2 | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {ex }}$, DIR pin |  |  | -25 |  |
| Current consumption | Icc1 | Operating frame frequency at 70 Hz |  | 200 | 320 | $\mu \mathrm{A}$ |
|  | IDD |  |  | 40 | 100 |  |

## AC Characteristics

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| STB high-level width | twsh |  | 500 |  |  | ns |
| STB low-level width | tws |  | 500 |  |  |  |
| /FRM setup time | tst |  | 100 |  |  |  |
| /FRM hold time | thf |  | 100 |  |  |  |
| STB rising time | tr |  |  |  | 150 |  |
| STB falling time | tf |  |  |  | 150 |  |
| Output delay time | $t_{\text {pdsx }}$ | Output no-load |  |  | 300 |  |
|  | tpdout |  |  |  | 200 |  |

AC CHARACTERISTICS WAVEFORM DIAGRAMS


## LEVEL SELECTION TIMING OF LIQUID-CRYSTAL DRIVE OUTPUT

The /FRM is input twice in one frame. The STB is input 81 times in half a frame, and 162 times in one frame.


Remark When /DOFF' is " L ", the X output becomes $\mathrm{V}_{1}$ level. Afterward, if /DOFF' becomes " H ", the level of the $X$ output is output with the above timing.

Caution When the time difference between the STB, L1, and L2 signals is large, hazards may occur in output.


## Detail of cross mark



## TCP tape winding direction



PIN CONFIGURATION

[MEMO]

NEC
[MEMO]

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