NEC

MOS INTEGRATED CIRCUIT

μPD16670

1/17, 1/25, 1/33 DUTY LCD CONTROLLER/DRIVER

DESCRIPTION

The μPD16670 is a LCD controller/driver with 1/17, 1/25 and 1/33 duty capable of displaying a dot matrix LCD. It has 60 segment outputs, 33 common outputs, giving a maximum display capability of 12 columns x 4 lines (at 1/33 duty).

The μPD16670 includes 4 x mode on-chip booster circuit, capable of operating on single 3 V-power supply.

FEATURES

- Dot matrix LCD controller/driver
- Able to operate using +3-V single power supply
- 4 x mode on-chip boost circuit
- Display contents
  1/17 duty: 12 columns x 2 lines + 60 pictograph displays
  1/25 duty: 12 columns x 3 lines + 60 pictograph displays
  1/33 duty: 12 columns x 4 lines + 60 pictograph displays
- Serial data input (SCK, STB, DATA)

ORDERING INFORMATION

Part number	Package
μPD16670W-xxx	Wafer
μPD16670P-xxx	Chip

★ **Remark** Purchasing the above chip/wafer entails exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

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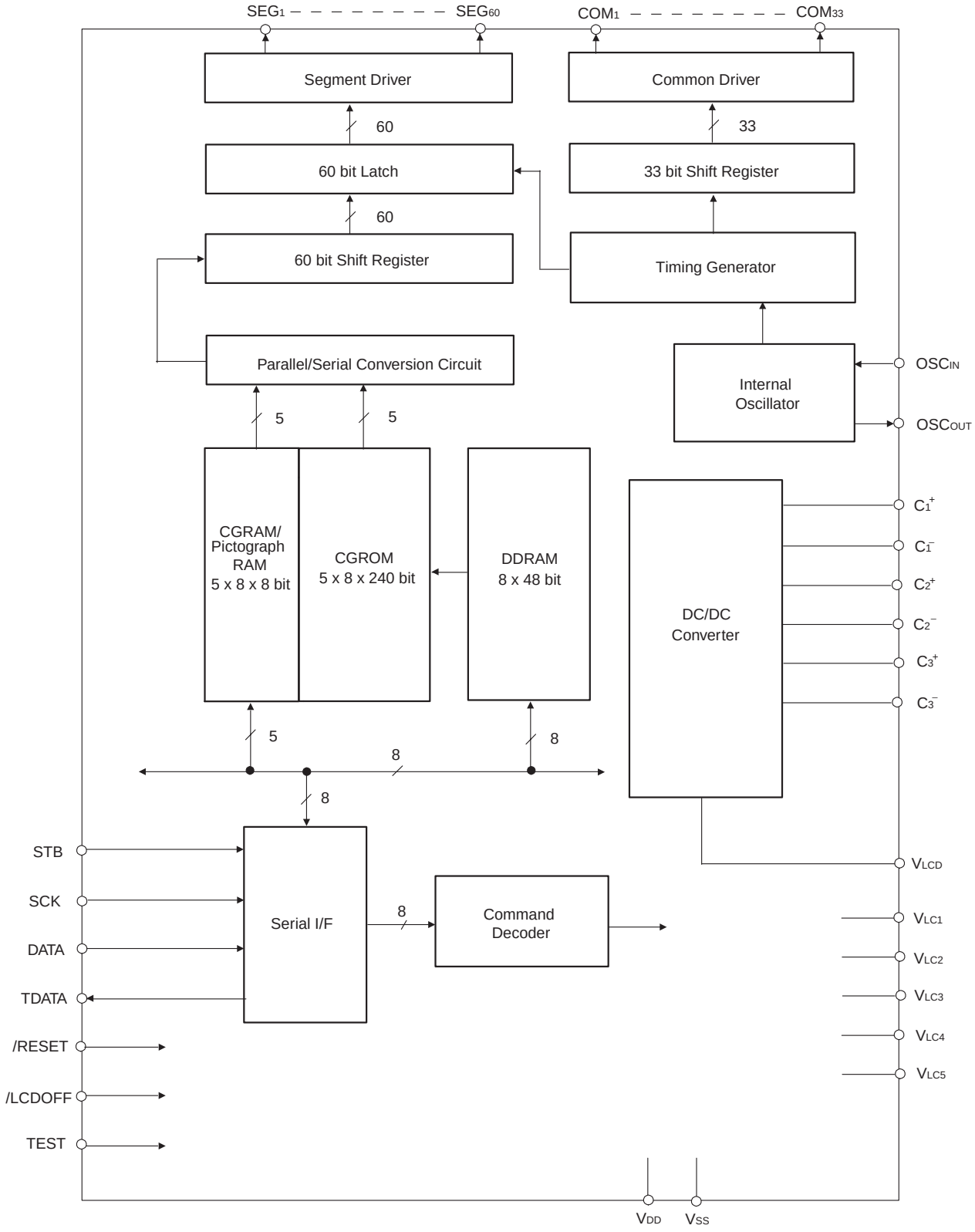
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



★ **Remark** /xxx indicates active low signals.

2. PIN CONFIGURATION (Pad Layout)

Chip size: 4.20 x 5.40 mm^2

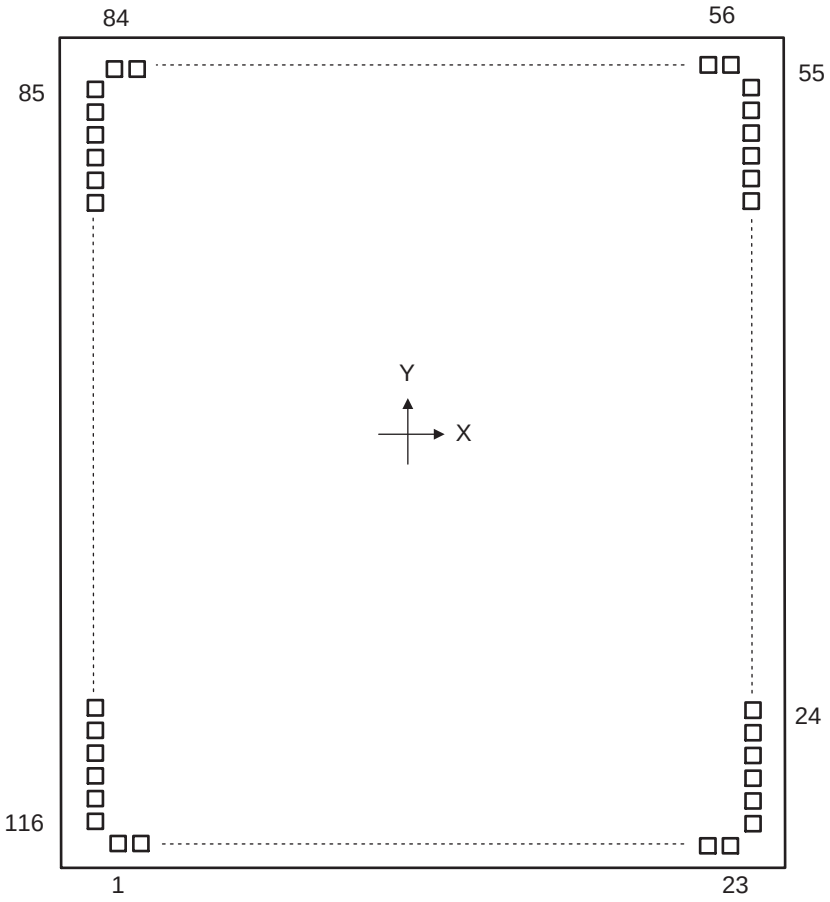


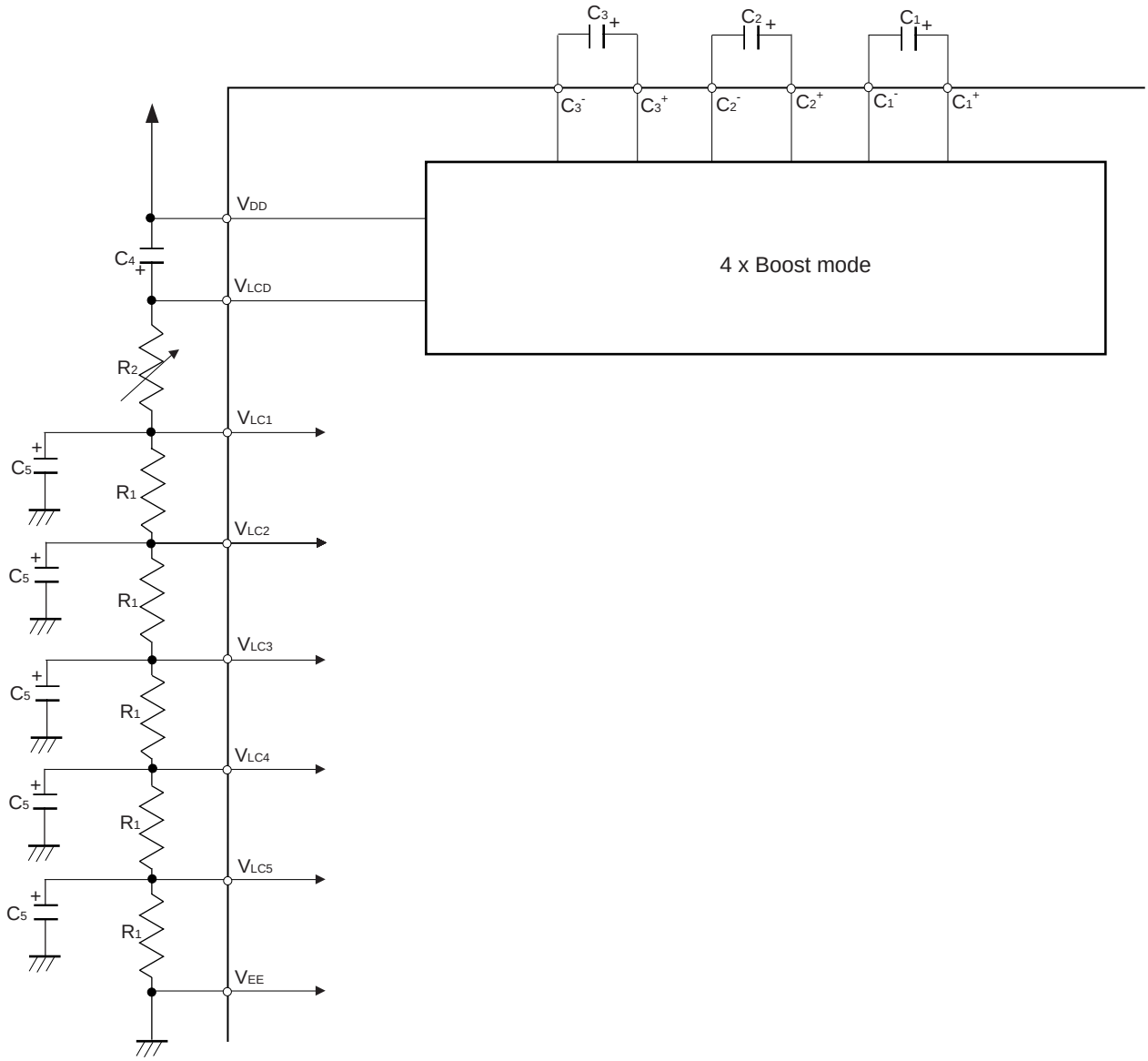
Table 2–1. Pad Layout

PAD No.	Pad Name	X (μm)	Y (μm)
1	C_2^+	–1545	–2480
2	C_2^-	–1425	–2480
3	C_3^+	–1305	–2480
4	C_3^-	–1135	–2480
5	C_1^+	–1015	–2480
6	C_1^-	–845	–2480
7	V_{DD}	–725	–2480
8	V_{LCD}	–605	–2480
9	V_{LC1}	–435	–2480
10	V_{LC2}	–265	–2480
11	V_{LC3}	–95	–2480
12	V_{LC4}	75	–2480
13	V_{LC5}	245	–2480
14	V_{SS}	365	–2480
15	OSC_{IN}	485	–2480
16	OSC_{OUT}	605	–2480
17	TEST	775	–2480
18	TDATA	895	–2480
19	RESETB	1065	–2480
20	LCDOFFB	1185	–2480
21	STB	1355	–2480
22	SCK	1475	–2480
23	DATA	1645	–2480
24	COM_{18}	1837	–1839
25	COM_{19}	1837	–1719
26	COM_{20}	1837	–1599
27	COM_{21}	1837	–1479
28	COM_{22}	1837	–1359
29	COM_{23}	1837	–1239
30	COM_{24}	1837	–1119
31	COM_{25}	1837	–999
32	COM_{26}	1837	–879
33	COM_{27}	1837	–759
34	COM_{28}	1837	–639
35	COM_{29}	1837	–519
36	COM_{30}	1837	–399
37	COM_{31}	1837	–279
38	COM_{32}	1837	–159
39	COM_{33}	1837	–39
40	SEG_{60}	1837	81
41	SEG_{59}	1837	201
42	SEG_{58}	1837	321
43	SEG_{57}	1837	441
44	SEG_{56}	1837	561
45	SEG_{55}	1837	681
46	SEG_{54}	1837	801
47	SEG_{53}	1837	921
48	SEG_{52}	1837	1041
49	SEG_{51}	1837	1161
50	SEG_{50}	1837	1281
51	SEG_{49}	1837	1401
52	SEG_{48}	1837	1521
53	SEG_{47}	1837	1641
54	SEG_{46}	1837	1761
55	SEG_{45}	1837	1881
56	SEG_{44}	1679	2479
57	SEG_{43}	1559	2479
58	SEG_{42}	1439	2479
59	SEG_{41}	1319	2479
60	SEG_{40}	1199	2479
61	SEG_{39}	1079	2479
62	SEG_{38}	959	2479
63	SEG_{37}	839	2479
64	SEG_{36}	719	2479
65	SEG_{35}	599	2479
66	SEG_{34}	479	2479
67	SEG_{33}	359	2479
68	SEG_{32}	239	2479
69	SEG_{31}	119	2479
70	SEG_{30}	–1	2479
71	SEG_{29}	–121	2479
72	SEG_{28}	–241	2479
73	SEG_{27}	–361	2479
74	SEG_{26}	–481	2479
75	SEG_{25}	–601	2479
76	SEG_{24}	–721	2479
77	SEG_{23}	–841	2479
78	SEG_{22}	–961	2479
79	SEG_{21}	–1081	2479
80	SEG_{20}	–1201	2479
81	SEG_{19}	–1321	2479
82	SEG_{18}	–1441	2479
83	SEG_{17}	–1561	2479
84	SEG_{16}	–1681	2479
85	SEG_{15}	–1837	1880
86	SEG_{14}	–1837	1760
87	SEG_{13}	–1837	1640
88	SEG_{12}	–1837	1520
89	SEG_{11}	–1837	1400
90	SEG_{10}	–1837	1280
91	SEG_9	–1837	1160
92	SEG_8	–1837	1040
93	SEG_7	–1837	920
94	SEG_6	–1837	800
95	SEG_5	–1837	680
96	SEG_4	–1837	560
97	SEG_3	–1837	440
98	SEG_2	–1837	320
99	SEG_1	–1837	200
100	COM_{17}	–1837	80
101	COM_{16}	–1837	–40
102	COM_{15}	–1837	–160
103	COM_{14}	–1837	–280
104	COM_{13}	–1837	–400
105	COM_{12}	–1837	–520
106	COM_{11}	–1837	–640
107	COM_{10}	–1837	–760
108	COM_9	–1837	–880
109	COM_8	–1837	–1000
110	COM_7	–1837	–1120
111	COM_6	–1837	–1240
112	COM_5	–1837	–1360
113	COM_4	–1837	–1480
114	COM_3	–1837	–1600
115	COM_2	–1837	–1720
116	COM_1	–1837	–1840

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Pad No.	I/O	Description
SEG_1 to SEG_{60}	Segment	40 to 99	O	Segment output pins
★ COM_1 to COM_{33}	Common	24 to39 100 to116	O	Common output pins COM_1 is assigned to common for pictograph.
SCK	Shift clock	22	I	Data shift clock During the read-in operation, data is captured in the shift register at the signal's rising edge. During a read-out operation, data is read from the shift register at the signal's falling edge.
DATA	Data	23	I	Performs input of commands and data. Input is performed from the MSB on the rise of the shift clock.
STB	Strobe	21	I	Communication is enabled when STB is low.
/LCDOFF	LCD off input	20	I	When at low level, a forced LCD off operation is performed SEGn = COMn = V_{SS}
/RESET	Reset	19	I	This pin is used for internal resets at low level.
TDATA	Test output	18	O	This is a test output pin. Leave this pin open when using the device.
TEST	Test pin	17	I	Test mode is set when at high level.
OSC_{IN}	Oscillator pins	15, 16	I	These pins are connected to a 100-kΩ resistance. When using an external oscillator, input to OSC_{IN} and leave OSC_{OUT} open.
OSC_{OUT}		5, 6	O	
C_1^+, C_1^- C_2^+, C_2^- C_3^+, C_3^-	Capacitor connection pins	1 to 6	–	These are capacitor connection pins for the boost circuit. Connect a 1-μF capacitor.
V_{DD}	Logic power supply pin	7	–	Power supply pins for logic
V_{SS}	Logic ground pin	14	–	Ground pin for logic
V_{LCD}	Driver power supply pins	8	–	Power supply pin for driver. Output pin for internal boost circuit. Connect a 1-μF capacitor between this pin and the V_{SS} pin for boosting. If not using the internal boost circuit, a direct driver power supply can be input.
V_{LC1} - V_{LC5}	Reference power supply pins for driver	9 to 13	–	These are reference power supply pins for the LCD driver. Input divided register by each external power supply pin.

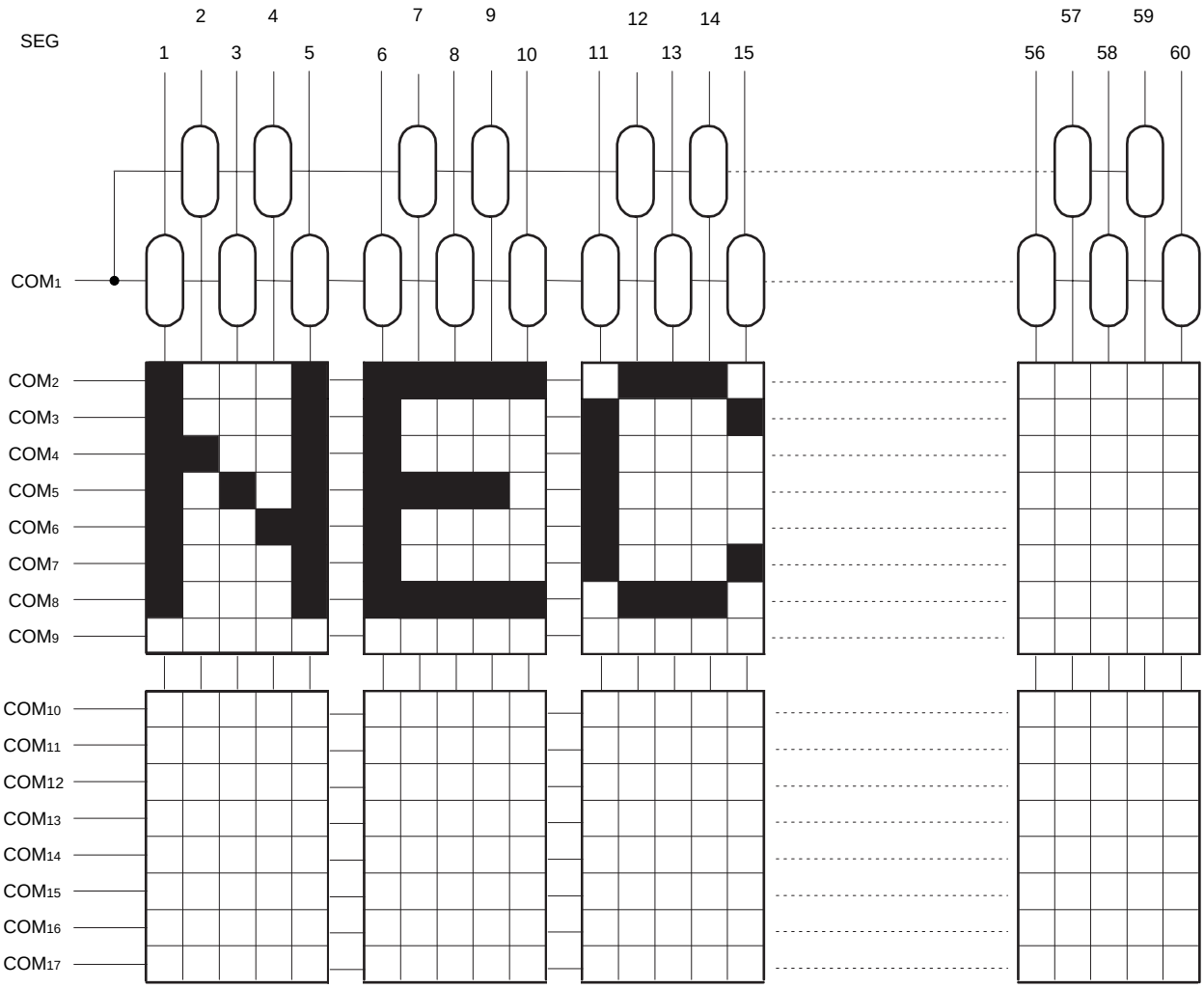
Figure 3–1. Example of LCD driver's circuit and external circuit for boosted circuit



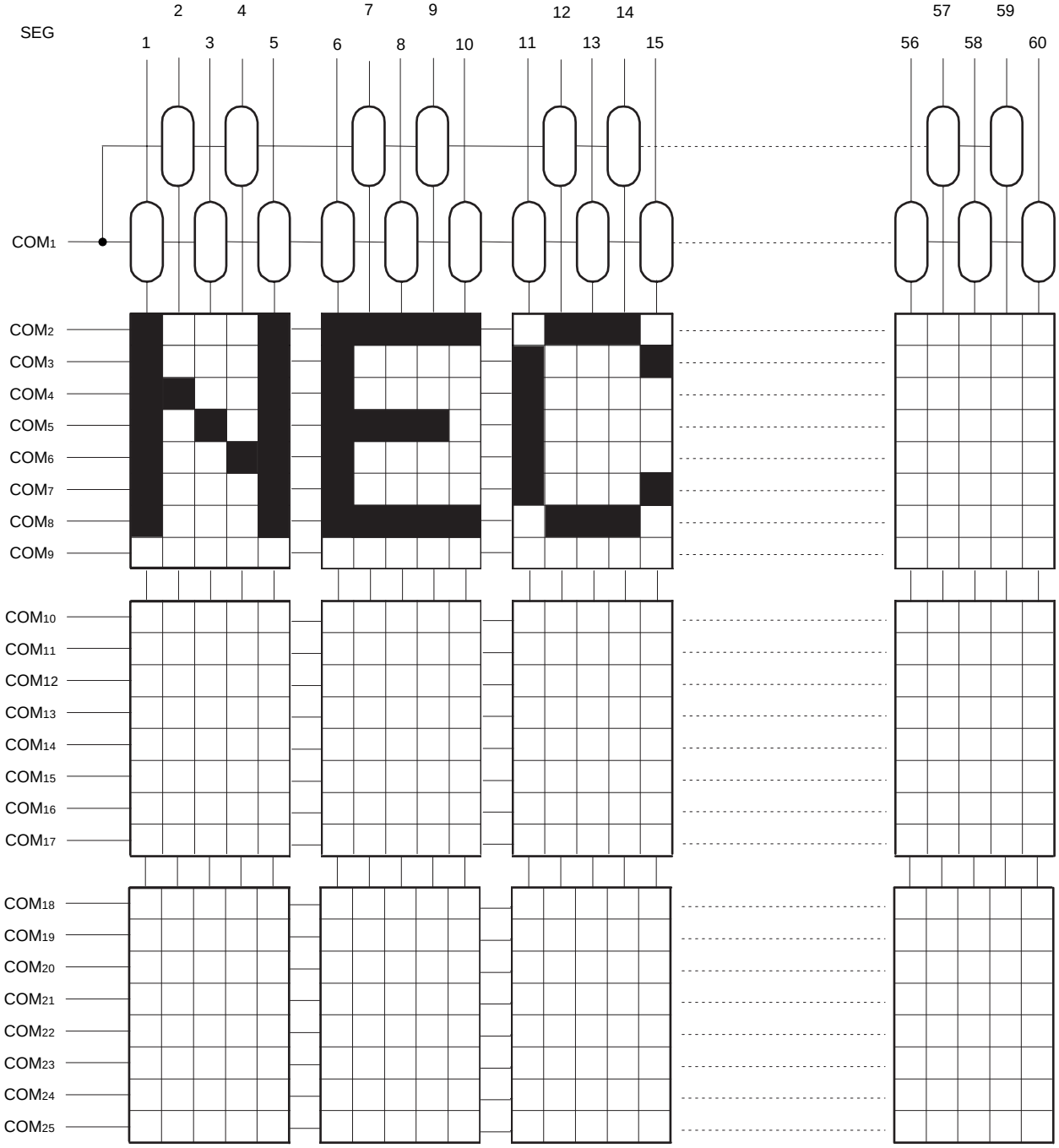
4. LCD DISPLAY DRIVER

μPD16670, a 5 x 8 segment display and pictograph display segments can be driven.

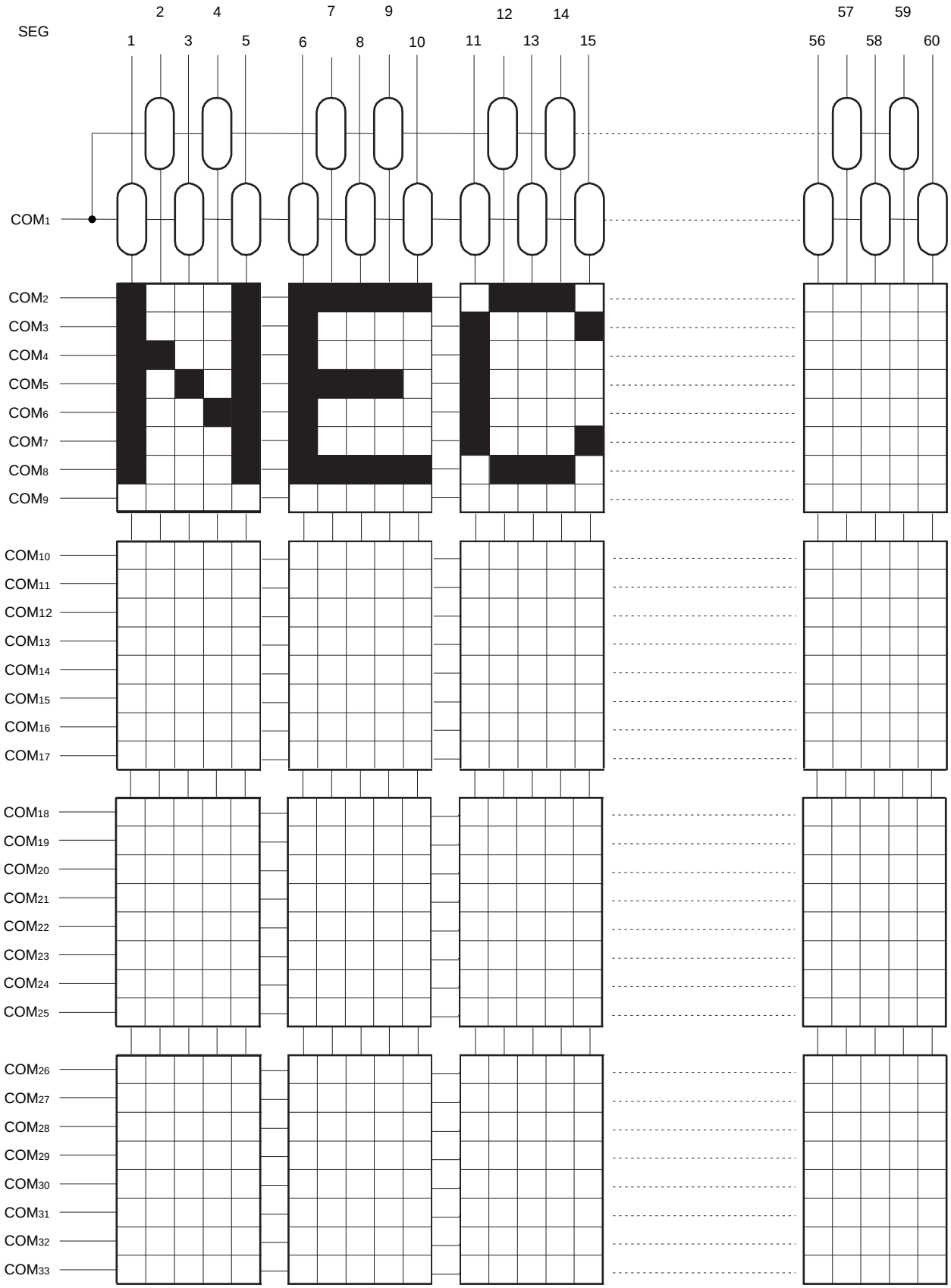
(1) Example of 1/17 duty connection: 12 columns x 2 lines + 60 pictograph displays



(2) Example of 1/25 duty connection: 12 columns x 3 lines + 60 pictograph displays



(3) Example of 1/33 duty connection: 12 columns x 4 lines + 60 pictograph displays



5. CHARACTER CODE

The relation between character codes and character patterns is shown below. Character codes [0xxx] are allocated to CGRAM.

Higher bits / Lower bits 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)													
XXXX0001	(2)													
XXXX0010	(3)													
XXXX0011	(4)													
XXXX0100	(5)													
XXXX0101	(6)													
XXXX0110	(7)													
XXXX0111	(8)													
XXXX1000	(1)													
XXXX1001	(2)													
XXXX1010	(3)													
XXXX1011	(4)													
XXXX1100	(5)													
XXXX1101	(6)													
XXXX1110	(7)													
XXXX1111	(8)													

6. DESCRIPTION OF BLOCKS

6.1 Display Data RAM (DDRAM)

DDRAM addresses are allocated as shown below

	1	2	3	4	5	6	7	8	9	10	11	12
1st line	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH
2nd line	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH
3rd line	24H	25H	26H	27H	28H	29H	2AH	2BH	2CH	2DH	2EH	2FH
4th line	36H	37H	38H	39H	3AH	3BH	3CH	3DH	3EH	3FH	40H	41H

Caution DDRAM are used 0BH → 10H, 1BH → 20H, 2BH → 30H, 3BH → 00H when in auto increment mode.

6.2 Character Generator RAM (CGRAM)

CGRAM is RAM to which the user can freely set character patterns. Eight types of 5 x 8 dot character patterns can be defined. CGRAM is the RAM that contains pictograph display data.

The relation between character codes and CGRAM addresses used to access CGRAM is shown below.

CGRAM address	D4	D3	D2	D1	D0	CGROM address
00H						00H
01H						
02H						
03H						
04H						
05H						
06H						
07H						
08H						00H
09H						
0AH						
0BH						
0CH						
0DH						
0EH						
0FH						
10H						01H
11H						
12H						
13H						
14H						
15H						
16H						
17H						
18H						02H
19H						
1AH						
1BH						
1CH						
1DH						
1EH						
1FH						

CGRAM address	D4	D3	D2	D1	D0	CGROM address
20H						04H
21H						
22H						
23H						
24H						
25H						
26H						
27H						
28H						05H
29H						
2AH						
2BH						
2CH						
2DH						
2EH						
2FH						
30H						06H
31H						
32H						
33H						
34H						
35H						
36H						
37H						
38H						07H
39H						
3AH						
3BH						
3CH						
3DH						
3EH						
3FH						

Caution Some addresses in 06H and all 07H address in CGROM are shared with pictograph data RAM.

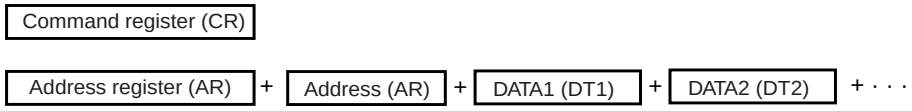
6.2.1 Pictograph Display RAM (PDRAM)

Pictograph display RAM addresses used to some parts of CGRAM is shown below.

CGRAM address	D5	D4	D3	D2	D1	CGROM address
30H	45	44	43	42	41	06H
31H	50	49	48	47	46	
32H	55	54	53	52	51	
33H	60	59	58	57	56	
34H						
35H						
36H						
37H						
38H	5	4	3	2	1	07H
39H	10	9	8	7	6	
3AH	15	14	13	12	11	
3BH	20	19	18	17	16	
3CH	25	24	23	22	21	
3DH	30	29	28	27	26	
3EH	35	34	33	32	31	
3FH	40	39	38	37	36	

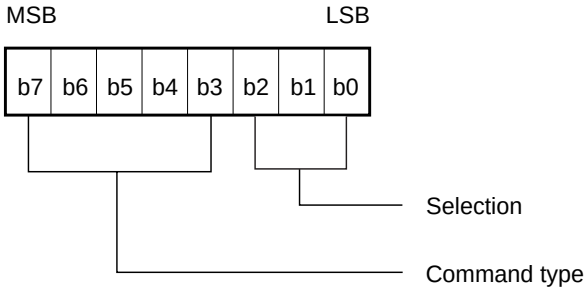
7. COMMANDS

7.1 Basic format



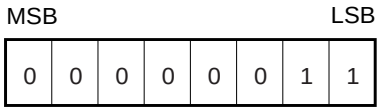
7.2 Command register

The command register's basic configuration is as follows.



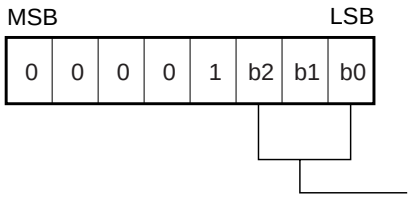
7.2.1 Reset

This command resets all of the commands in the μPD16670.



7.2.2 Display ON/OFF

This command controls the display's ON/OFF status.



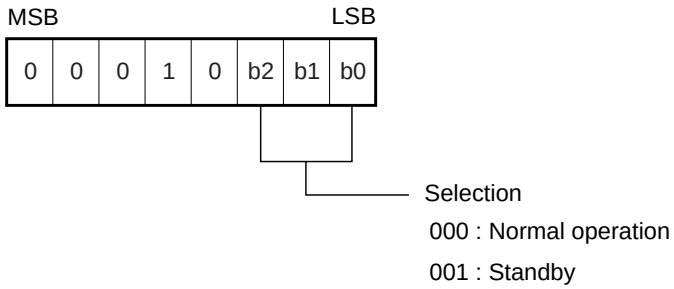
Selection

000 : LCD OFF (SEG_n = non-select waveform)

111 : LCD ON (Normal operation)

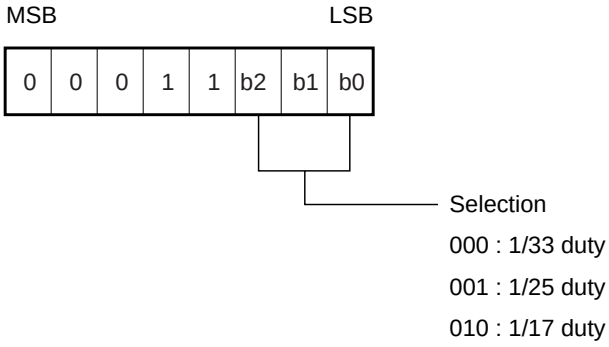
7.2.3 Standby

This command stops the DC/DC converter, which reduces the supply current. The display is set to OFF mode (SEG_n, $COM_n = V_{LC5}$).



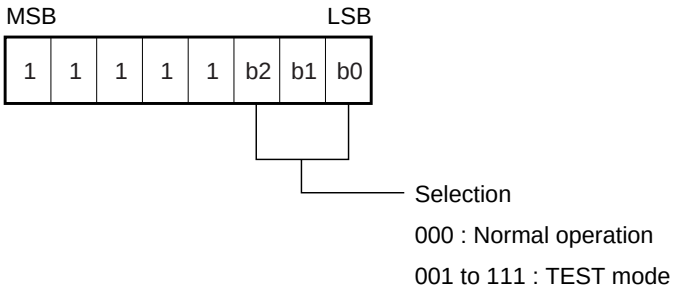
7.2.4 Duty setting

This command specifies the duty setting.



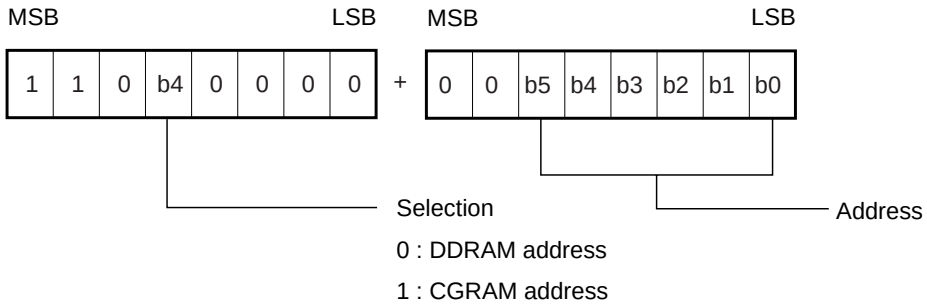
7.2.5 Test mode

This command sets the test mode. The test mode is only for confirming the IC's operation. Regular or continuous use while in test mode is not guaranteed.



7.3 Address Register

This command selects the address type and specifies addresses.



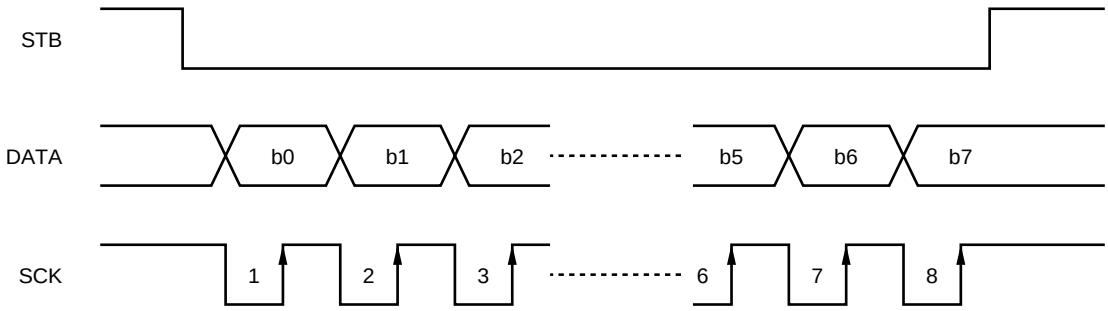
Caution Operation is not guaranteed if an invalid address is set.

★ 7.4 Reset

The contents of the various registers appear as shown below after a reset (command reset or hardware [pin] reset).

Command	Register Contents								Description
	b7	b6	b5	b4	b3	b2	b1	b0	
Display ON/OFF	0	0	0	0	1	0	0	0	LCD OFF
Standby	0	0	0	1	0	0	0	0	Normal operation
Duty setting	0	0	0	1	1	0	1	0	1/33 duty
Test mode	1	1	1	1	1	0	0	0	Normal operation

7.5 Serial communication format



8. CPU ACCESS EXAMPLES

Examples of access procedure are shown below.

8.1 Initialize and Data Write

Parameter	STB	Command/data								Description
		b7	B6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Reset	L	0	0	0	0	0	1	1	1	All commands initialized
	H	X	X	X	X	X	X	X	X	
Duty setting	L	0	0	0	1	1	0	0	1	12 columns by 3 rows + 60 pictographs (1/25 duty)
	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	1	0	0	0	0	CGRAM
Address register 2	L	0	0	0	0	0	0	0	0	CGRAM address = 00H
Data 1	L	X	X	X	D4	D3	D2	D1	D0	
to	:	:	:	:	:	:	:	:	:	CGRAM data
CGRAM data48	L	X	X	X	D4	D3	D2	D1	D0	
	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	1	0	0	0	0	Pictograph data RAM
Address register 2	L	0	0	1	1	0	0	0	0	Pictograph data RAM address = 30H
Pictograph data 1	L	X	X	D5	D4	D3	D2	D1	X	
to	:	:	:	:	:	:	:	:	:	Pictograph data
Pictograph data 4	L	X	X	D5	D4	D3	D2	D1	X	
	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	1	0	0	0	0	Pictograph data RAM
Address register 2	L	0	0	1	1	0	0	0	0	Pictograph data RAM address = 38H
Pictograph data 5	L	X	X	X	D4	D3	D2	D1	D0	
to	:	:	:	:	:	:	:	:	:	Pictograph data
Pictograph data 12	L	X	X	X	D4	D3	D2	D1	D0	
	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	1	0	0	0	0	Display data RAM
Address register 2	L	0	0	0	0	0	0	0	0	Display data RAM address = 00H
Character data 1	L	D	D	D	D	D	D	D	D	
to	:	:	:	:	:	:	:	:	:	Display data
Character data 36	L	D	D	D	D	D	D	D	D	
	H	X	X	X	X	X	X	X	X	
Display ON/OFF	L	0	0	0	0	1	1	1	1	LCD ON (at the STB rising edge)
End	H	X	X	X	X	X	X	X	X	

★ **Remark** X = Don't care, D = Data

8.2 Initialize and Data Write (unused pictograph)

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Reset	L	0	0	0	0	0	1	1	1	All commands initialized
	H	X	X	X	X	X	X	X	X	
Duty setting	L	0	0	0	1	1	0	0	1	12 columns by 3 rows + 60 pictographs (1/25 duty)
	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	1	0	0	0	0	CGRAM
Address register 2	L	0	0	0	0	0	0	0	0	CGRAM address = 00H
CGRAM data1	L	X	X	X	D4	D3	D2	D1	D0	
to	:	:	:	:	:	:	:	:	:	CGRAM data
CGRAM data 64	L	X	X	X	D4	D3	D2	D1	D0	
	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	0	0	0	0	0	Display data RAM
Address register 2	L	0	0	0	0	0	0	0	0	Display data RAM address = 00H
Character data 1	L	D	D	D	D	D	D	D	D	
to	:	:	:	:	:	:	:	:	:	Display data
Character data 36	L	D	D	D	D	D	D	D	D	
	H	X	X	X	X	X	X	X	X	
Display ON/OFF	L	0	0	0	0	1	1	1	1	LCD ON (at the STB rising edge)
End	H	X	X	X	X	X	X	X	X	

★ **Remark** X = Don't care, D = Data

8.3 Change display data

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Address register 1	L	1	1	0	0	0	0	0	0	Display data RAM
Address register 2	L	0	0	0	1	0	0	0	1	Display RAM address = 11H (2 lines 2 clumns)
Character data 1	L	0	0	1	0	0	0	0	0	Display RAM address = 11H, Data write: character code (20H: space)
Character data 2	L	0	1	0	0	1	1	1	0	Display RAM address = 12H, Data write: character code (4EH: ”N”)
Character data 3	L	0	1	0	0	0	1	0	1	Display RAM address = 13H, Data write: character code (45H: ”E”)
Character data 4	L	0	1	0	0	0	0	1	1	Display RAM address = 14H, Data write: character code (43H: ”C”)
Character data 5	L	0	0	1	0	0	0	0	0	Display RAM address = 15H, Data write: character code (20H: space)
End	H	X	X	X	X	X	X	X	X	

★ **Remark** X = Don't Care

8.4 Standby mode

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Standby	L	0	0	0	1	0	0	0	1	Standby
	H	X	X	X	X	X	X	X	X	
Standby off	L	0	0	0	1	0	0	0	0	Normal operation [Note]
End	H	X	X	X	X	X	X	X	X	

Note When in standby mode, DC/DC converter is stop.

If the display operation mode is set before entering the standby mode, it may not be normally working until DC/DC converter, which set after cleaning the standby mode.

★ **Remark** X = Don't Care

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic power supply voltage	V_{DD}	–0.3 to +7.0	V
Logic input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Driver supply voltage	V_{LCD}	–0.3 to +16.0	V
Driver reference supply input voltage	V_{LC1}-V_{LC5}	–0.3 to V_{LCD}+0.3	V
Logic system output voltage (SEG_n, COM_n)	V_{OUT}	–0.3 to V_{DD}+0.3	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

★ **Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Recommended Operating Range (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic power supply voltage	V_{DD}	2.7	3.0	3.6	V
Logic system input voltage	V_{IN}	0		V_{DD}	V
Driver supply voltage	V_{LCD}	2.7		14.4	V
Logic system input voltage	V_{LC1}-V_{LC5}	0		V_{LCD}	V
Output capacitance	C_1-C_3	0.05	0.1	1.0	μF
	C_4	0.05	0.1	1.0	μF
Oscillation frequency	f_{OSC}	245	350	455	kHz

Electrical characteristics (Unless otherwise specified, T_A = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage 1	V_{IH1}	SCK,STB,DATA,/RESET,/LCDOFF	0.8 V_{DD}		V_{DD}	V
Low-level input voltage 1	V_{IL1}	SCK,STB,DATA,/RESET,/LCDOFF	0		0.2 V_{DD}	V
High-level input voltage 2	V_{IH2}	TEST,OSC_{IN}	0.7 V_{DD}		V_{DD}	V
Low-level input voltage 2	V_{IL2}	TEST,OSC_{IN}	0		0.3 V_{DD}	V
High-level input current	I_{IH}	SCK,STB,DATA,/RESET,/LCDOFF, OSC_{IN}			1	μA
		TEST	3	15	75	μA
Low-level input current	I_{IL}	SCK,STB,DATA,TEST,OSC_{IN}			– 1	μA
		/RESET,/LCDOFF	–3	– 15	– 75	μA
High-level output voltage	V_{OH}	TDATA,I_{OH} = –100 μA	0.8 V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL}	TDATA,I_{OL} = 100 μA	V_{SS}		0.2 V_{DD}	V
Common output ON resistance	R_{COM}	COM_1 to COM_{33}, IIoI = 50 μA			15	kΩ
Segment output ON resistance	R_{SEG}	SEG_1 to SEG_{60} , IIoI = 50 μA			30	kΩ
Current consumption (Normal mode)	I_{DD1}	V_{DD} = 3 V, f_{OSC} = 350 kHz, 4-fold voltage mode, no load		200	300	μA
Current consumption (Standby mode)	I_{DD2}	V_{DD} = 3 V, no load			100	μA
Driver voltage (boost voltage)	V_{LCD}	No load	3.5 V_{DD}		4.0 V_{DD}	V

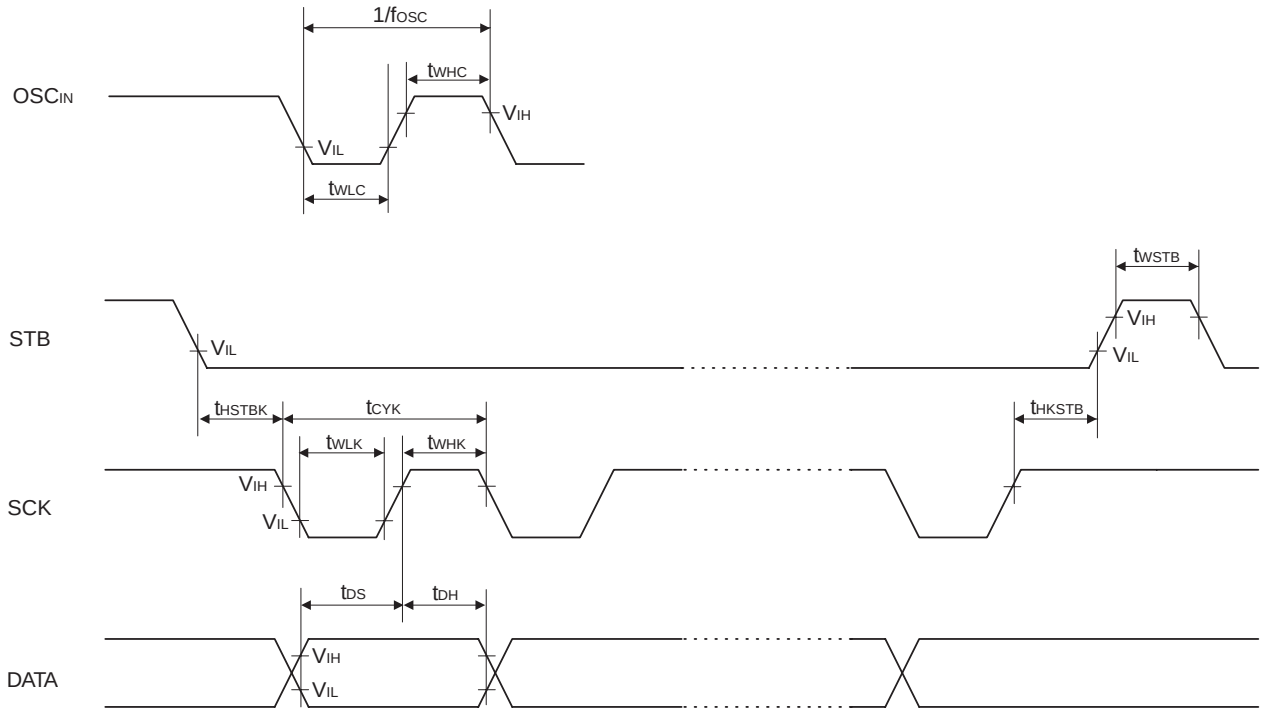
Switching characteristics (Unless otherwise specified, T_A = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	Self-oscillation, V_{DD} = 3 V ± 10 %, R = 100 kΩ	245	350	455	kHz

Required timing conditions (Unless otherwise specified, T_A = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Clock frequency	f_{OSC}	OSC_{IN} external clock	245	350	455	kHz
	High-level clock pulse width	t_{WHC}	OSC_{IN} external clock	0.4 f_{OSC}		0.6 f_{OSC}	–
	Low-level clock pulse width	t_{WLC}	OSC_{IN} external clock	0.4 f_{OSC}		0.6 f_{OSC}	–
	Shift clock cycle	t_{CYK}	SCK	1.2			ns
	High-level shift clock pulse width	t_{WHK}	SCK	350			ns
	Low-level shift clock pulse width	t_{WLK}	SCK	350			ns
	Shift clock hold time	t_{HSTBK}	STB ↓ → SCK ↓	350			ns
★	Data setup time	t_{DS}	DATA ↑↓ → SCK ↑	100			ns
★	Data hold time	t_{DH}	SCK ↑ → DATA ↑↓	450			ns
	STB hold time	t_{HKSTB}	SCK ↑ → STB ↑	350			ns
	STB pulse width	t_{WSTB}		350			ns

Switching characteristic waveform



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

★ **Reference Documents**

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Semiconductor Device Mounting Technology (C10535E)