NEC

MOS INTEGRATED CIRCUIT

μPD16676

1/16, 1/32 DUTY LCD CONTROLLER/DRIVER WITH RAM

DESCRIPTION

μPD16676 is a controller/driver containing RAMs capable of full-dot LCD displays. One of these IC chips can drive the full-dot LCD up to 61-by-16 dots.

These ICs are the most suitable for Kanji character or Chinese character pagers, as well as graphic pagers, displaying 16-by-16 dots per character.

FEATURES

- LCD driver with built-in display RAM
- Dot display RAM: 2560 bits
- Output: 61 segments & 16 commons
- 8-bit parallel interface
- Oscillation circuit incorporated

★ ORDERING INFORMATION

Part Number	Package
μPD16676P	Chips
μPD16676W	Wafer

Remark Purchasing the above products in terms of chips per wafer requires an exchange of other documents as well, including a memorandum of the product quality. Therefore, those who are interested in this regard are advised to contact one of our sales representatives for further details.

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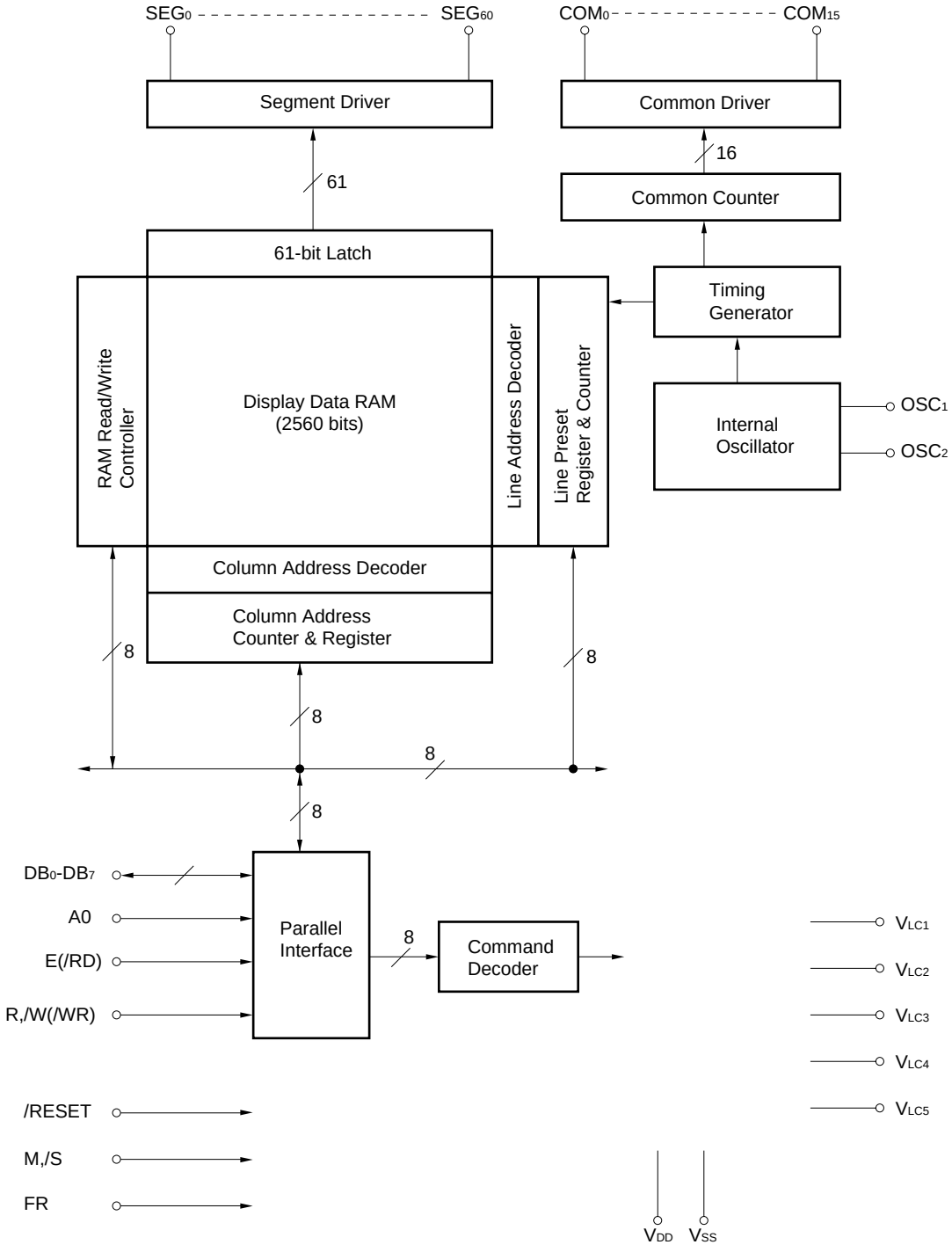
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signals.

★ 2. PIN CONFIGURATION (PAD LAYOUT)

Chip Size : 4.04 x 5.53 mm^2
Pad Size Al Area : 120 x 120 μm^2
Pad Size Open Area : 108 x 108 μm^2

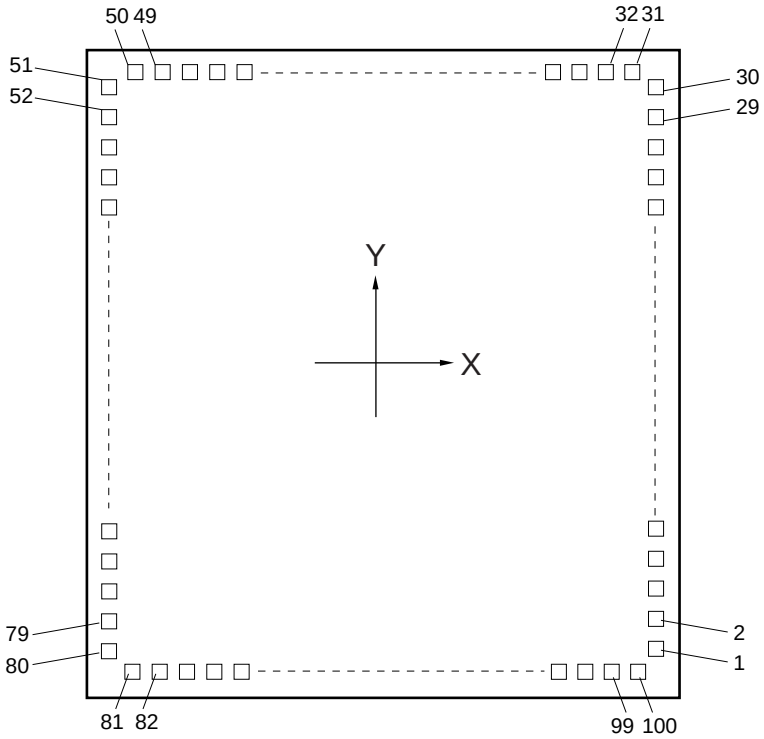


Table2–1. Pad Connection

Pin No.	Pin Symbol	I/O
1	COM_5	Output
2	COM_6	Output
3	COM_7	Output
4	COM_8	Output
5	COM_9	Output
6	COM_{10}	Output
7	COM_{11}	Output
8	COM_{12}	Output
9	COM_{13}	Output
10	COM_{14}	Output
11	COM_{15}	Output
12	SEG_{60}	Output
13	SEG_{59}	Output
14	SEG_{58}	Output
15	SEG_{57}	Output
16	SEG_{56}	Output
17	SEG_{55}	Output
18	SEG_{54}	Output
19	SEG_{53}	Output
20	SEG_{52}	Output
21	SEG_{51}	Output
22	SEG_{50}	Output
23	SEG_{49}	Output
24	SEG_{48}	Output
25	SEG_{47}	Output
26	SEG_{46}	Output
27	SEG_{45}	Output
28	SEG_{44}	Output
29	SEG_{43}	Output
30	SEG_{42}	Output
31	SEG_{41}	Output
32	SEG_{40}	Output
33	SEG_{39}	Output
34	SEG_{38}	Output
35	SEG_{37}	Output
36	SEG_{36}	Output
37	SEG_{35}	Output
38	SEG_{34}	Output
39	SEG_{33}	Output
40	SEG_{32}	Output
41	SEG_{31}	Output
42	SEG_{30}	Output
43	SEG_{29}	Output
44	SEG_{28}	Output
45	SEG_{27}	Output
46	SEG_{26}	Output
47	SEG_{25}	Output
48	SEG_{24}	Output
49	SEG_{23}	Output
50	SEG_{22}	Output

Pin No.	Pin Symbol	I/O
51	SEG_{21}	Output
52	SEG_{20}	Output
53	SEG_{19}	Output
54	SEG_{18}	Output
55	SEG_{17}	Output
56	SEG_{16}	Output
57	SEG_{15}	Output
58	SEG_{14}	Output
59	SEG_{13}	Output
60	SEG_{12}	Output
61	SEG_{11}	Output
62	SEG_{10}	Output
63	SEG_9	Output
64	SEG_8	Output
65	SEG_7	Output
66	SEG_6	Output
67	SEG_5	Output
68	SEG_4	Output
69	SEG_3	Output
70	SEG_2	Output
71	SEG_1	Output
72	SEG_0	Output
73	A0	Input
74	OSC_1	Input
75	OSC_2	Output
76	E(/RD)	Input
77	R,/W(/WR)	Input
78	V_{SS}	—
79	DB_0	Input/Output
80	DB_1	Input/Output
81	DB_2	Input/Output
82	DB_3	Input/Output
83	DB_4	Input/Output
84	DB_5	Input/Output
85	DB_6	Input/Output
86	DB_7	Input/Output
87	V_{DD}	—
88	/RESET	Input
89	FR	Input/Output
90	V_{LC5}	—
91	V_{LC3}	—
92	V_{LC2}	—
93	M,/S	Input
94	V_{LC4}	—
95	V_{LC1}	—
96	COM_0	Output
97	COM_1	Output
98	COM_2	Output
99	COM_3	Output
100	COM_4	Output

Table2–2. Pad Layout

Pin No.	X (μm)	Y (μm)	Pin No.	X (μm)	Y (μm)	Pin No.	X (μm)	Y (μm)
1	1771	–2230	36	668.8	2517.2	71	–1771	–757.2
2	1771	–2076	37	518.8	2517.2	72	–1771	–907.2
3	1771	–1922	38	368.8	2517.2	73	–1767.8	–1149.4
4	1771	–1768	39	218.8	2517.2	74	–1767.8	–1299.4
5	1771	–1614	40	68.8	2517.2	75	–1767.8	–1489.4
6	1771	–1460	41	–81.2	2517.2	76	–1767.8	–1639.4
7	1771	–1306	42	–231.2	2517.2	77	–1767.8	–1839.4
8	1771	–1152	43	–381.2	2517.2	78	–1767.8	–1989.4
9	1771	–998	44	–531.2	2517.2	79	–1767.8	–2139.4
10	1771	–844	45	–681.2	2517.2	80	–1767.8	–2289.4
11	1771	–690	46	–831.2	2517.2	81	–1745	–2513.4
12	1771	–536	47	–981.2	2517.2	82	–1595	–2513.4
13	1771	–382	48	–1131.2	2517.2	83	–1395	–2513.4
14	1771	–228	49	–1281.2	2517.2	84	–1245	–2513.4
15	1771	–74	50	–1431.2	2517.2	85	–1045	–2513.4
16	1771	80	51	–1771	2242.8	86	–895	–2513.4
17	1771	234	52	–1771	2092.8	87	–682.6	–2513.4
18	1771	388	53	–1771	1942.8	88	–532.2	–2513.4
19	1771	542	54	–1771	1792.8	89	–382.2	–2513.4
20	1771	696	55	–1771	1642.8	90	–106.6	–2513.4
21	1771	850	56	–1771	1492.8	91	69.8	–2513.4
22	1771	1004	57	–1771	1342.8	92	219.8	–2513.4
23	1771	1158	58	–1771	1192.8	93	369.8	–2513.4
24	1771	1312	59	–1771	1042.8	94	569.8	–2513.4
25	1771	1466	60	–1771	892.8	95	719.8	–2513.4
26	1771	1620	61	–1771	742.8	96	952.4	–2513.4
27	1771	1774	62	–1771	592.8	97	1102.4	–2513.4
28	1771	1928	63	–1771	442.8	98	1252.4	–2513.4
29	1771	2082	64	–1771	292.8	99	1402.4	–2513.4
30	1771	2236	65	–1771	142.8	100	1552.4	–2513.4
31	1418.8	2517.2	66	–1771	–7.2			
32	1268.8	2517.2	67	–1771	–157.2			
33	1118.8	2517.2	68	–1771	–307.2			
34	968.8	2517.2	69	–1771	–457.2			
35	818.8	2517.2	70	–1771	–607.2			

5. PIN FUNCTIONS

5.1 Power System

Pin Symbol	Pin Name	Pin No.	I/O	Description
V_{DD}	Power supply pin	87	—	Power supply
V_{SS}	Ground	78	—	Ground
V_{LC1} to V_{LC5}	Reference power supply for drivers	90,91,92,94, 95	—	Reference power supply for LCD driving

5.2 Logic system

Pin Symbol	Pin Name	Pin No.	I/O	Description
M,/S	Master/Slave selection	93	Input	Switches between the master chip and the slave chip.
FR	LCD to AC signal	89	Input/ Output	Exchanges synchronizing signals (LCD-to-AC signals) in connecting cascades. This pin is for output if the chip is the master, and for input if the chip is the slave.
DB_0 to DB_7	Data Bus	79 to 86	Input/ Output	Data inputs/outputs
A0	Data/Instruction Switching	73	Input	This pin is used for switching between the display data and the instruction. High level : Display data Low level : Instruction
/RESET	Reset and 68/80-series switching	88	Input	This pin performs reset at the edge of the low-level pulse. At that level, it performs switching 68/80 series modes. High level : 68 series CPU interface Low level : 80 series CPU interface
E(/RD)	Enable and read enable	76	Input	68 series mode : Enable signal 80 series mode : Read enable signal
R,/W(/WR)	Read/Write and Write enable	77	Input	68 series mode : Read/Write signal 80 series mode : Write enable signal
OSC_1	Oscillation pin	74	Input	Oscillation (connected with a register between OSC_2)
OSC_2	Oscillation pin	75	Output	Oscillation (connected with a register between OSC_1)

5.3 Driver System

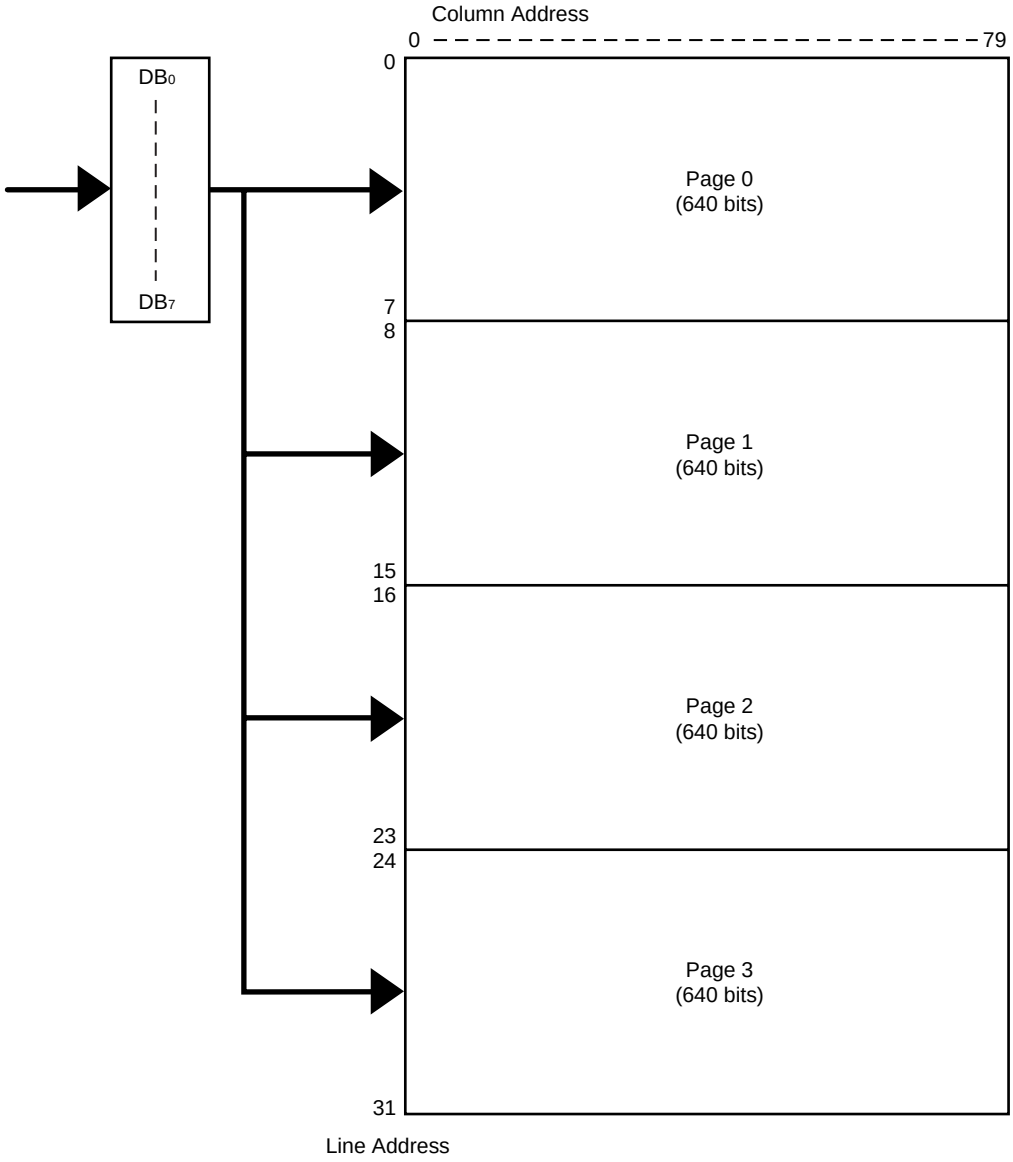
Pin Symbol	Pin Name	Pin No.	I/O	Description
SEG_0 to SEG_{60}	Segment	72 to 12	Output	Segment output pins
COM_0 to COM_{15}	Common	96 to 100, 1 to 11	Output	Common output pins If the chip is a slave, these pins correspond to COM_{16} to COM_{31}.

4. COMMANDS

Command		/RD	/WR	A0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Function
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	ON/OFF of the whole display is performed independent of the display RAM's data or internal state. 1: ON, 0: OFF (Power save at static drive ON)[Note]
2	Display start line	1	0	0	1	1	0	Display start address (0 to 31)					Determines the RAM line displayed on the uppermost line (COM_0) of the display.
3	Page address set	1	0	0	1	0	1	1	1	0	Pages (0 to 3)		Sets display RAM pages in the page address register.
4	Column(segment) address set	1	0	0	0	Column addresses (0 to 79)							Sets display RAM's column address in the column address register.
5	Status read	0	1	0	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads status BUSY 1: During internal operation 0: READY status ADC 1: Clockwise output(Normal rotation) 0: Counterclockwise output (Reverse) ON/OFF 1: Display OFF, 0: Display ON RESET 1: Being reset, 0: Normal
6	Display data write	1	0	1	Write Data								Displays the data bus data and writes it onto the display RAM. Accesses the display RAM of a pre-specified address. After access, the column address is incremented.
7	Display data read	0	1	1	Read data								Reads the data in the display RAM onto the data bus.
8	ADC select	1	0	0	1	0	1	0	0	0	0	0/1	This command is used to reverse the correspondence relationship between display RAM's column addresses and segment driver outputs. 0: Clockwise output (Normal rotation) 1: Counterclockwise output (Reverse)
9	Static drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects between the normal display operation and the static all-lamp-driven display. 1: Static drive (Power save)[Note] 0: Normal display operation
10	Duty select	1	0	0	1	0	1	0	1	0	0	0/1	Selects between two different liquid-crystal cell driving duties. 1: 1/32 duty 0: 1/16 duty
11	Read modify write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter only when writing the display data; but not when reading it.
12	END	1	0	0	1	1	1	0	1	1	1	0	Cancels read modify write mode
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Sets the display start line register to the first line. Sets the column address counter and the page address register to 0.

Note If the static drive is turned ON in the display OFF state, the machine is placed in the power save state.

5. DISPLAY RAM MAP

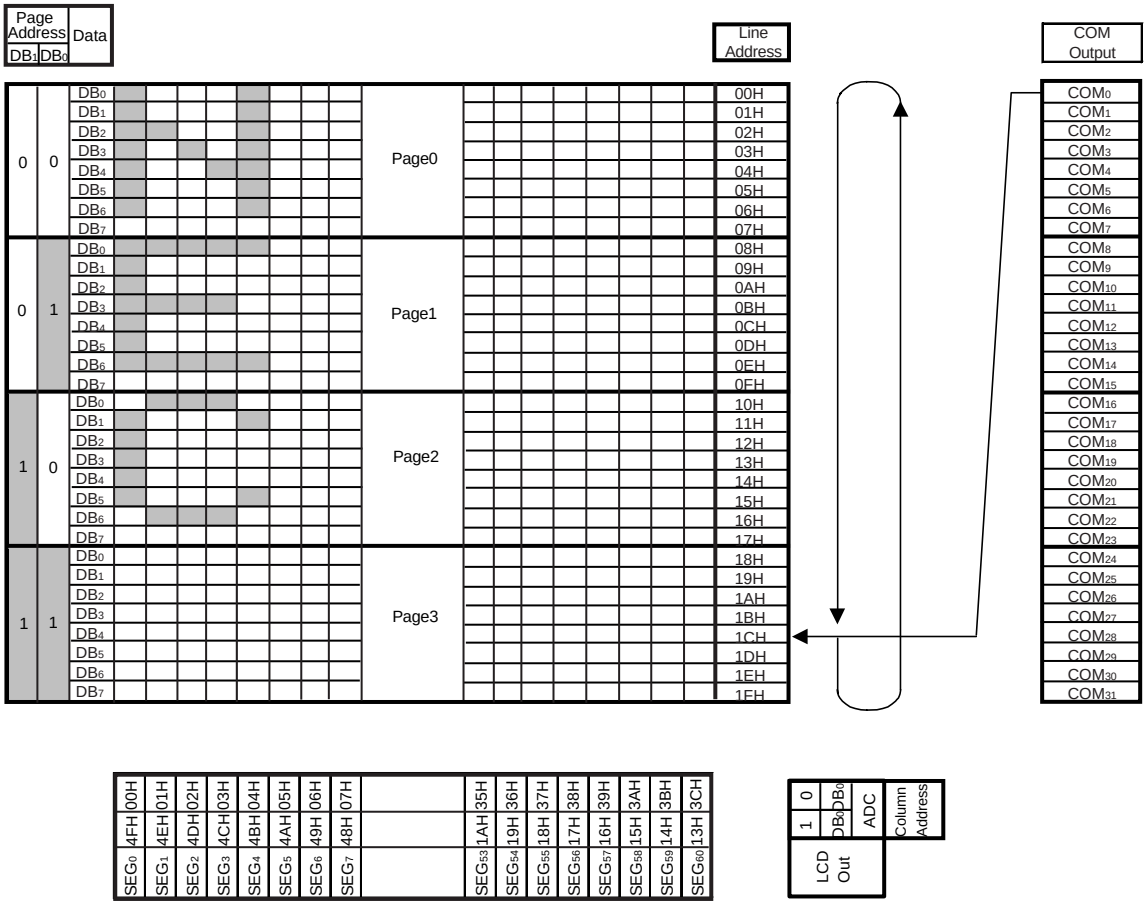


6. Line Address Circuit

As is shown in Figure 6–1, the line address circuit specifies the line address that corresponds to a COM output for displaying the contents of display data RAM. The display start line address set command specifies line address of to the COM_0 output.

The screen can be scrolled by dynamically changing the line address via the display start line address set command.

Figure 6–1. Specification of Display Start Line Address in Display Data RAM



Remark COM_{16} to COM_{31} are valid in only 1/32 duty.

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to +6.5	V
Driver reference supply input voltage	V_{LC1} to V_{LC4}	V_{DD} – 13 to V_{DD} + 0.3	V
	V_{LC5}	V_{DD} – 13 to +0.3	V
Logic system input voltage	V_{IN1}	–0.3 to V_{DD} + 0.3	V
Logic system output voltage	V_{OUT1}	–0.3 to V_{DD} + 0.3	V
Logic system input/output voltage	$V_{I/O1}$	–0.3 to V_{DD} + 0.3	V
Driver system output voltage	V_{OUT2}	V_{LC5} – 0.3 to V_{DD} + 0.3	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Cautions1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. Ensure that the phase relationship is $V_{DD} \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} \geq V_{LC4} \geq V_{LC5}$.

★ **Recommended Operating Range (T_A = –40 to +85°C, V_{SS} = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2.7		5.5	V
Reference supply voltage	V_{LC1} to V_{LC4}	V_{DD} – 12		V_{DD}	V
	V_{LC5}	V_{DD} – 12		0	V
Logic system input voltage	V_{IN1}	0		V_{DD}	V

Electrical Characteristics (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

	Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
	High-level input voltage	V_{IH1}	A0, DB_0 to DB_7, E, R,/W	0.8 V_{DD}			V
		V_{IH2}	FR, M,/S, /RESET	0.8 V_{DD}			V
	Low-level input voltage	V_{IL1}	A0, DB_0 to DB_7, E, R,/W			0.2 V_{DD}	V
		V_{IL2}	FR, M,/S, /RESET			0.2 V_{DD}	V
	High-level input current	I_{IH}	A0, E, R,/W, /RESET			1	μA
	Low-level input current	I_{IL}	A0, E, R,/W, /RESET			–1	μA
	High-level output voltage	V_{OH1}	I_{OUT} = –3 mA, DB_0 to DB_7, V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}			V
		V_{OH2}	I_{OUT} = –2 mA, FR, V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}			V
		V_{OH3}	I_{OUT} = –120 μA, OSC_2, V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}			V
	Low-level output voltage	V_{OL1}	I_{OUT} = 3 mA, DB_0 to DB_7, V_{DD} = 4.5 to 5.5 V			0.2 V_{DD}	V
		V_{OL2}	I_{OUT} = 2 mA, FR, V_{DD} = 4.5 to 5.5 V			0.2 V_{DD}	V
		V_{OL3}	I_{OUT} = 120 μA, OSC_2, V_{DD} = 4.5 to 5.5 V			0.2 V_{DD}	V
	High-level output voltage	V_{OH1}	I_{OUT} = –1.5 mA, DB_0 to DB_7, V_{DD} = 2.7 to 4.5 V	0.8 V_{DD}			V
		V_{OH2}	I_{OUT} = –1 mA, FR, V_{DD} = 2.7 to 4.5 V	0.8 V_{DD}			V
		V_{OH3}	I_{OUT} = –80 μA, OSC_2, V_{DD} = 2.7 to 4.5 V	0.8 V_{DD}			V
	Low-level output voltage	V_{OL1}	I_{OUT} = 1.5 mA, DB_0 to DB_7, V_{DD} = 2.7 to 4.5 V			0.2 V_{DD}	V
		V_{OL2}	I_{OUT} = 1 mA, FR, V_{DD} = 2.7 to 4.5 V			0.2 V_{DD}	V
		V_{OL3}	I_{OUT} = 80 μA, OSC_2, V_{DD} = 2.7 to 4.5 V			0.2 V_{DD}	V
	High-level leak current	I_{LOH}	DB_0 to DB_7, $V_{IN/OUT}$ = V_{DD}			3	μA
	Low-level leak current	I_{LOL}	DB_0 to DB_7, $V_{IN/OUT}$ = V_{SS}			–3	μA
★	Driver output ON resistor	R_{ON1}	T_A = 25°C, V_{DD} = 5 V, V_{LC5} = V_{SS}			7.5	kΩ
★		R_{ON2}	T_A = 25°C, V_{DD} = 3.5 V, V_{LC5} = V_{SS}			50	kΩ
	Static current consumption	I_{DD0}				1.0	μA
	Dynamic current consumption	I_{DD1}	External clock: 18 kHz			15.0	μA
			Self-oscillation: R = 1.3 MΩ			30.0	μA
★		I_{DD2}	During access: t_{CYC} = 200 kHz			500	μA
	Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz			8.0	pF
★	Oscillator frequency	f_{OSC1}	In self-oscillation, V_{DD} = 5.0 V, R = 1.3 MΩ ± 2%	15	18	21	kHz
★		f_{OSC2}	In self-oscillation, V_{DD} = 3.0 V, R = 1.3 MΩ ± 2%	11	16	21	kHz
	Reset time	t_R	/RESET↓ →Internal reset release	1.0		1000	μs

Remark The TYP. value is a reference value when T_A = 25°C.

AC Characteristics 1 (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

80 Series CPU Read/Write Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t_{AH8}	A0	10			ns
Address setup time	t_{AW8}		20			ns
System cycle time	t_{CYC8}	/WR, /RD	1000			ns
Control pulse width	t_{CC}		200			ns
Data setup time	t_{DS8}	DB_0 to DB_7	80			ns
Data hold time	t_{DH8}		10			ns
/RD access time	t_{ACC8}	DB_0 to DB_7, C_L = 100 pF			90	ns
Output disable time	t_{OH8}		10		60	ns

68 Series CPU Read/Write Timing

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
System cycle time		t_{CYC6}	A0, R,/W	1000			ns
Address setup time		t_{AW6}		20			ns
Address hold time		t_{AH6}		10			ns
Data setup time		t_{DS6}	DB_0 to DB_7	80			ns
Data hold time		t_{DH6}		10			ns
Output disable time		t_{OH6}	DB_0 to DB_7, C_L = 100 pF	10		60	ns
Access time		t_{ACC6}				90	ns
Enable pulse width	Read	t_{EW}	E	100			ns
	Write			80			ns

AC Characteristics 2 (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = 2.7 to 4.5 V)

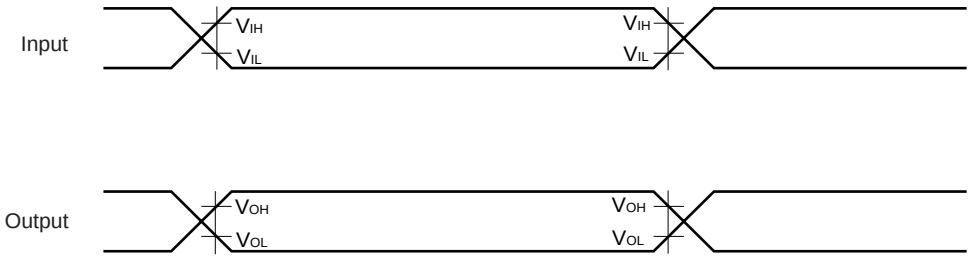
80 Series CPU Read/Write Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t_{AH8}	A0	20			ns
Address setup time	t_{AW8}		40			ns
System cycle time	t_{CYC8}	/WR, /RD	2000			ns
Control pulse width	t_{CC}		400			ns
Data setup time	t_{DS8}	DB_0 to DB_7	160			ns
Data hold time	t_{DH8}		20			ns
/RD access time	t_{ACC8}	DB_0 to DB_7, C_L = 100 pF			180	ns
Output disable time	t_{OH8}		20		120	ns

68 Series CPU Read/Write Timing

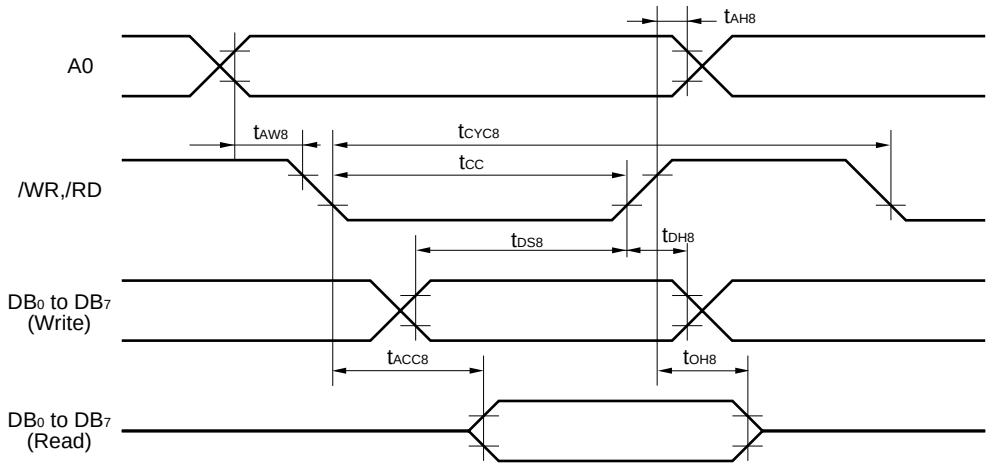
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
System cycle time		t_{CYC6}	A0, R,/W	2000			ns
Address setup time		t_{AW6}		40			ns
Address hold time		t_{AH6}		20			ns
Data setup time		t_{DS6}	DB_0 to DB_7	160			ns
Data hold time		t_{DH6}		20			ns
Output disable time		t_{OH6}	DB_0 to DB_7, C_L = 100 pF	20		120	ns
Access time		t_{ACC6}				180	ns
Enable pulse width	Read	t_{EW}	E	200			ns
	Write			160			ns

Test Point of Switching Characteristics

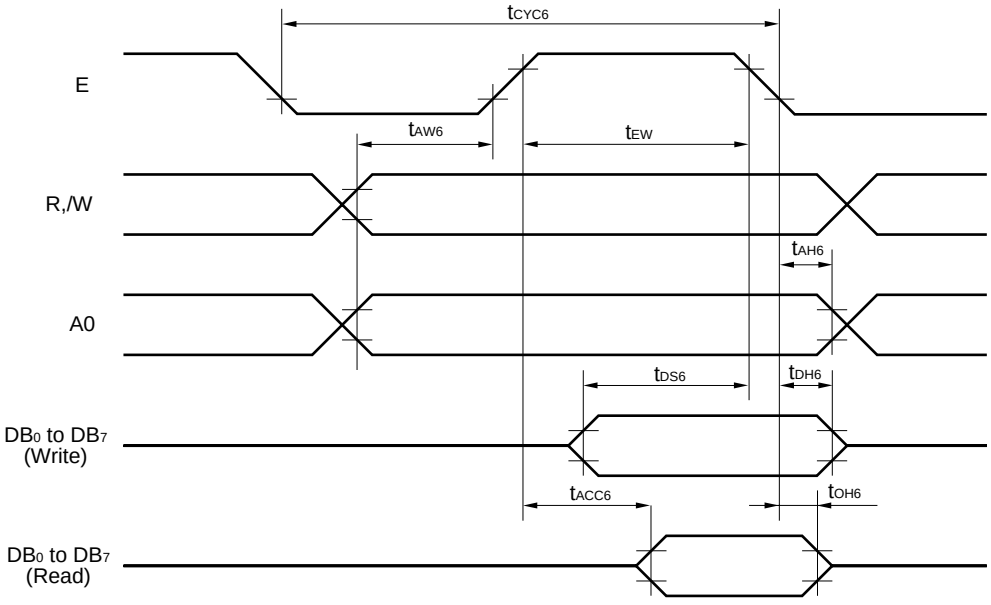


Waveforms of Switching Characteristics

80 Series CPU Read/Write Timing

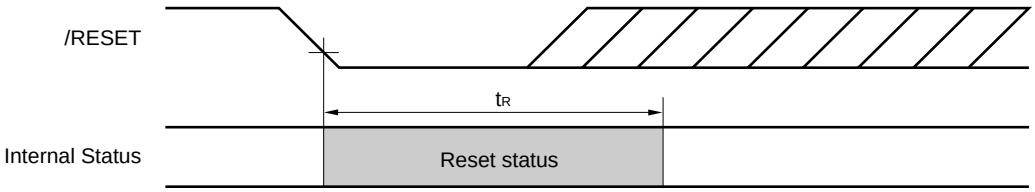


68 Series CPU Read/Write Timing

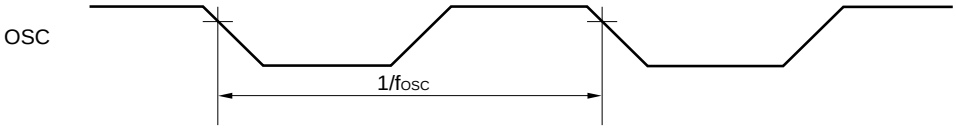


★

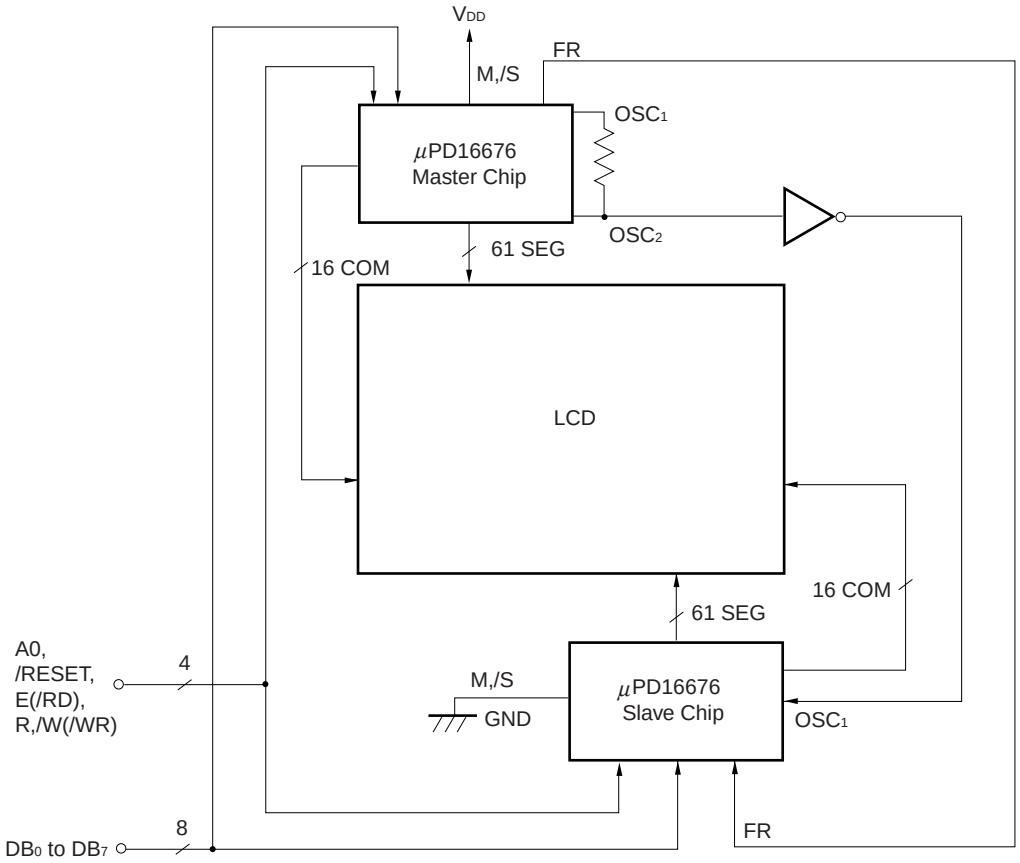
Reset



OSC



8. EXAMPLE of APPLICATION CIRCUIT



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

★ **Reference Documents**

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)