NEC

MOS INTEGRATED CIRCUIT

μPD16710

300/309 OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALE)

DESCRIPTION

The μPD16710 is a source driver for TFT-LCDs capable of dealing with displays with 64 gray scale. Data input is based on digital input configured as 6 bits by 6 dots (1 pixel), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 9-by-2 external power modules. Because the output dynamic range is as large as 9.8 V_{P-P}, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 45 MHz when driving at 3.0 V, this driver is applicable to SVGA/XGA-standard TFT-LCD panels.

FEATURES

- Capable of outputting 64 values by means of 9-by-2 external power modules (18 units) and a D/A converter
- Output dynamic range 9.8 $V_{p-p\ MIN.}$ (@ V_{DD2} = 10.0 V)
- CMOS level input
- Input of 6 bits (gray scale data) by 3 dots
- High-speed data transfer: $f_{max.}$ = 45 MHz (internal data transfer speed when operating at 3.0 V)
- 300/309 outputs
- Dedicated to dot inversion
- Input data inversion function (POL2)
- Single-sided mounting possible (loaded with slim TCP)

ORDERING INFORMATION

Part Number	Package
μPD16710N-×××	TCP (TAB)

The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

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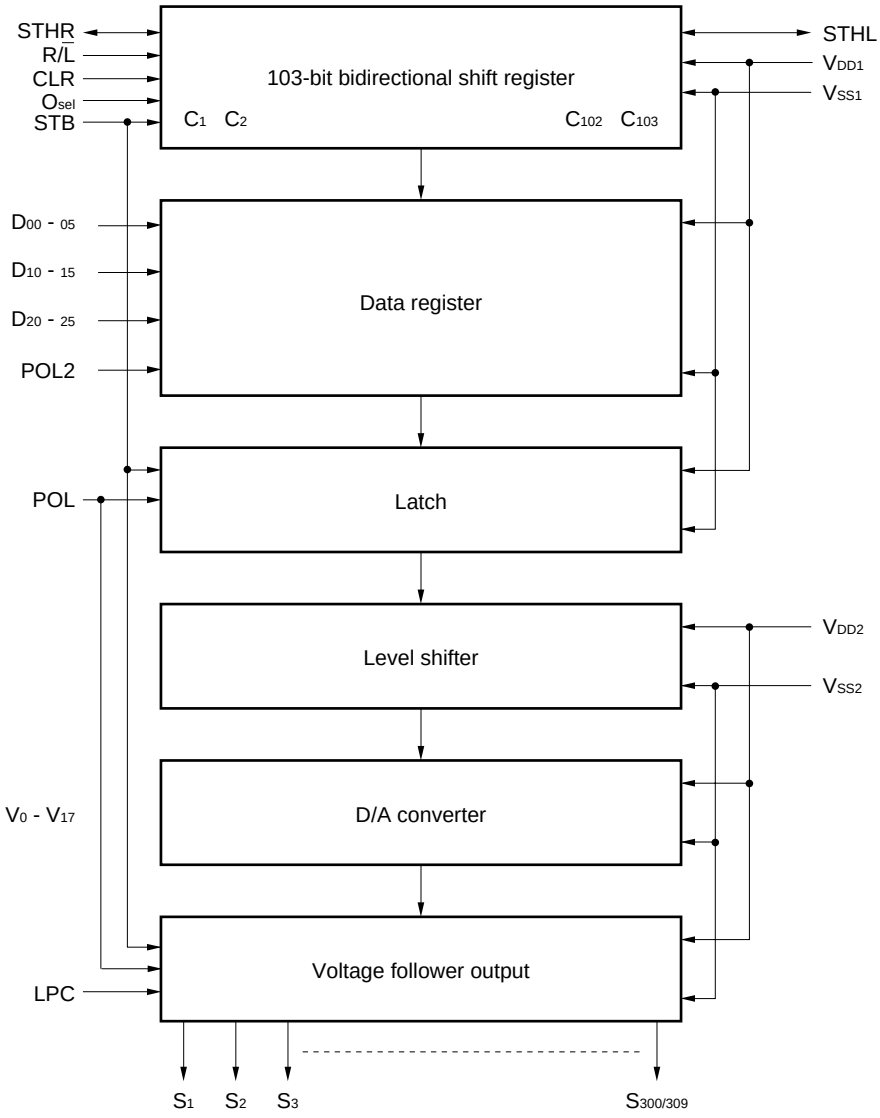
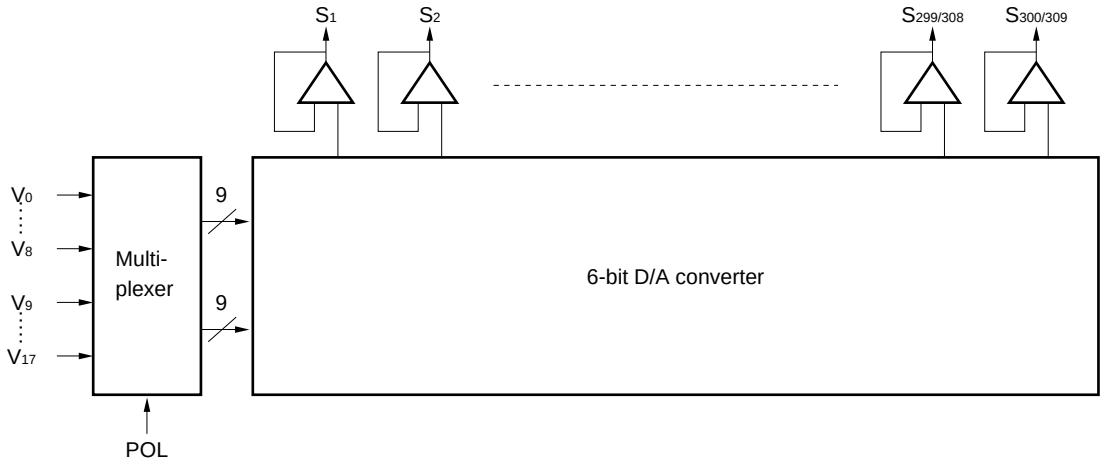
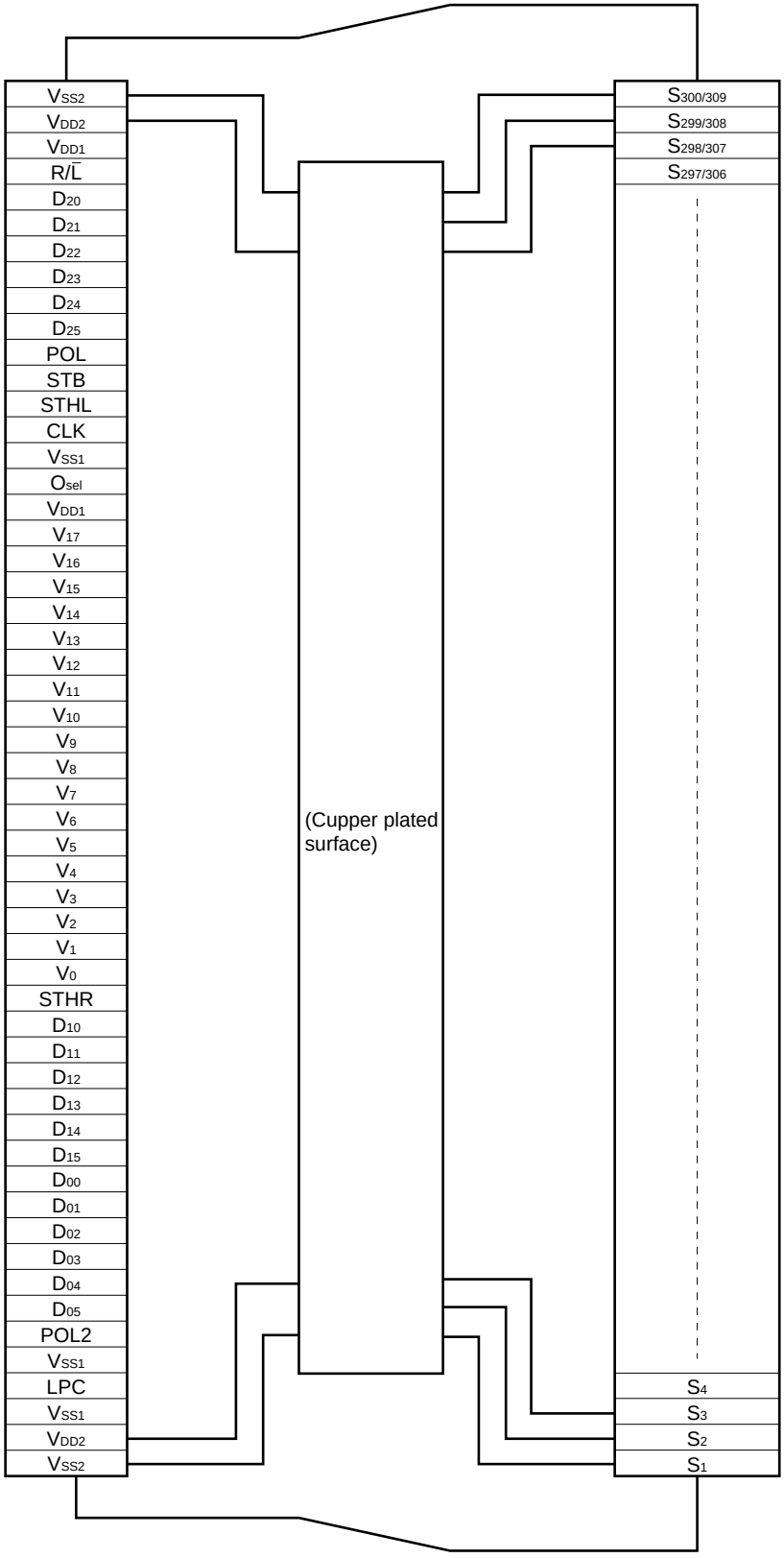
1. BLOCK DIAGRAM



2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONNECTION DIAGRAM (μPD16710N-×××) (TOP VIEW OF COPPER FOIL SURFACE)



Caution This diagram does not represent the actual shape of TCP.
LPC is internally pulled up to V_{DD1}.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to $S_{300/309}$	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05}	Display data input	The display data is input with a width of 18 bits, viz., the gray scale data (6 bits) by 3 dots (1 pixel). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
R/$\overline{L}$	Shift direction switching input pin	Shift direction switching pin of shift register. The shift directions are as follows. R/$\overline{L}$ = H (right shift): STHR (input) → S_1 → $S_{300/309}$ → STHL (output) R/$\overline{L}$ = L (left shift) : STHL (input) → $S_{300/309}$ → S_1 → STHR (output)
STHR	Right shift start pulse input/output	Start pulse I/O pins when two or more μPD16710's are connected in cascade. When H level of these pins is read at the rising edge of CLK, input of display data is started. In the case of right shift, STHR serves as an input pin and STHL serves as an output pin. In the case of left shift, STHL serves as an input pin and STHR serves as an output pin.
STHL	Left shift start pulse input/output	
CLK	Shift clock input	Shift clock input to shift register. Display data is loaded to the data register at the rising edge of this signal. The start pulse output goes high and is used as the start pulse for the driver on the next stage at the rising edge of the 103rd clock in the 309-output mode (100th clock in the 300-output mode). When 105 clock pulses (102 pulses in the 300-output mode) are input after the start pulse has been input, loading the display data is automatically stopped, and the contents of the shift register are cleared at the rising edge of STB.
STB	Latch input	The contents of the data register are transferred to the latch at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
O_{sel}	Number of output pins select pin	This pin selects the number of output pins. O_{sel} = L : 309-output mode O_{sel} = H : 300-output mode
POL	Polarity input	POL = L ; S_{2n-1} output uses V_9 to V_{17} and S_{2n} output uses V_0 to V_8 as the reference power supply. POL = H ; S_{2n-1} output uses V_0 to V_8 and S_{2n} output uses V_9 to V_{17} as the reference power supply. S_{2n-1} indicates odd-numbered output pins and S_{2n} indicates even-numbered output pins. The POL signal is input after a specified setup time ($t_{POL-STB}$) from the rising edge of STB.
POL2	Data inversion	POL2 = H : Data is internally inverted in the IC. POL2 = L : The input data is not inverted.
LPC	Low-power control input	Reduces current consumption by cutting off the constant-current supply to the output buffer. In the low-power mode (LPC = H: DC level can be input), the static current consumption can be reduced.
V_0 to V_{17}	γ-corrected power supplies	Input the γ-corrected power supplies from outside. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{SS2}$
V_{DD1}	Logic part power supply	3.3 V ± 0.3 V
V_{DD2}	Driver part power supply	9.0 V to 12.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

5. CAUTIONS

(1) The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_{17} in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_{17} is possible.)

(2) To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ⋯, V_{17}) and V_{SS2}.

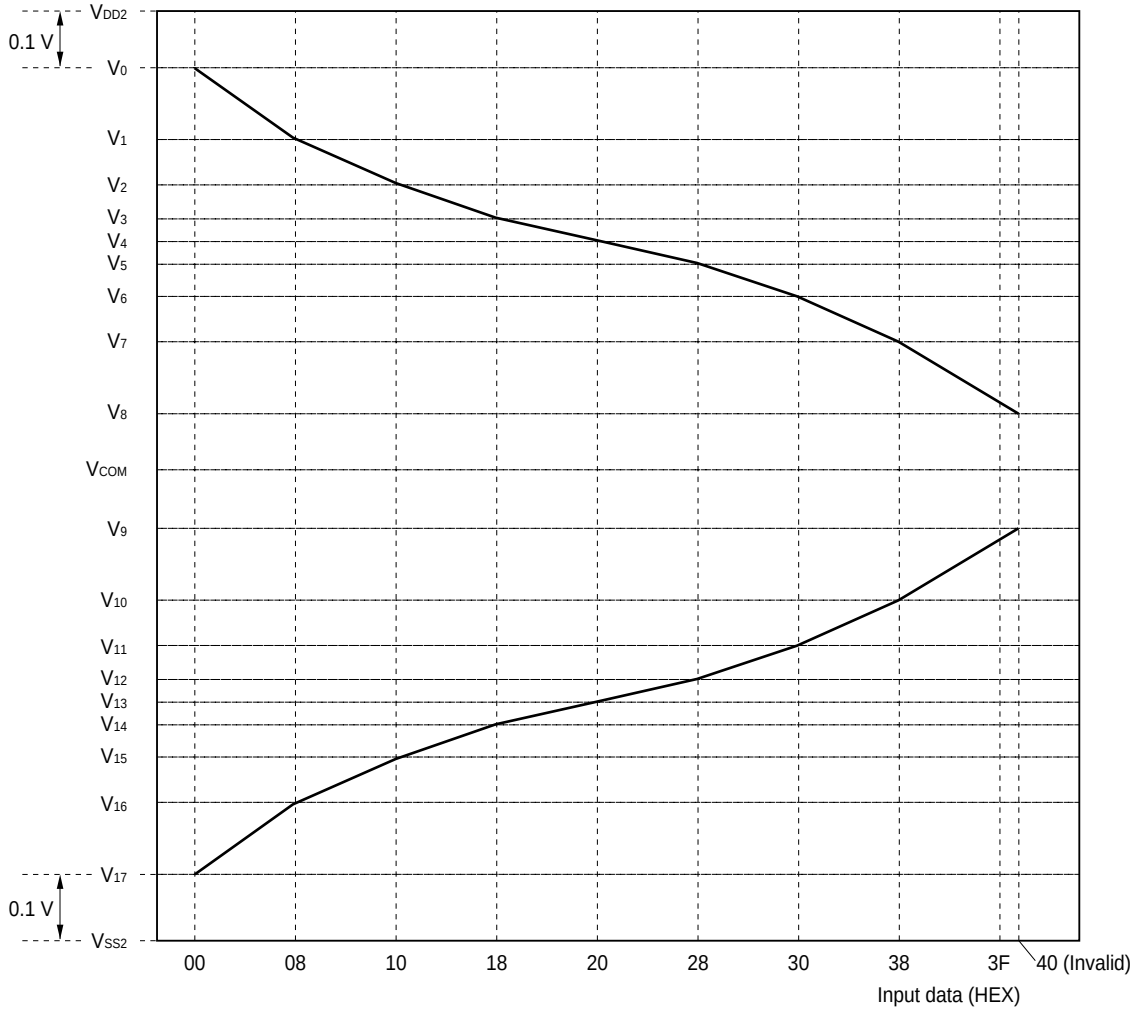
6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ-corrected voltages and V_0' to V_{63}' and V_0" to V_{63}" are roughly equal; and their respective resistance values are as shown on page 9. Among the 9-by-2 γ-corrected voltages, input gray scale voltages of the same polarity with respect to the common electrode, for the respective nine γ-corrected voltages of V_0 to V_8 and V_9 to V_{17}.

Figure 1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_{17} and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{SS2}$. Figures 2-1 and 2-2 show the relationship between the input data and the output data. Table 1 shows the resistance values of the resistor strings.

This driver IC is designed for dot inversion in single-sided mounting. Therefore, please do not use it in double-sided mounting.

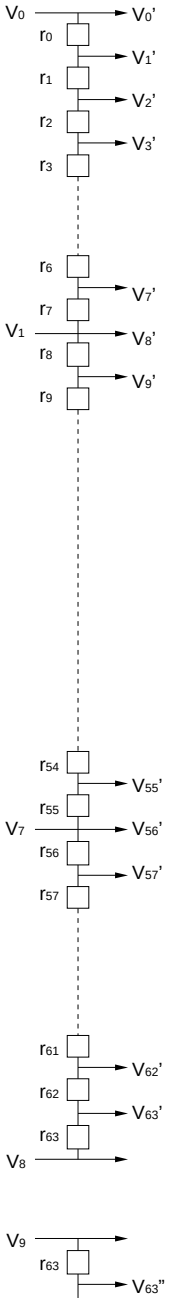
Figure 1. Relationship Between Input Data and Output Voltage



7. RESISTOR STRINGS

(Relationship Between Input Data and Output Voltage: $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9$)

Figure 2-1

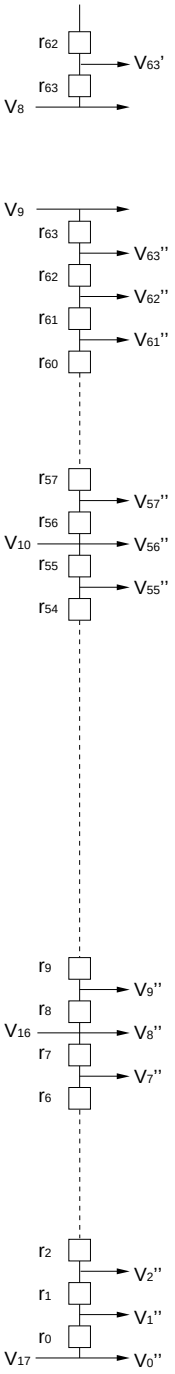


Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00_H	0	0	0	0	0	0	V_0'	V_0
01_H	0	0	0	0	0	1	V_1'	$V_1 + (V_0 - V_1) \times 7/8$
02_H	0	0	0	0	1	0	V_2'	$V_1 + (V_0 - V_1) \times 6/8$
03_H	0	0	0	0	1	1	V_3'	$V_1 + (V_0 - V_1) \times 5/8$
04_H	0	0	0	1	0	0	V_4'	$V_1 + (V_0 - V_1) \times 4/8$
05_H	0	0	0	1	0	1	V_5'	$V_1 + (V_0 - V_1) \times 3/8$
06_H	0	0	0	1	1	0	V_6'	$V_1 + (V_0 - V_1) \times 2/8$
07_H	0	0	0	1	1	1	V_7'	$V_1 + (V_0 - V_1) \times 1/8$
08_H	0	0	1	0	0	0	V_8'	V_1
09_H	0	0	1	0	0	1	V_9'	$V_2 + (V_1 - V_2) \times 7/8$
$0A_H$	0	0	1	0	1	0	V_{10}'	$V_2 + (V_1 - V_2) \times 6/8$
$0B_H$	0	0	1	0	1	1	V_{11}'	$V_2 + (V_1 - V_2) \times 5/8$
$0C_H$	0	0	1	1	0	0	V_{12}'	$V_2 + (V_1 - V_2) \times 4/8$
$0D_H$	0	0	1	1	0	1	V_{13}'	$V_2 + (V_1 - V_2) \times 3/8$
$0E_H$	0	0	1	1	1	0	V_{14}'	$V_2 + (V_1 - V_2) \times 2/8$
$0F_H$	0	0	1	1	1	1	V_{15}'	$V_2 + (V_1 - V_2) \times 1/8$
10_H	0	1	0	0	0	0	V_{16}'	V_2
11_H	0	1	0	0	0	1	V_{17}'	$V_3 + (V_2 - V_3) \times 7/8$
12_H	0	1	0	0	1	0	V_{18}'	$V_3 + (V_2 - V_3) \times 6/8$
13_H	0	1	0	0	1	1	V_{19}'	$V_3 + (V_2 - V_3) \times 5/8$
14_H	0	1	0	1	0	0	V_{20}'	$V_3 + (V_2 - V_3) \times 4/8$
15_H	0	1	0	1	0	1	V_{21}'	$V_3 + (V_2 - V_3) \times 3/8$
16_H	0	1	0	1	1	0	V_{22}'	$V_3 + (V_2 - V_3) \times 2/8$
17_H	0	1	0	1	1	1	V_{23}'	$V_3 + (V_2 - V_3) \times 1/8$
18_H	0	1	1	0	0	0	V_{24}'	V_3
19_H	0	1	1	0	0	1	V_{25}'	$V_4 + (V_3 - V_4) \times 7/8$
$1A_H$	0	1	1	0	1	0	V_{26}'	$V_4 + (V_3 - V_4) \times 6/8$
$1B_H$	0	1	1	0	1	1	V_{27}'	$V_4 + (V_3 - V_4) \times 5/8$
$1C_H$	0	1	1	1	0	0	V_{28}'	$V_4 + (V_3 - V_4) \times 4/8$
$1D_H$	0	1	1	1	0	1	V_{29}'	$V_4 + (V_3 - V_4) \times 3/8$
$1E_H$	0	1	1	1	1	0	V_{30}'	$V_4 + (V_3 - V_4) \times 2/8$
$1F_H$	0	1	1	1	1	1	V_{31}'	$V_4 + (V_3 - V_4) \times 1/8$
20_H	1	0	0	0	0	0	V_{32}'	V_4
21_H	1	0	0	0	0	1	V_{33}'	$V_5 + (V_4 - V_5) \times 7/8$
22_H	1	0	0	0	1	0	V_{34}'	$V_5 + (V_4 - V_5) \times 6/8$
23_H	1	0	0	0	1	1	V_{35}'	$V_5 + (V_4 - V_5) \times 5/8$
24_H	1	0	0	1	0	0	V_{36}'	$V_5 + (V_4 - V_5) \times 4/8$
25_H	1	0	0	1	0	1	V_{37}'	$V_5 + (V_4 - V_5) \times 3/8$
26_H	1	0	0	1	1	0	V_{38}'	$V_5 + (V_4 - V_5) \times 2/8$
27_H	1	0	0	1	1	1	V_{39}'	$V_5 + (V_4 - V_5) \times 1/8$
28_H	1	0	1	0	0	0	V_{40}'	V_5
29_H	1	0	1	0	0	1	V_{41}'	$V_6 + (V_5 - V_6) \times 7/8$
$2A_H$	1	0	1	0	1	0	V_{42}'	$V_6 + (V_5 - V_6) \times 6/8$
$2B_H$	1	0	1	0	1	1	V_{43}'	$V_6 + (V_5 - V_6) \times 5/8$
$2C_H$	1	0	1	1	0	0	V_{44}'	$V_6 + (V_5 - V_6) \times 4/8$
$2D_H$	1	0	1	1	0	1	V_{45}'	$V_6 + (V_5 - V_6) \times 3/8$
$2E_H$	1	0	1	1	1	0	V_{46}'	$V_6 + (V_5 - V_6) \times 2/8$
$2F_H$	1	0	1	1	1	1	V_{47}'	$V_6 + (V_5 - V_6) \times 1/8$
30_H	1	1	0	0	0	0	V_{48}'	V_6
31_H	1	1	0	0	0	1	V_{49}'	$V_7 + (V_6 - V_7) \times 7/8$
32_H	1	1	0	0	1	0	V_{50}'	$V_7 + (V_6 - V_7) \times 6/8$
33_H	1	1	0	0	1	1	V_{51}'	$V_7 + (V_6 - V_7) \times 5/8$
34_H	1	1	0	1	0	0	V_{52}'	$V_7 + (V_6 - V_7) \times 4/8$
35_H	1	1	0	1	0	1	V_{53}'	$V_7 + (V_6 - V_7) \times 3/8$
36_H	1	1	0	1	1	0	V_{54}'	$V_7 + (V_6 - V_7) \times 2/8$
37_H	1	1	0	1	1	1	V_{55}'	$V_7 + (V_6 - V_7) \times 1/8$
38_H	1	1	1	0	0	0	V_{56}'	V_7
39_H	1	1	1	0	0	1	V_{57}'	$V_8 + (V_7 - V_8) \times 7/8$
$3A_H$	1	1	1	0	1	0	V_{58}'	$V_8 + (V_7 - V_8) \times 6/8$
$3B_H$	1	1	1	0	1	1	V_{59}'	$V_8 + (V_7 - V_8) \times 5/8$
$3C_H$	1	1	1	1	0	0	V_{60}'	$V_8 + (V_7 - V_8) \times 4/8$
$3D_H$	1	1	1	1	0	1	V_{61}'	$V_8 + (V_7 - V_8) \times 3/8$
$3E_H$	1	1	1	1	1	0	V_{62}'	$V_8 + (V_7 - V_8) \times 2/8$
$3F_H$	1	1	1	1	1	1	V_{63}'	$V_8 + (V_7 - V_8) \times 1/8$

Caution V_8 and V_9 are not interconnected inside the IC.

(**Relationship Between Input Data and Output Voltage: $V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{SS2}$**)

Figure 2-2



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00H	0	0	0	0	0	0	V_0''	V_{17}
01H	0	0	0	0	0	1	V_1''	$V_{17} + (V_{16} - V_{17}) \times 1/8$
02H	0	0	0	0	1	0	V_2''	$V_{17} + (V_{16} - V_{17}) \times 2/8$
03H	0	0	0	0	1	1	V_3''	$V_{17} + (V_{16} - V_{17}) \times 3/8$
04H	0	0	0	1	0	0	V_4''	$V_{17} + (V_{16} - V_{17}) \times 4/8$
05H	0	0	0	1	0	1	V_5''	$V_{17} + (V_{16} - V_{17}) \times 5/8$
06H	0	0	0	1	1	0	V_6''	$V_{17} + (V_{16} - V_{17}) \times 6/8$
07H	0	0	0	1	1	1	V_7''	$V_{17} + (V_{16} - V_{17}) \times 7/8$
08H	0	0	1	0	0	0	V_8''	V_{16}
09H	0	0	1	0	0	1	V_9''	$V_{16} + (V_{15} - V_{16}) \times 1/8$
0AH	0	0	1	0	1	0	V_{10}''	$V_{16} + (V_{15} - V_{16}) \times 2/8$
0BH	0	0	1	0	1	1	V_{11}''	$V_{16} + (V_{15} - V_{16}) \times 3/8$
0CH	0	0	1	1	0	0	V_{12}''	$V_{16} + (V_{15} - V_{16}) \times 4/8$
0DH	0	0	1	1	0	1	V_{13}''	$V_{16} + (V_{15} - V_{16}) \times 5/8$
0EH	0	0	1	1	1	0	V_{14}''	$V_{16} + (V_{15} - V_{16}) \times 6/8$
0FH	0	0	1	1	1	1	V_{15}''	$V_{16} + (V_{15} - V_{16}) \times 7/8$
10H	0	1	0	0	0	0	V_{16}''	V_{15}
11H	0	1	0	0	0	1	V_{17}''	$V_{15} + (V_{14} - V_{15}) \times 1/8$
12H	0	1	0	0	1	0	V_{18}''	$V_{15} + (V_{14} - V_{15}) \times 2/8$
13H	0	1	0	0	1	1	V_{19}''	$V_{15} + (V_{14} - V_{15}) \times 3/8$
14H	0	1	0	1	0	0	V_{20}''	$V_{15} + (V_{14} - V_{15}) \times 4/8$
15H	0	1	0	1	0	1	V_{21}''	$V_{15} + (V_{14} - V_{15}) \times 5/8$
16H	0	1	0	1	1	0	V_{22}''	$V_{15} + (V_{14} - V_{15}) \times 6/8$
17H	0	1	0	1	1	1	V_{23}''	$V_{15} + (V_{14} - V_{15}) \times 7/8$
18H	0	1	1	0	0	0	V_{24}''	V_{14}
19H	0	1	1	0	0	1	V_{25}''	$V_{14} + (V_{13} - V_{14}) \times 1/8$
1AH	0	1	1	0	1	0	V_{26}''	$V_{14} + (V_{13} - V_{14}) \times 2/8$
1BH	0	1	1	0	1	1	V_{27}''	$V_{14} + (V_{13} - V_{14}) \times 3/8$
1CH	0	1	1	1	0	0	V_{28}''	$V_{14} + (V_{13} - V_{14}) \times 4/8$
1DH	0	1	1	1	0	1	V_{29}''	$V_{14} + (V_{13} - V_{14}) \times 5/8$
1EH	0	1	1	1	1	0	V_{30}''	$V_{14} + (V_{13} - V_{14}) \times 6/8$
1FH	0	1	1	1	1	1	V_{31}''	$V_{14} + (V_{13} - V_{14}) \times 7/8$
20H	1	0	0	0	0	0	V_{32}''	V_{13}
21H	1	0	0	0	0	1	V_{33}''	$V_{13} + (V_{12} - V_{13}) \times 1/8$
22H	1	0	0	0	1	0	V_{34}''	$V_{13} + (V_{12} - V_{13}) \times 2/8$
23H	1	0	0	0	1	1	V_{35}''	$V_{13} + (V_{12} - V_{13}) \times 3/8$
24H	1	0	0	1	0	0	V_{36}''	$V_{13} + (V_{12} - V_{13}) \times 4/8$
25H	1	0	0	1	0	1	V_{37}''	$V_{13} + (V_{12} - V_{13}) \times 5/8$
26H	1	0	0	1	1	0	V_{38}''	$V_{13} + (V_{12} - V_{13}) \times 6/8$
27H	1	0	0	1	1	1	V_{39}''	$V_{13} + (V_{12} - V_{13}) \times 7/8$
28H	1	0	1	0	0	0	V_{40}''	V_{12}
29H	1	0	1	0	0	1	V_{41}''	$V_{12} + (V_{11} - V_{12}) \times 1/8$
2AH	1	0	1	0	1	0	V_{42}''	$V_{12} + (V_{11} - V_{12}) \times 2/8$
2BH	1	0	1	0	1	1	V_{43}''	$V_{12} + (V_{11} - V_{12}) \times 3/8$
2CH	1	0	1	1	0	0	V_{44}''	$V_{12} + (V_{11} - V_{12}) \times 4/8$
2DH	1	0	1	1	0	1	V_{45}''	$V_{12} + (V_{11} - V_{12}) \times 5/8$
2EH	1	0	1	1	1	0	V_{46}''	$V_{12} + (V_{11} - V_{12}) \times 6/8$
2FH	1	0	1	1	1	1	V_{47}''	$V_{12} + (V_{11} - V_{12}) \times 7/8$
30H	1	1	0	0	0	0	V_{48}''	V_{11}
31H	1	1	0	0	0	1	V_{49}''	$V_{11} + (V_{10} - V_{11}) \times 1/8$
32H	1	1	0	0	1	0	V_{50}''	$V_{11} + (V_{10} - V_{11}) \times 2/8$
33H	1	1	0	0	1	1	V_{51}''	$V_{11} + (V_{10} - V_{11}) \times 3/8$
34H	1	1	0	1	0	0	V_{52}''	$V_{11} + (V_{10} - V_{11}) \times 4/8$
35H	1	1	0	1	0	1	V_{53}''	$V_{11} + (V_{10} - V_{11}) \times 5/8$
36H	1	1	0	1	1	0	V_{54}''	$V_{11} + (V_{10} - V_{11}) \times 6/8$
37H	1	1	0	1	1	1	V_{55}''	$V_{11} + (V_{10} - V_{11}) \times 7/8$
38H	1	1	1	0	0	0	V_{56}''	V_{10}
39H	1	1	1	0	0	1	V_{57}''	$V_{10} + (V_9 - V_{10}) \times 1/8$
3AH	1	1	1	0	1	0	V_{58}''	$V_{10} + (V_9 - V_{10}) \times 2/8$
3BH	1	1	1	0	1	1	V_{59}''	$V_{10} + (V_9 - V_{10}) \times 3/8$
3CH	1	1	1	1	0	0	V_{60}''	$V_{10} + (V_9 - V_{10}) \times 4/8$
3DH	1	1	1	1	0	1	V_{61}''	$V_{10} + (V_9 - V_{10}) \times 5/8$
3EH	1	1	1	1	1	0	V_{62}''	$V_{10} + (V_9 - V_{10}) \times 6/8$
3FH	1	1	1	1	1	1	V_{63}''	$V_{10} + (V_9 - V_{10}) \times 7/8$

Caution V_8 and V_9 are not interconnected inside the IC.

LADDER RESISTANCE VALUES (r_0 to r_{62}): REFERENCE VALUE

	Resistance Name	Resistance Value (Ω)	Resistance Name	Resistance Value (Ω)	
V_0, V_{17} →	r_0	380	r_{32}	191	← V_4, V_{13}
	r_1	380	r_{33}	191	
	r_2	380	r_{34}	191	
	r_3	380	r_{35}	191	
	r_4	380	r_{36}	191	
	r_5	380	r_{37}	191	
	r_6	380	r_{38}	191	
V_1, V_{16} →	r_7	380	r_{39}	191	← V_5, V_{12}
	r_8	191	r_{40}	191	
	r_9	191	r_{41}	191	
	r_{10}	191	r_{42}	191	
	r_{11}	191	r_{43}	191	
	r_{12}	191	r_{44}	191	
	r_{13}	191	r_{45}	191	
	r_{14}	191	r_{46}	191	
V_2, V_{15} →	r_{15}	191	r_{47}	191	← V_6, V_{11}
	r_{16}	191	r_{48}	191	
	r_{17}	191	r_{49}	191	
	r_{18}	191	r_{50}	191	
	r_{19}	191	r_{51}	191	
	r_{20}	191	r_{52}	191	
	r_{21}	191	r_{53}	191	
	r_{22}	191	r_{54}	191	
V_3, V_{14} →	r_{23}	191	r_{55}	191	← V_7, V_{10}
	r_{24}	191	r_{56}	380	
	r_{25}	191	r_{57}	380	
	r_{26}	191	r_{58}	380	
	r_{27}	191	r_{59}	380	
	r_{28}	191	r_{60}	380	
	r_{29}	191	r_{61}	380	
	r_{30}	191	r_{62}	380	
V_4, V_{13} →	r_{31}	191	r_{63}	380	← V_8, V_9
			Total	15260	

8. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × RGBs (3 dots)
Input width : 18 bits (1-pixel data)

(1) $R/\overline{L}$ = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	$S_{299/308}$	$S_{300/309}$
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	···	D_{10} to D_{15}	D_{20} to D_{25}

(2) $R/\overline{L}$ = L (Left shift)

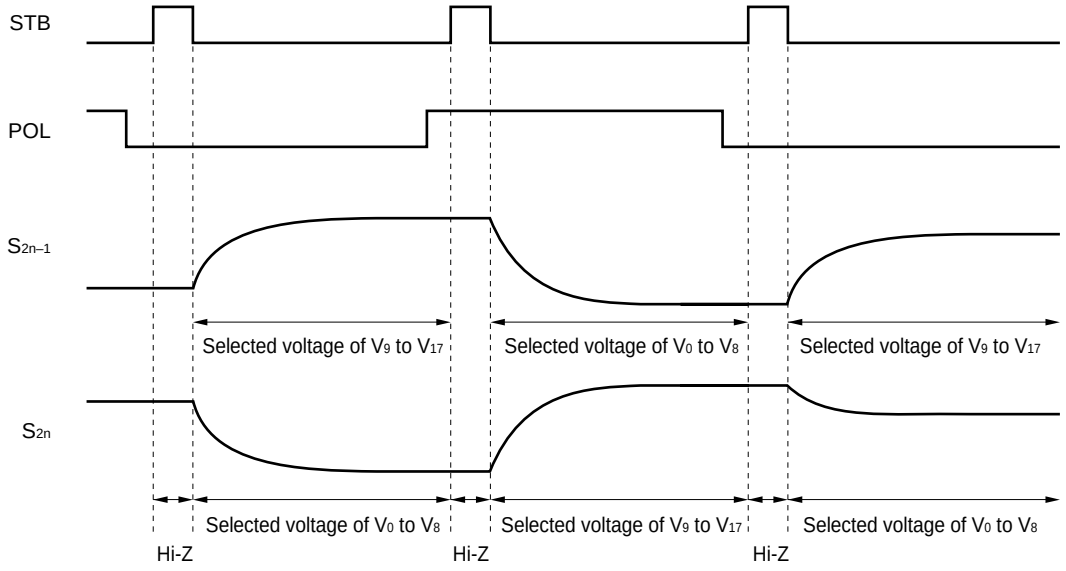
Output	S_1	S_2	S_3	S_4	···	$S_{299/308}$	$S_{300/309}$
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	···	D_{10} to D_{15}	D_{20} to D_{25}

POL	S_{2n-1}	S_{2n}
L	V_9 to V_{17}	V_0 to V_8
H	V_0 to V_8	V_9 to V_{17}

S_{2n-1} (Odd output), S_{2n} (Even output) n = 1, 2, ·····, 155 (excluding S_{310})

9. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

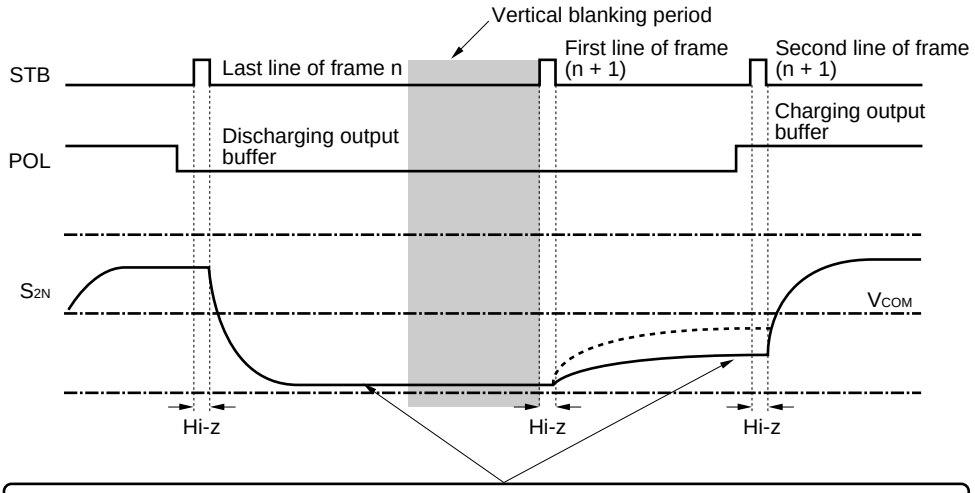


10. NOTES ON FRAME INVERSION

The μPD16710 is an IC for dot inversion and inverts dots by alternately using a charging output buffer and a discharging output buffer. Therefore, the output voltage of the first line may not be correctly written because the last line's output polarity of frame n (n + 1) and the first line's output polarity are the same (refer to **Figure 3**).

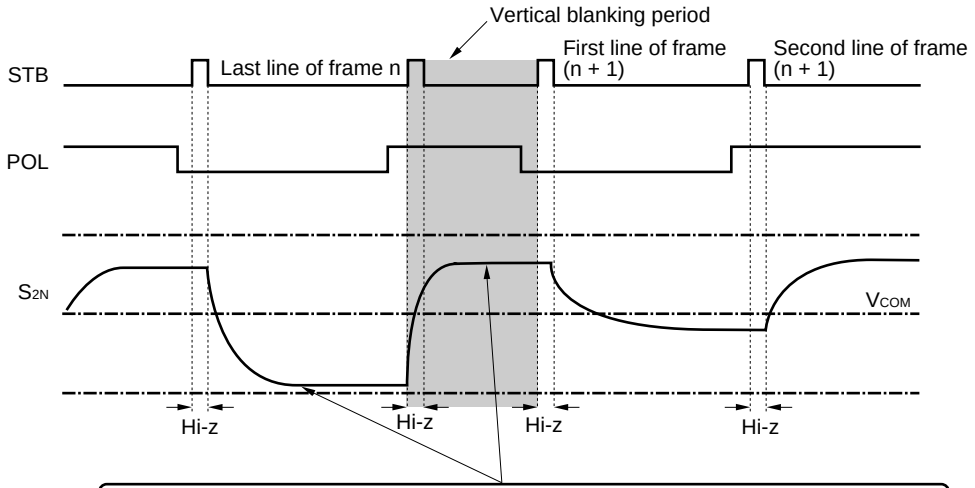
Consequently, polarity inversion and write operation must be performed between frames (vertical blanking period) in order to invert (clear) the polarity of the wiring level of the liquid crystal panel by using the last line output of the previous frame (refer to **Figure 4**).

Figure 3



If the write voltage of the first line of the last (n + 1) frame is greater than the write voltage of the last line of frame n, the targeted voltage cannot be correctly written with the discharging buffer with a low charging capability.

Figure 4



Because data of negative polarity is to be written on the first line of frame (n + 1), write data of positive polarity in advance during the vertical blanking period.

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +5.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +15.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Temperature Range	T_A	–10 to +75	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	9.0		12.5	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ-Corrected Supply Voltage	V_0 to V_{17}	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Driver Part Output Voltage	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{max.}$	45			MHz

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 9.0 V to 12.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leakage Current	I_L					±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1			V
Low-level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA				0.1	V
γ-Corrected Static Current Consumption	I_γ	V_0 to V_8 = V_9 to V_{17} = 4.0 V	V_0, V_9	131	262	524	μA
			V_8, V_{17}	–131	–262	–524	μA
Driver Output Current	I_{VOH}	V_X = 8.0 V, V_{OUT} = 7.5 V			–0.59	–0.1	mA
	I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V		0.1	0.34		mA

V_X refers to the output voltage of analog output pins S_1 to $S_{300/309}$.

V_{OUT} refers to the voltage applied to analog output pins S_1 to $S_{300/309}$.

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 9.0 V to 12.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage Deviation	ΔV_O	All input data		±5	±20	mV
Average Output Voltage Deviation	ΔV_{AV}	All input data		±10		mV
Driver Output Voltage Range	V_O	All input data	0.1		V_{DD2} – 0.1	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}; with no load		3.0	8.0	mA
Driver Part Dynamic Current Consumption	I_{DD21}	V_{DD2} = 9.5 V, LPC = L, with no load		5.0	12.0	mA
Driver Part Dynamic Current Consumption	I_{DD22}	V_{DD2} = 12.0 V, LPC = L, with no load		7.5	17.0	mA

Remarks 1. The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).

2. The average output voltage deviation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same. The average output voltage deviation is a reference value.

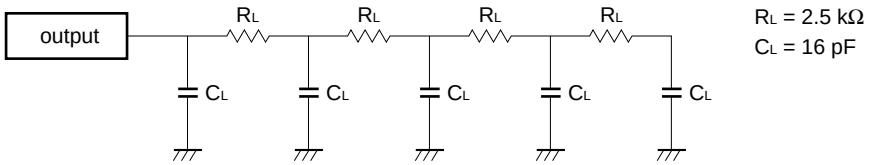
3. The STB cycle is defined to be 15 μs at f_{CLK} = 32.5 MHz.
The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

4. Refers to the current consumption per driver when cascades are connected under the assumption of SVGA single-sided mounting (10 units).
When LPC = H level, the static current consumption can be reduced by 50%.

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 9.0 V to 12.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF		11	17	ns
Driver Output Delay Time	t_{PLH2}	R_L = 2.5 kΩ × 4 C_L = 16 pF × 5		2.0	10	μs
	t_{PLH3}			3.1	15	μs
	t_{PHL2}			2.0	10	μs
	t_{PHL3}			4.3	15	μs
Input Capacitance 1	C_{I1}	STHR (STHL) excluded, T_A = 25 °C		5.5	15	pF
Input Capacitance 2	C_{I2}	STHR (STHL), T_A = 25 °C		5.6	15	pF

<Test condition>



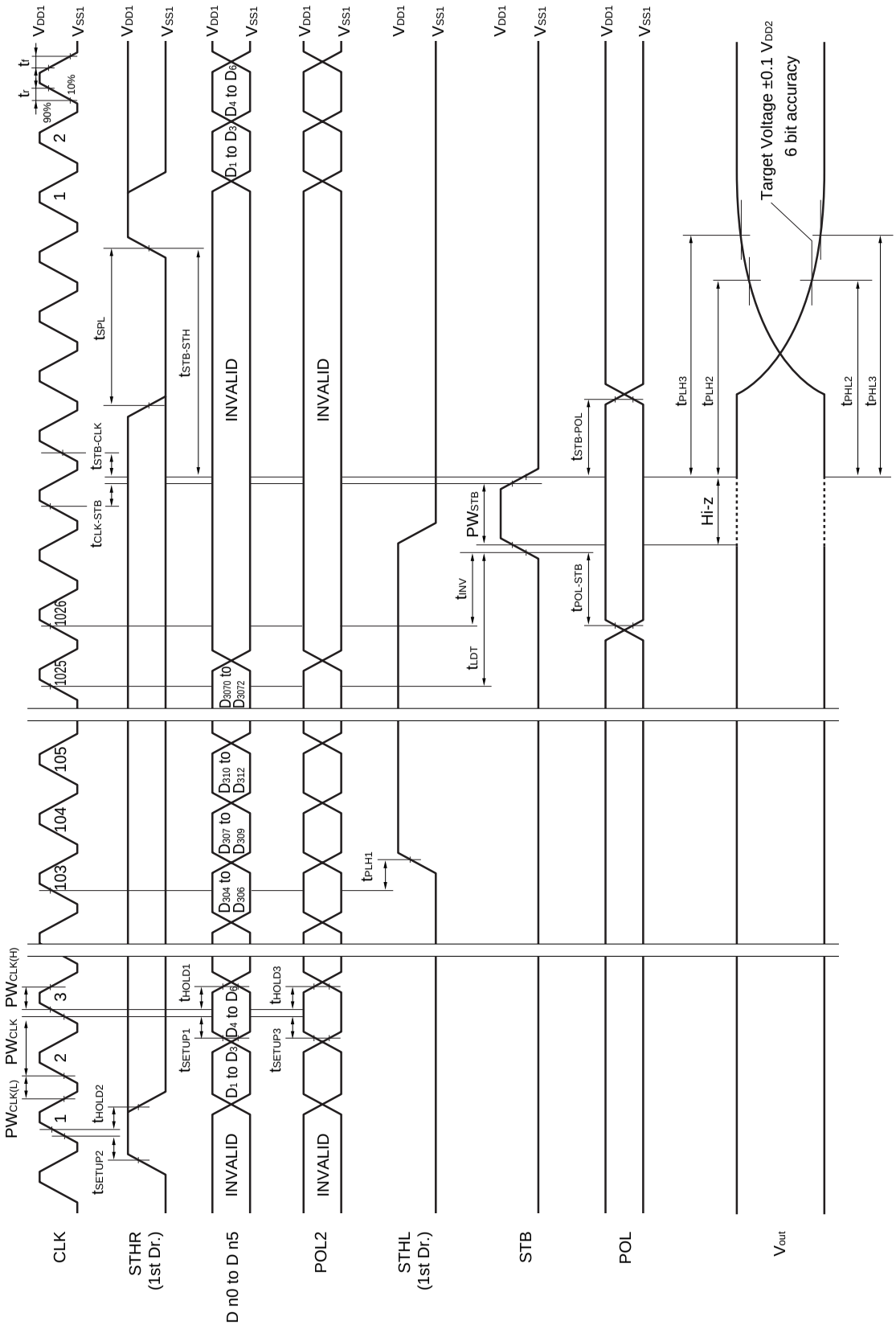
Conditions Required for Timing

(T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 4.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Pulse High Period	$PW_{CLK(H)}$		6			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		6			ns
Data Setup Time	t_{SETUP1}		6			ns
Data Hold Time	t_{HOLD1}		6			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		6			ns
POL2 Setup Time	t_{SETUP3}		6			ns
POL2 Hold Time	t_{HOLD3}		6			ns
Start Pulse Low Period	t_{SPL}		6			ns
STB Pulse Width	PW_{STB}		1			μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↓	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↓ → CLK ↑	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↓ → STHR (STHL) ↑	60			ns
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

12. SWITCHING CHARACTERISTICS WAVEFORM

Unless otherwise specified, V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



13. RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Mounting Condition	Mounting Method	Condition
Thermocompression bonding	Soldering	Heating tool 300 to 350 °C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF[Note] (Sheet-shape bonding agent)	Temporary bonding 70 to 100 °C; pressure 3 to 8 kg/cm^2; time 3 to 5 secs. Real bonding 165 to 180 °C; pressure 25 to 45 kg/cm^2; time 30 to 40 secs. (when using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Note To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company.

Caution Be sure to avoid using two or more packaging methods at a time.

REFERENCE

NEC Semiconductor Device Reliability/Quality Control System (C10983E)
Quality Grades on NEC Semiconductor Devices (C11531E)

[MEMO]

[MEMO]

[MEMO]

[MEMO]