NEC

MOS INTEGRATED CIRCUIT

μPD16717

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD16717 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.2 V to V_{DD2} – 0.2 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 55 MHz when driving at 2.5 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels.

FEATURES

- CMOS level input (2.5 to 3.6 V)
- 384 outputs
- Input of 6 bits (gray-scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- Logic power supply voltage (V_{DD1}): 2.5 to 3.6 V
- Driver power supply voltage (V_{DD2}): 8.5 V ± 0.5 V
- High-speed data transfer: f_{CLK} = 55 MHz (internal data transfer speed when operating at V_{DD1} = 2.5 V)
- Output dynamic range: V_{SS2} + 0.2 V to V_{DD2} – 0.2 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Input data inversion function (POL2)
- Through rate control inversion function (SRC)
- ★ • Output reset control inversion function (MODE)
- Slim chip

ORDERING INFORMATION

Part Number	Package
μPD16717N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

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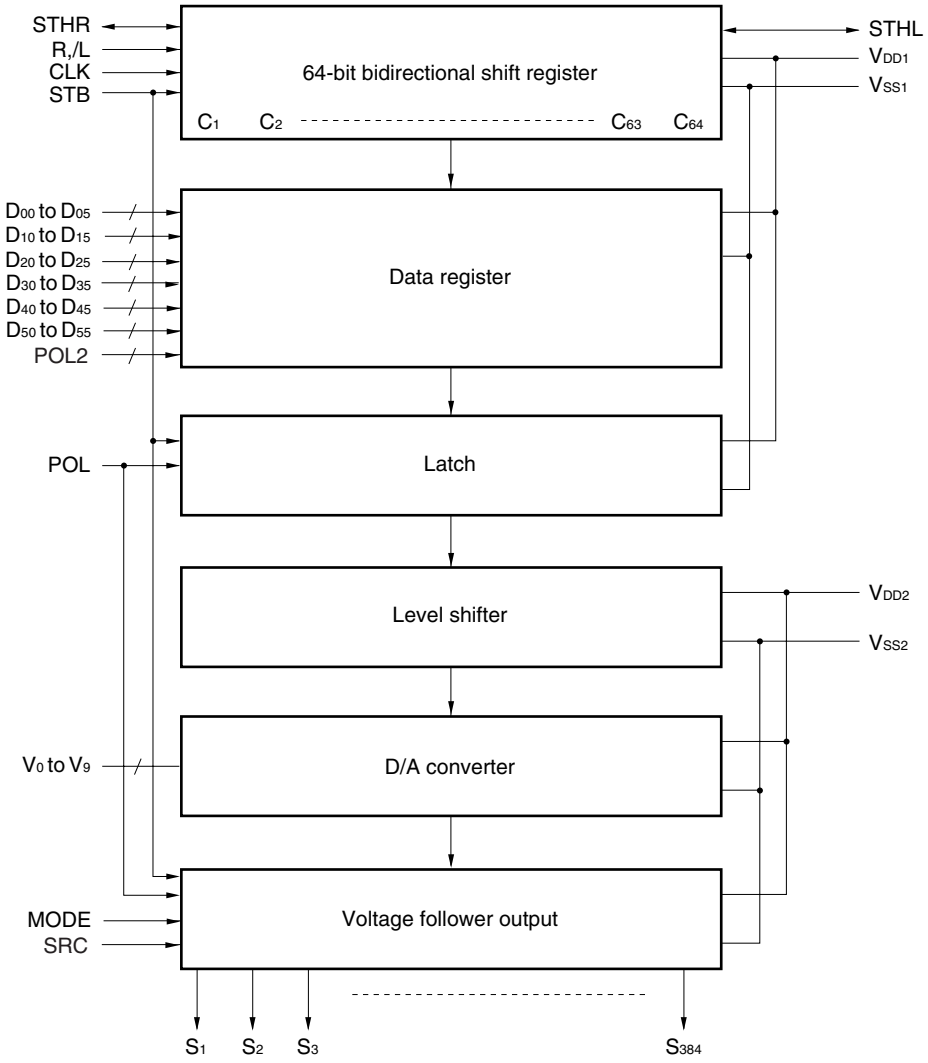
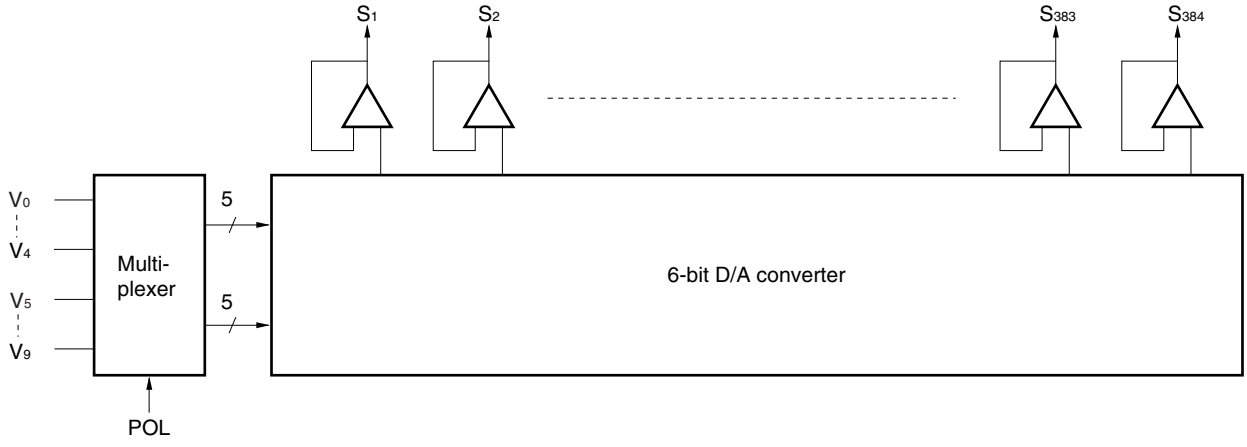
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM

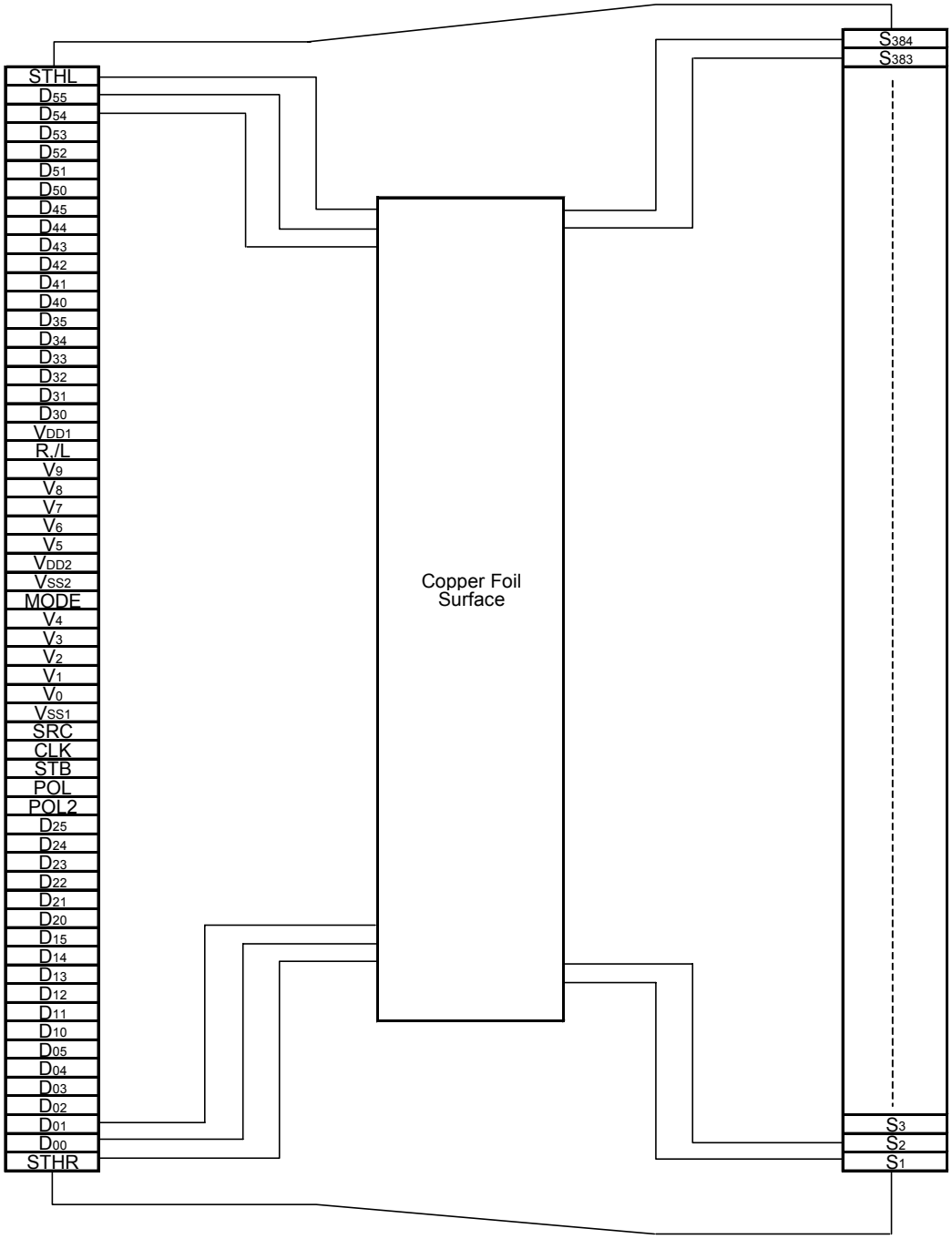


Remark /xxx indicates active low signal.

★ 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16717) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

★ 4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{384}	Driver	Output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25} D_{30} to D_{35} D_{40} to D_{45} D_{50} to D_{55}	Display data	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
R,/L	Shift direction control	Input	These refer to the shift direction control input pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR (input), $S_1 \rightarrow S_{384}$, STHL (output) R,/L = L (left shift) : STHL (input), $S_{384} \rightarrow S_1$, STHR (output)
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output A high level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more than 2CLK, the first 1CLK of the high-level input is valid.
STHL	Left shift start pulse	I/O	
CLK	Shift clock	Input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 66th clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge. This pin should not stop during blanking period.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. Output timing of gray scale voltage is changed by setting MODE. MODE = H or open: STB at the falling edge, the gray scale voltage is supplied to the driver. MODE = L: After set to STB = H, the gray scale voltage is supplied by the rising edge behind 3 clocks. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	Input	POL = L: The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
POL2	Data inversion	Input	Data inversion can invert when display data is loaded. POL2 = H: Data inversion inverts display data inside IC. POL2 = L: Data inversion does not invert input data. When in STB = H, it becomes test mode if POL2 is changed, throughout STB = H period should not carry out the change of POL2.

(2/2)

Pin Symbol	Pin Name	I/O	Description
MODE	Output reset control	Input	MODE = H or open: Output reset. STB at the falling edge, the gray scale voltage is supplied to the driver. MODE = L: Non-output reset. After set to STB = H, the gray scale voltage is supplied by the rising edge behind 3 clocks. This pin is pulled up to the V_{DD2} power supply inside the IC.
SRC	High driving time control	Input	This pin is set up to high drive time by the multiple of STB width. SRC = H or open: High drive time is twice the STB width. SRC = L: High drive time is three times the STB width. Refer to **9. SRC PIN AND HIGH DRIVING TIME** This pin is pulled up to the V_{DD1} power supply inside the IC.
V_0 to V_9	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$ $0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.2\ V$
V_{DD1}	Logic power supply	–	2.5 to 3.6 V
V_{DD2}	Driver power supply	–	8.5 V ± 0.5 V
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.).

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also recommended between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_9) and V_{SS}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD16717 incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0" to V_{63}" is almost equivalent. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of

$V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$

$0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.2\ V$

Figures 5–2 and 5–3 indicate the relationship between the input data and output voltage and the resistance values of the resistor string.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

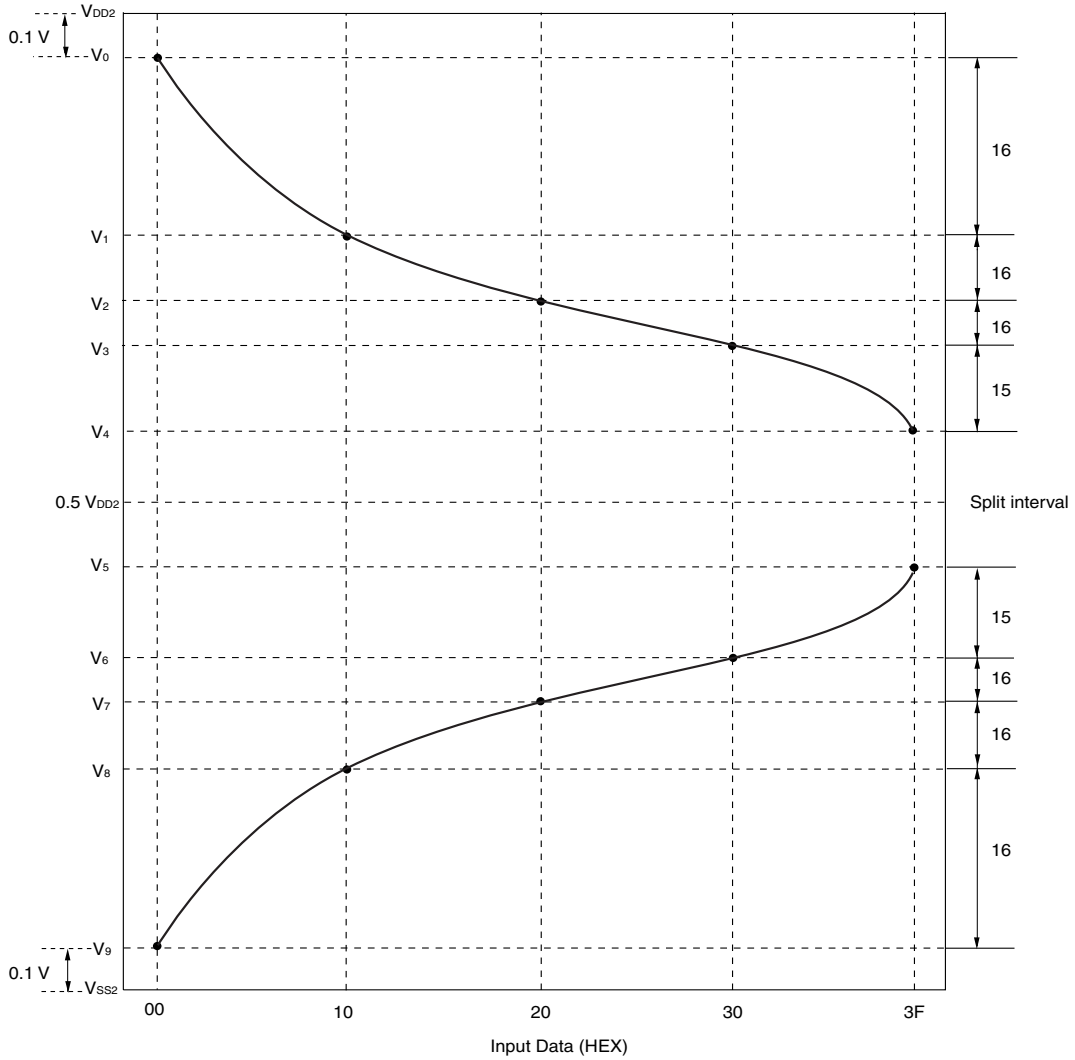
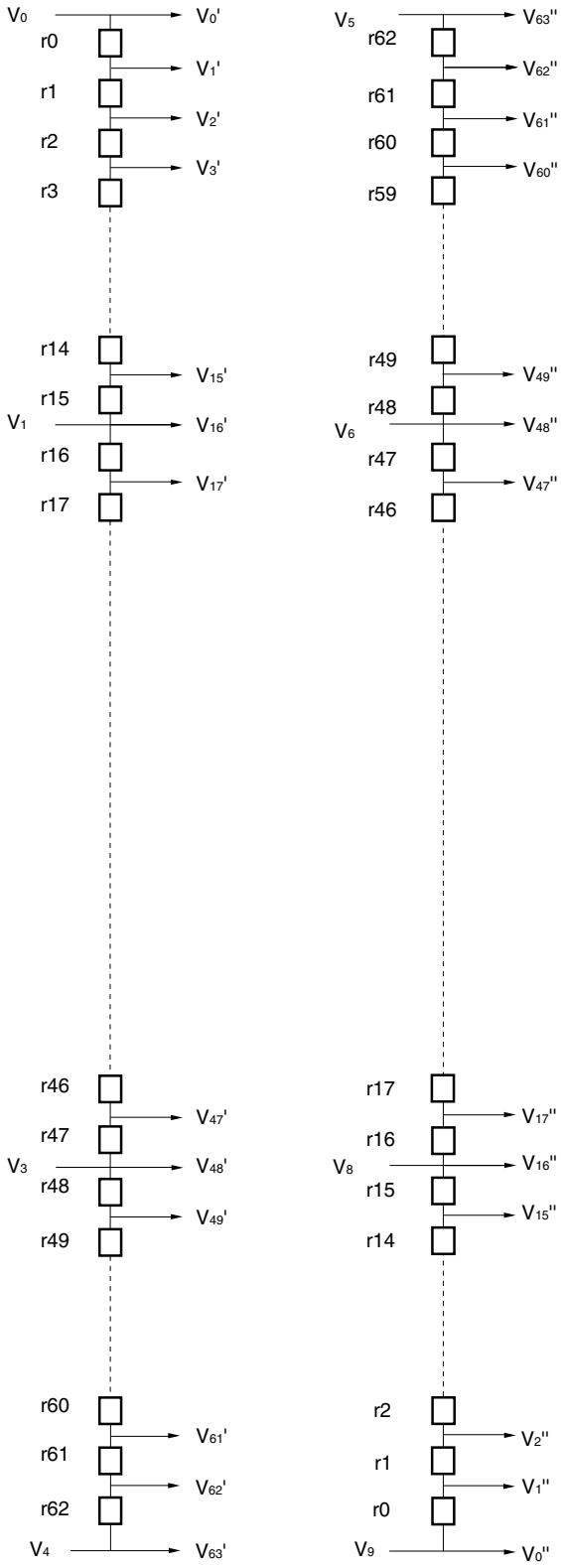


Figure 5–2. γ-corrected Voltages and Ladder Resistors Ratio



rn	Ratio
r0	6.2
r1	5.8
r2	5.4
r3	5.1
r4	4.7
r5	4.3
r6	4.3
r7	3.9
r8	3.9
r9	3.1
r10	3.1
r11	2.7
r12	2.7
r13	2.7
r14	2.3
r15	2.3
r16	2.0
r17	1.8
r18	1.8
r19	1.7
r20	1.6
r21	1.5
r22	1.5
r23	1.4
r24	1.3
r25	1.3
r26	1.2
r27	1.2
r28	1.1
r29	1.1
r30	1.0
r31	1.0
r32	1.0
r33	1.0
r34	1.0
r35	1.0
r36	1.0
r37	1.0
r38	1.0
r39	1.0
r40	1.0
r41	1.0
r42	1.0
r43	1.0
r44	1.0
r45	1.0
r46	1.0
r47	1.0
r48	1.1
r49	1.1
r50	1.1
r51	1.1
r52	1.1
r53	1.6
r54	1.6
r55	1.6
r56	1.6
r57	1.6
r58	2.1
r59	2.7
r60	3.4
r61	5.2
r62	11.2

Caution There is no connection between V_4 and V_5 terminal in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (POL2 = L)

(Output Voltage 1) V_{DD2} – 0.2 V ≥ V_5 > V_6 > V_7 > V_8 > V_9 ≥ 0.5 V_{DD2}

(Output Voltage 2) 0.5 V_{DD2} ≥ V_5 > V_6 > V_7 > V_8 > V_9 ≥ V_{SS2} + 0.2 V

Input Data	Output Voltage1					Output Voltage2				
00H	$V_{0'}$	V_0				$V_{0''}$	V_9			
01H	$V_{1'}$	$V_1+(V_0-V_1)\times$	56.4	/	62.6	$V_{1''}$	$V_9+(V_8-V_9)\times$	6.2	/	62.6
02H	$V_{2'}$	$V_1+(V_0-V_1)\times$	50.6	/	62.6	$V_{2''}$	$V_9+(V_8-V_9)\times$	12.1	/	62.6
03H	$V_{3'}$	$V_1+(V_0-V_1)\times$	45.1	/	62.6	$V_{3''}$	$V_9+(V_8-V_9)\times$	17.5	/	62.6
04H	$V_{4'}$	$V_1+(V_0-V_1)\times$	40.1	/	62.6	$V_{4''}$	$V_9+(V_8-V_9)\times$	22.6	/	62.6
05H	$V_{5'}$	$V_1+(V_0-V_1)\times$	35.4	/	62.6	$V_{5''}$	$V_9+(V_8-V_9)\times$	27.2	/	62.6
06H	$V_{6'}$	$V_1+(V_0-V_1)\times$	31.1	/	62.6	$V_{6''}$	$V_9+(V_8-V_9)\times$	31.5	/	62.6
07H	$V_{7'}$	$V_1+(V_0-V_1)\times$	26.8	/	62.6	$V_{7''}$	$V_9+(V_8-V_9)\times$	35.8	/	62.6
08H	$V_{8'}$	$V_1+(V_0-V_1)\times$	22.9	/	62.6	$V_{8''}$	$V_9+(V_8-V_9)\times$	39.7	/	62.6
09H	$V_{9'}$	$V_1+(V_0-V_1)\times$	19.1	/	62.6	$V_{9''}$	$V_9+(V_8-V_9)\times$	43.6	/	62.6
0AH	$V_{10'}$	$V_1+(V_0-V_1)\times$	15.9	/	62.6	$V_{10''}$	$V_9+(V_8-V_9)\times$	46.7	/	62.6
0BH	$V_{11'}$	$V_1+(V_0-V_1)\times$	12.8	/	62.6	$V_{11''}$	$V_9+(V_8-V_9)\times$	49.8	/	62.6
0CH	$V_{12'}$	$V_1+(V_0-V_1)\times$	10.1	/	62.6	$V_{12''}$	$V_9+(V_8-V_9)\times$	52.5	/	62.6
0DH	$V_{13'}$	$V_1+(V_0-V_1)\times$	7.4	/	62.6	$V_{13''}$	$V_9+(V_8-V_9)\times$	55.2	/	62.6
0EH	$V_{14'}$	$V_1+(V_0-V_1)\times$	4.7	/	62.6	$V_{14''}$	$V_9+(V_8-V_9)\times$	57.9	/	62.6
0FH	$V_{15'}$	$V_1+(V_0-V_1)\times$	2.3	/	62.6	$V_{15''}$	$V_9+(V_8-V_9)\times$	60.3	/	62.6
10H	$V_{16'}$	V_1				$V_{16''}$	V_8			
11H	$V_{17'}$	$V_2+(V_1-V_2)\times$	20.7	/	22.6	$V_{17''}$	$V_8+(V_7-V_8)\times$	2.0	/	22.6
12H	$V_{18'}$	$V_2+(V_1-V_2)\times$	18.8	/	22.6	$V_{18''}$	$V_8+(V_7-V_8)\times$	3.8	/	22.6
13H	$V_{19'}$	$V_2+(V_1-V_2)\times$	17.0	/	22.6	$V_{19''}$	$V_8+(V_7-V_8)\times$	5.7	/	22.6
14H	$V_{20'}$	$V_2+(V_1-V_2)\times$	15.3	/	22.6	$V_{20''}$	$V_8+(V_7-V_8)\times$	7.4	/	22.6
15H	$V_{21'}$	$V_2+(V_1-V_2)\times$	13.7	/	22.6	$V_{21''}$	$V_8+(V_7-V_8)\times$	9.0	/	22.6
16H	$V_{22'}$	$V_2+(V_1-V_2)\times$	12.1	/	22.6	$V_{22''}$	$V_8+(V_7-V_8)\times$	10.5	/	22.6
17H	$V_{23'}$	$V_2+(V_1-V_2)\times$	10.7	/	22.6	$V_{23''}$	$V_8+(V_7-V_8)\times$	12.0	/	22.6
18H	$V_{24'}$	$V_2+(V_1-V_2)\times$	9.3	/	22.6	$V_{24''}$	$V_8+(V_7-V_8)\times$	13.4	/	22.6
19H	$V_{25'}$	$V_2+(V_1-V_2)\times$	7.9	/	22.6	$V_{25''}$	$V_8+(V_7-V_8)\times$	14.7	/	22.6
1AH	$V_{26'}$	$V_2+(V_1-V_2)\times$	6.7	/	22.6	$V_{26''}$	$V_8+(V_7-V_8)\times$	16.0	/	22.6
1BH	$V_{27'}$	$V_2+(V_1-V_2)\times$	5.4	/	22.6	$V_{27''}$	$V_8+(V_7-V_8)\times$	17.2	/	22.6
1CH	$V_{28'}$	$V_2+(V_1-V_2)\times$	4.2	/	22.6	$V_{28''}$	$V_8+(V_7-V_8)\times$	18.4	/	22.6
1DH	$V_{29'}$	$V_2+(V_1-V_2)\times$	3.1	/	22.6	$V_{29''}$	$V_8+(V_7-V_8)\times$	19.5	/	22.6
1EH	$V_{30'}$	$V_2+(V_1-V_2)\times$	2.0	/	22.6	$V_{30''}$	$V_8+(V_7-V_8)\times$	20.6	/	22.6
1FH	$V_{31'}$	$V_2+(V_1-V_2)\times$	1.0	/	22.6	$V_{31''}$	$V_8+(V_7-V_8)\times$	21.6	/	22.6
20H	$V_{32'}$	V_2				$V_{32''}$	V_7			
21H	$V_{33'}$	$V_3+(V_2-V_3)\times$	15.0	/	16.0	$V_{33''}$	$V_7+(V_6-V_7)\times$	1.0	/	16.0
22H	$V_{34'}$	$V_3+(V_2-V_3)\times$	14.0	/	16.0	$V_{34''}$	$V_7+(V_6-V_7)\times$	2.0	/	16.0
23H	$V_{35'}$	$V_3+(V_2-V_3)\times$	13.0	/	16.0	$V_{35''}$	$V_7+(V_6-V_7)\times$	3.0	/	16.0
24H	$V_{36'}$	$V_3+(V_2-V_3)\times$	12.0	/	16.0	$V_{36''}$	$V_7+(V_6-V_7)\times$	4.0	/	16.0
25H	$V_{37'}$	$V_3+(V_2-V_3)\times$	11.0	/	16.0	$V_{37''}$	$V_7+(V_6-V_7)\times$	5.0	/	16.0
26H	$V_{38'}$	$V_3+(V_2-V_3)\times$	10.0	/	16.0	$V_{38''}$	$V_7+(V_6-V_7)\times$	6.0	/	16.0
27H	$V_{39'}$	$V_3+(V_2-V_3)\times$	9.0	/	16.0	$V_{39''}$	$V_7+(V_6-V_7)\times$	7.0	/	16.0
28H	$V_{40'}$	$V_3+(V_2-V_3)\times$	8.0	/	16.0	$V_{40''}$	$V_7+(V_6-V_7)\times$	8.0	/	16.0
29H	$V_{41'}$	$V_3+(V_2-V_3)\times$	7.0	/	16.0	$V_{41''}$	$V_7+(V_6-V_7)\times$	9.0	/	16.0
2AH	$V_{42'}$	$V_3+(V_2-V_3)\times$	6.0	/	16.0	$V_{42''}$	$V_7+(V_6-V_7)\times$	10.0	/	16.0
2BH	$V_{43'}$	$V_3+(V_2-V_3)\times$	5.0	/	16.0	$V_{43''}$	$V_7+(V_6-V_7)\times$	11.0	/	16.0
2CH	$V_{44'}$	$V_3+(V_2-V_3)\times$	4.0	/	16.0	$V_{44''}$	$V_7+(V_6-V_7)\times$	12.0	/	16.0
2DH	$V_{45'}$	$V_3+(V_2-V_3)\times$	3.0	/	16.0	$V_{45''}$	$V_7+(V_6-V_7)\times$	13.0	/	16.0
2EH	$V_{46'}$	$V_3+(V_2-V_3)\times$	2.0	/	16.0	$V_{46''}$	$V_7+(V_6-V_7)\times$	14.0	/	16.0
2FH	$V_{47'}$	$V_3+(V_2-V_3)\times$	1.0	/	16.0	$V_{47''}$	$V_7+(V_6-V_7)\times$	15.0	/	16.0
30H	$V_{48'}$	V_3				$V_{48''}$	V_6			
31H	$V_{49'}$	$V_4+(V_3-V_4)\times$	36.7	/	37.8	$V_{49''}$	$V_6+(V_5-V_6)\times$	1.1	/	37.8
32H	$V_{50'}$	$V_4+(V_3-V_4)\times$	35.7	/	37.8	$V_{50''}$	$V_6+(V_5-V_6)\times$	2.1	/	37.8
33H	$V_{51'}$	$V_4+(V_3-V_4)\times$	34.6	/	37.8	$V_{51''}$	$V_6+(V_5-V_6)\times$	3.2	/	37.8
34H	$V_{52'}$	$V_4+(V_3-V_4)\times$	33.5	/	37.8	$V_{52''}$	$V_6+(V_5-V_6)\times$	4.2	/	37.8
35H	$V_{53'}$	$V_4+(V_3-V_4)\times$	32.5	/	37.8	$V_{53''}$	$V_6+(V_5-V_6)\times$	5.3	/	37.8
36H	$V_{54'}$	$V_4+(V_3-V_4)\times$	30.9	/	37.8	$V_{54''}$	$V_6+(V_5-V_6)\times$	6.9	/	37.8
37H	$V_{55'}$	$V_4+(V_3-V_4)\times$	29.3	/	37.8	$V_{55''}$	$V_6+(V_5-V_6)\times$	8.5	/	37.8
38H	$V_{56'}$	$V_4+(V_3-V_4)\times$	27.7	/	37.8	$V_{56''}$	$V_6+(V_5-V_6)\times$	10.1	/	37.8
39H	$V_{57'}$	$V_4+(V_3-V_4)\times$	26.1	/	37.8	$V_{57''}$	$V_6+(V_5-V_6)\times$	11.7	/	37.8
3AH	$V_{58'}$	$V_4+(V_3-V_4)\times$	24.5	/	37.8	$V_{58''}$	$V_6+(V_5-V_6)\times$	13.3	/	37.8
3BH	$V_{59'}$	$V_4+(V_3-V_4)\times$	22.4	/	37.8	$V_{59''}$	$V_6+(V_5-V_6)\times$	15.4	/	37.8
3CH	$V_{60'}$	$V_4+(V_3-V_4)\times$	19.7	/	37.8	$V_{60''}$	$V_6+(V_5-V_6)\times$	18.1	/	37.8
3DH	$V_{61'}$	$V_4+(V_3-V_4)\times$	16.4	/	37.8	$V_{61''}$	$V_6+(V_5-V_6)\times$	21.4	/	37.8
3EH	$V_{62'}$	$V_4+(V_3-V_4)\times$	11.2	/	37.8	$V_{62''}$	$V_6+(V_5-V_6)\times$	26.6	/	37.8
3FH	$V_{63'}$	V_4				$V_{63''}$	V_5			

Caution There is no connection between V_4 and V_5 terminal in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	...	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	...	D_{40} to D_{45}	D_{50} to D_{55}

(2) R,/L = L (Left shift)

Output	S_1	S_2	S3	S4	...	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	...	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} **Note**	S_{2n} **Note**
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM (MODE =L)

This chapter indicates relationship between STB, CLK, and output waveform in the μPD16717.

In figure 7–2, STB = H is taken in by the rising edge of CLK [1]. However, when not satisfying the standard of $t_{STB-CLK}$, STB = H is taken in by the rising edge of the next CLK [1']. The latch of display data is completed by the falling edge of the next CLK which took in STB = H.

Moreover, synchronizing with the rising edge of the next CLK, driver output is started after the completion of a display data latch.

Therefore, in order to output the gray scale voltage, it is at least 3 clock necessity.

Figure 7–1. Output Circuit Block Diagram

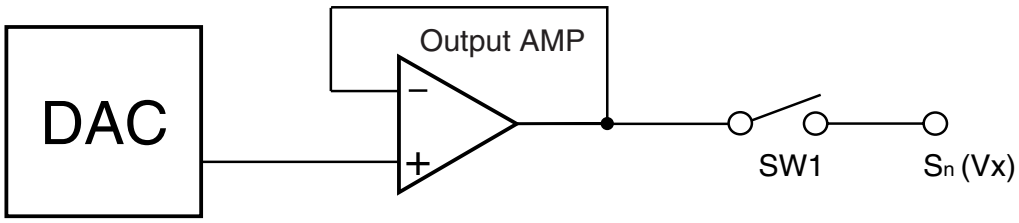
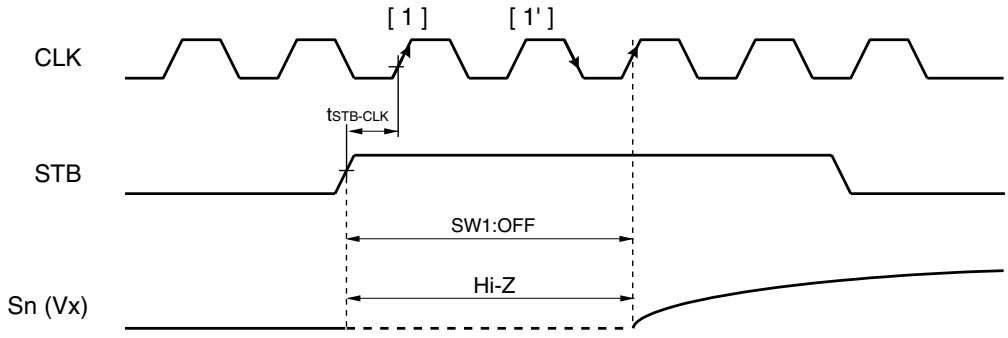


Figure 7–2. Output Circuit Block Diagram



8. RELATIONSHIP BETWEEN MODE, STB, POL AND OUTPUT WAVEFORM

MODE = H or open:

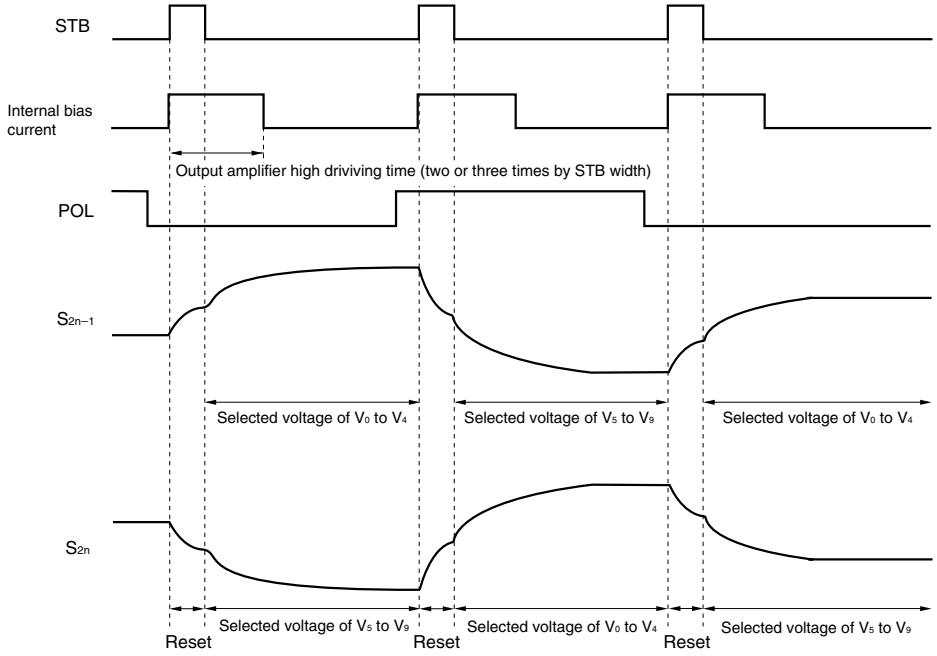
A total output serves as RESET (short circuit), and throughout STB = H outputs gray scale voltage to the LCD panel synchronizing with the falling edge of STB.

MODE = L:

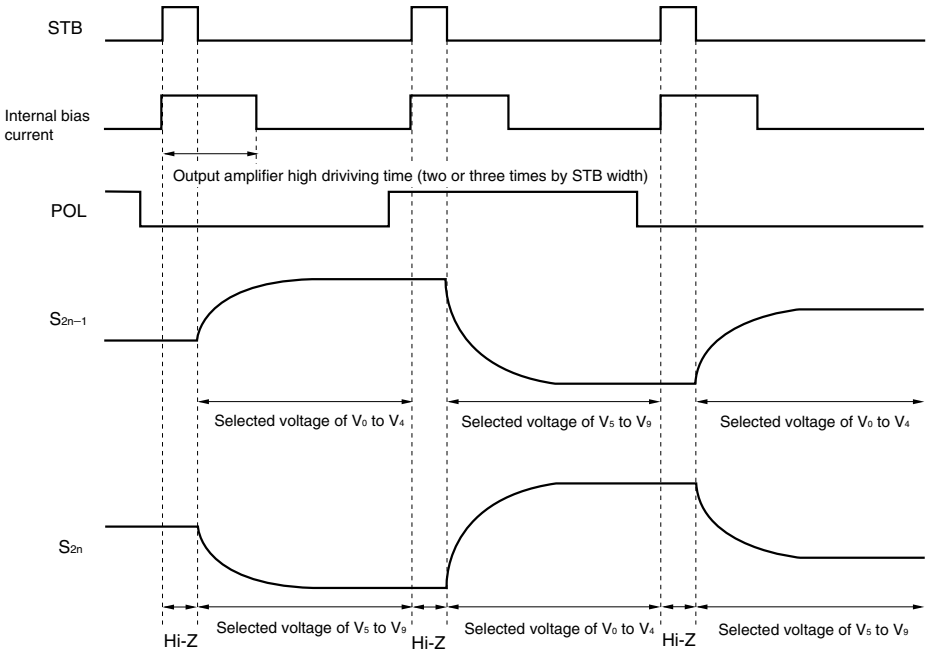
This is set to STB = H and a 2 clock cycle all output outputs gray scale voltage to the LCD panel after Hi-Z.

Refer to **7. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM (MODE = L).**

★ **Figure 8–1. MODE = H or open**



★ **Figure 8–2. MODE = L**



9. SRC PIN AND HIGH DRIVING TIME

The μPD16717 has a current consumption of selection or driver IC simple substance is the high drive time of output amplifier controllable by the logic of SRC pin.

SRC = H or open: High drive time is twice the STB width.
SRC = L: High drive time is three times the STB width.

High drive time at counting the clock has decided in STB period, and the relationship is as follows.
The high drive time of table is the number of clocks from STB falling.

Table 9–1. Relationship between Number of Clocks in STB Period and High Drive Time

CLK in STB period	High driving time	
	SRC = H or open (unit: CLK)	SRC = L (unit: CLK)
Under 7CLK	8	16
8 to 15CLK	16	32
16 to 23CLK	24	48
24 to 31CLK	32	64
32 to 39CLK	40	80
40 to 47CLK	48	96
48 to 55CLK	56	112
56 to 63CLK	64	128
64 to 71CLK	72	144
72 to 79CLK	80	160
80 to 87CLK	88	176
88 to 95CLK	96	192
96 to 103CLK	104	208
104 to 111CLK	112	224
112CLK or up	Prohibited	

In consideration of the characteristic of the LCD panel, after the system estimates sufficient, please decide on the high driving time of output amplifier.

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.5		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_4		0.5 V_{DD2}		V_{DD2} – 0.2	V
	V_5 to V_9		0.2		0.5 V_{DD2}	V
Driver Part Output Voltage	V_O		V_{SS2} + 0.2		V_{DD2} – 0.2	V
Clock Frequency	f_{CLK}				55	MHz

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 8.5 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}	Exclude MODE, SRC			±1.0	μA
★		MODE, SRC			T.B.D.	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA	V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA			0.1	V
γ-Corrected Resistance	R_γ	V_0 to V_4 = V_5 to V_9 = 4.0 V	9.8	13.8	23.0	kΩ
Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V Note			–300	μA
	I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V Note	300			μA
Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 8.5 V, V_{OUT} = 2.0 V, 4.25 V, 6.5 V, T_A = 25°C		±7	±20	mV
Output Swing Difference Deviation	ΔV_{P-P}			±2	±30	mV
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}		3.2	6.0	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2}, with no load		4.6	7.0	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{384}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. f_{STB} = 65 kHz, f_{CLK} = 54 MHz

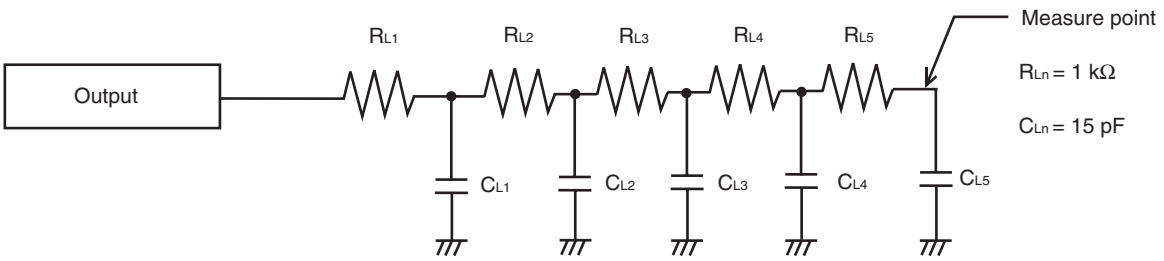
2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (10 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 8.5 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF, V_{DD1} = 2.5 to 3.6 V		10	17	ns
		C_L = 15 pF, V_{DD1} = 3.0 to 3.6 V		8	10.5	ns
Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ			(2.5)	μs
	t_{PLH3}				(4)	μs
	t_{PHL2}				(2.5)	μs
	t_{PHL3}				(4)	μs
Input Capacitance	C_{I1}	Exclude STHR (STHL), T_A = 25°C			10	pF
	C_{I2}	STHR (STHL), T_A = 25°C			15	pF

★ **<Measurement Condition>**



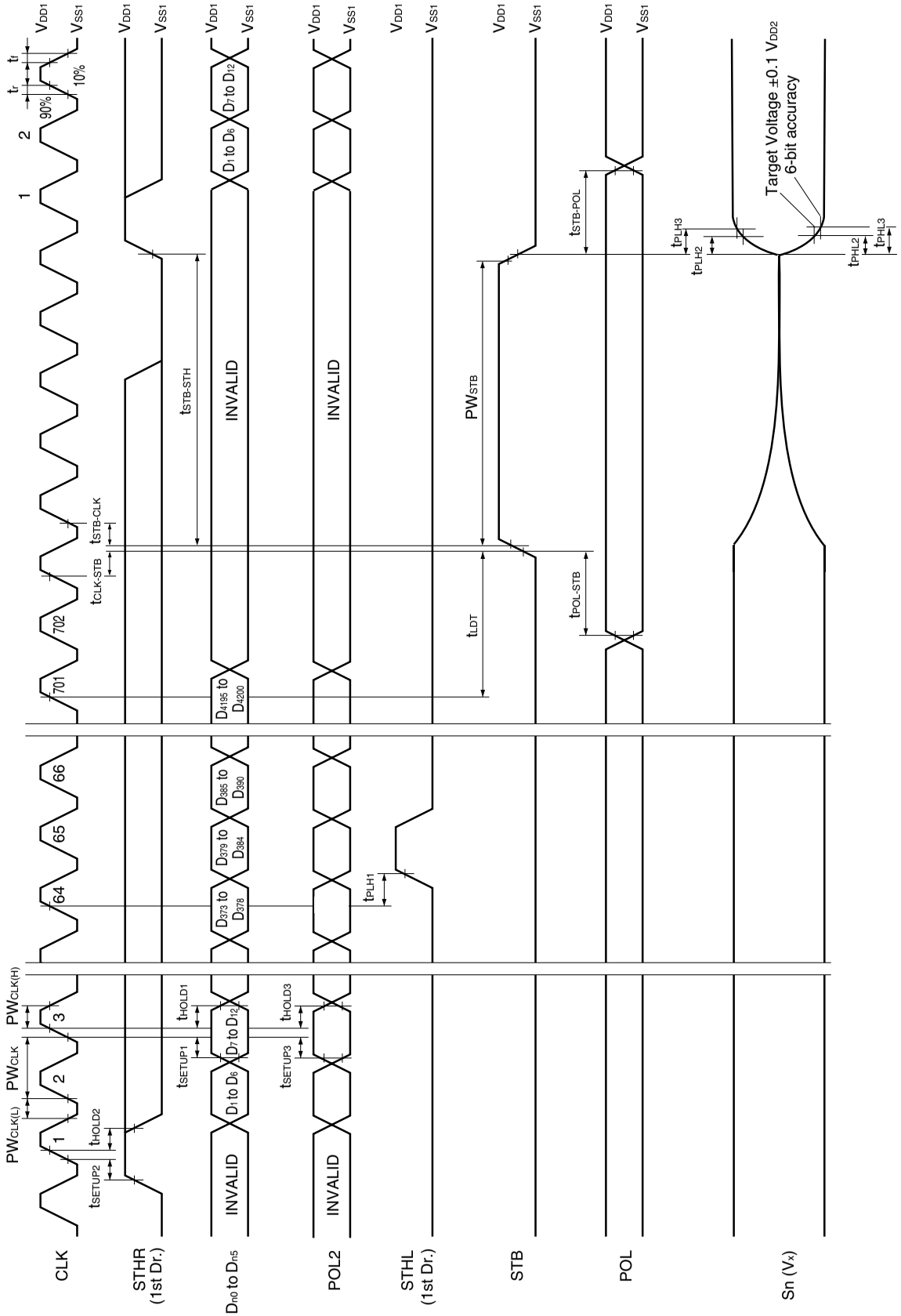
Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.6 V, V_{SS1} = 0 V, $t_r = t_f$ = 5.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		18			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$	2.5 V ≤ V_{DD1} < 3.0 V	6			ns
		3.0 V ≤ V_{DD1} ≤ 3.6 V	4			ns
Data Setup Time	t_{SETUP1}		2			ns
Data Hold Time	t_{HOLD1}		2			ns
Start Pulse Setup Time	t_{SETUP2}		2			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
POL21/22 Setup Time	t_{SETUP3}		2			ns
POL21/22 Hold Time	t_{HOLD3}		2			ns
STB Pulse Width	PW_{STB}		3		111	CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	9			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

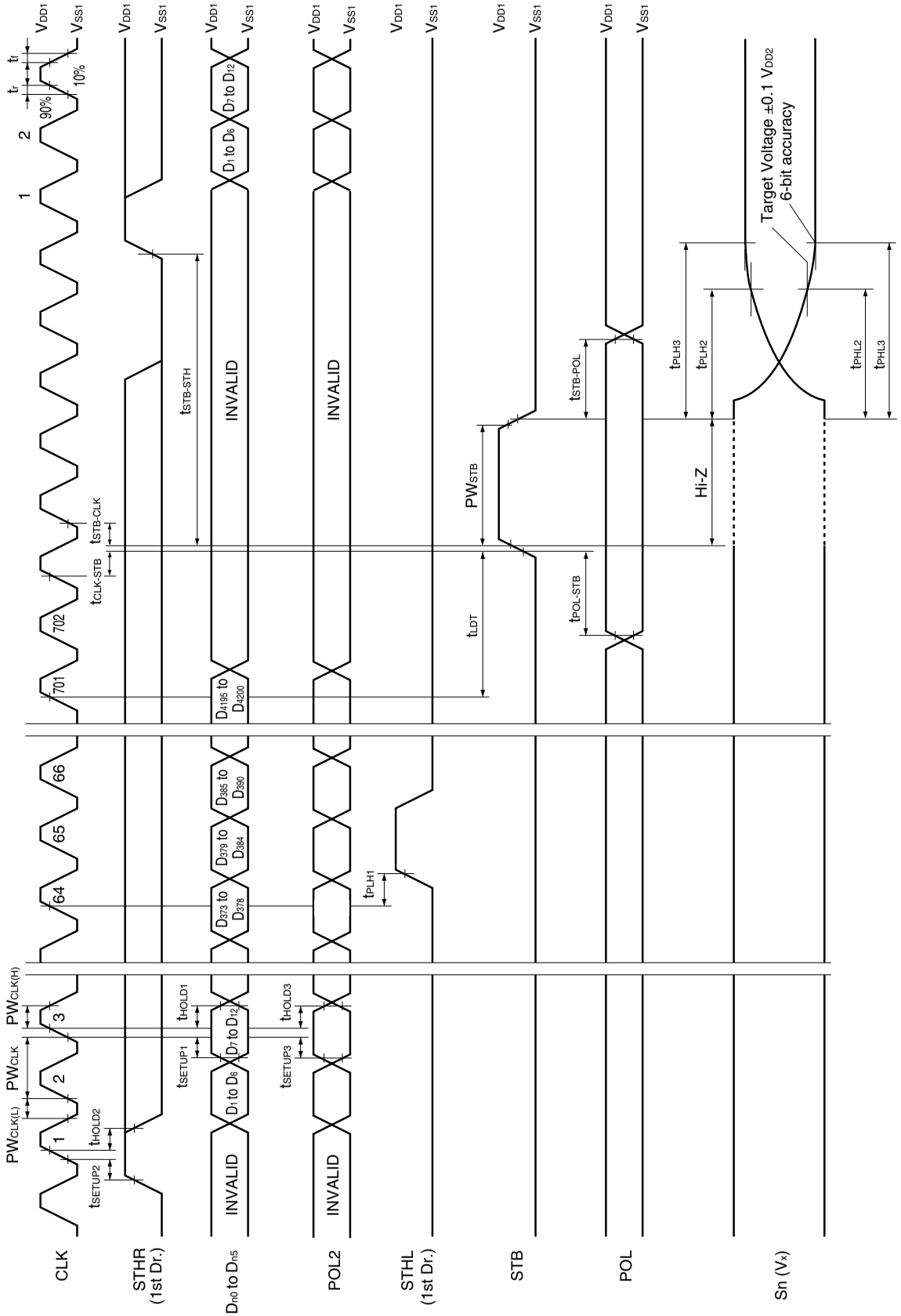
Switching Characteristic Waveform (R,/L= H, MODE = H or open)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



★ **Switching Characteristic Waveform(R,/L= H, MODE =L)**

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



★ 11. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16717.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16717N-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm^2: time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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