

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

DESCRIPTION

The μ PD16721 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ -corrected by an internal D/A converter and 8-by-2 external power modules.

Because the output dynamic range is as large as $V_{SS2} + 0.2$ V to $V_{DD2} - 0.2$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. The maximum clock frequency is 70 MHz when driving at 3.0 V.

FEATURES

- CMOS level input
- 384 outputs
- Input of 8 bits (gray scale data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- ★ • Logic power supply voltage (V_{DD1}): 2.5 to 3.4 V
- ★ • Driver power supply voltage (V_{DD2}): 13.0 \pm 0.5 V or 15.0 \pm 0.5 V (switchable, V_{SEL})
- ★ • High-speed data transfer: $f_{CLK} = 70$ MHz MAX. (internal data transfer speed when operating at $V_{DD1} = 3.0$ V)
= 55 MHz MAX. (internal data transfer speed when operating at $V_{DD1} = 2.5$ V)
- Output dynamic range: $V_{SS2} + 0.2$ V to $V_{DD2} - 0.2$ V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Output inversion function (POL21/22)
- ★ • Output reset control is possible (MODE)
- ★ • Slew-rate control is possible (SRC)
- ★ • Output resistance control is possible (ORC)
- Single bank arrangement is possible (Loaded with slim TCP)

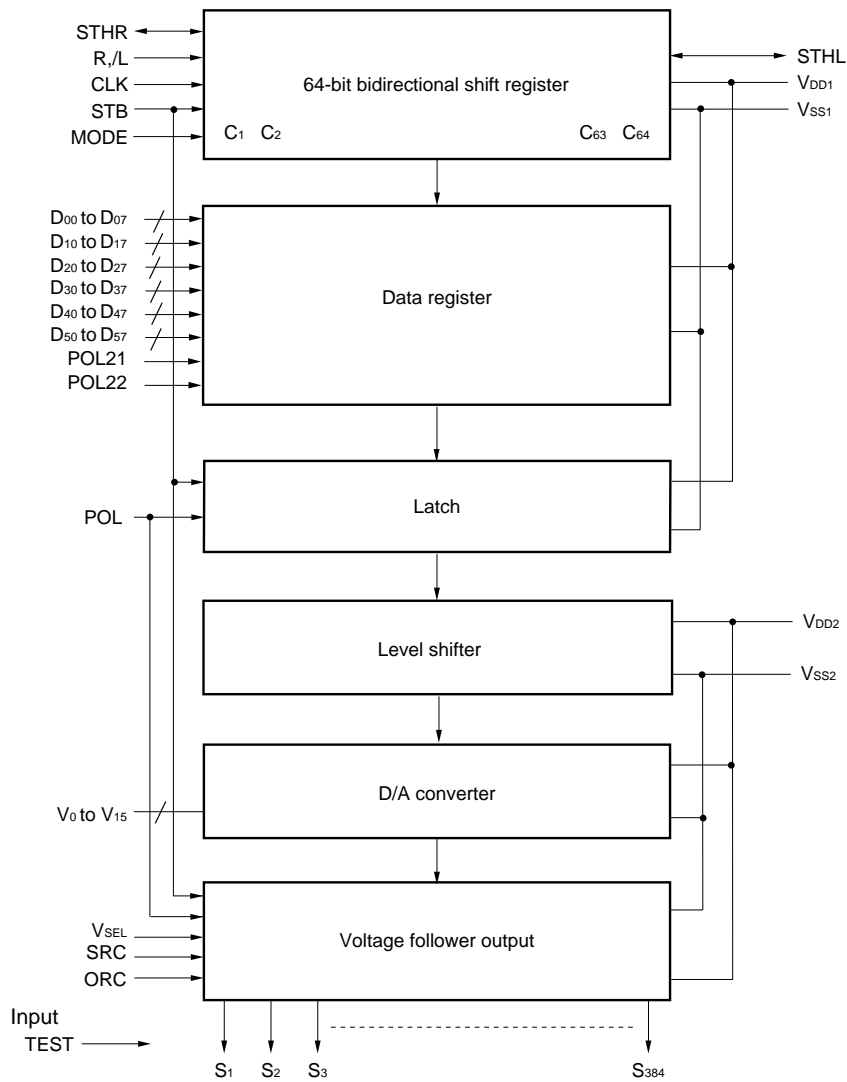
ORDERING INFORMATION

Part Number	Package
μ PD16721N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

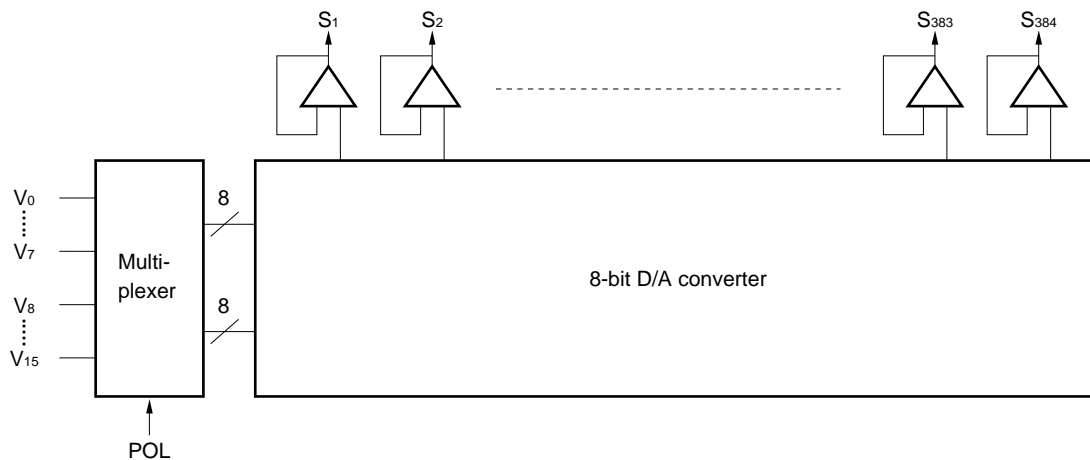
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★ 1. BLOCK DIAGRAM

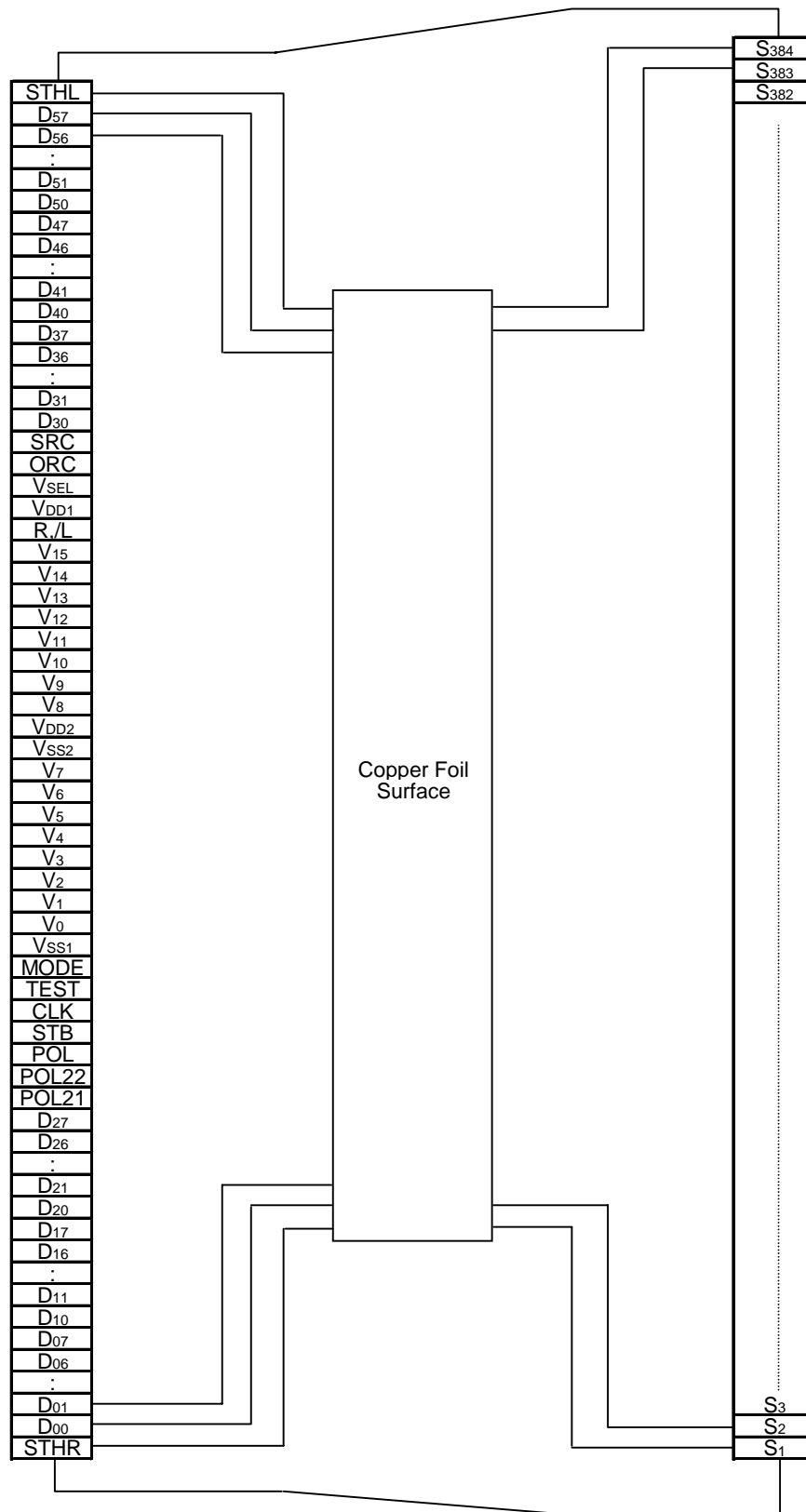


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16721N-xxx) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S ₁ to S ₃₈₄	Driver	O	The D/A converted 256-gray-scale analog voltage is output.
D ₀₀ to D ₀₇	Port 1 display data	I	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D _{x0} : LSB, D _{x7} : MSB
D ₁₀ to D ₁₇			
D ₂₀ to D ₂₇			
D ₃₀ to D ₃₇			
D ₄₀ to D ₄₇	Port 2 display data	I	
D ₅₀ to D ₅₇			
R _/ L	Shift direction control	I	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R _/ L = H (right shift): STHR input, S ₁ →S ₃₈₄ , STHL output R _/ L = L (left shift) : STHL input, S ₃₈₄ →S ₁ , STHR output
STHR	Right shift start pulse	I/O	This is the start pulse input/output pin when connected in cascade. Loading of display data starts when a high level is read at the rising edge of CLK. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STHL	Left shift start pulse	I/O	For right shift, STHR is input and STHL is output. For left shift, STHL is input and STHR is output.
CLK	Shift clock	I	The shift clock input pin of shift register. The display data is loaded into the data register at the rising edge. If 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	I	The contents of the data register are transferred to the latch circuit at the rising edge. In addition, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
SRC	Slew-rate control	I	SRC = H: High-slew-rate mode (large current consumption) SRC = L: Low-slew-rate mode (small current consumption) SRC is pulled up to the V _{DD1} in the LSI.
ORC	Output resistance control	I	ORC = H: Low output resistance mode ORC = L: High output resistance mode ORC is pulled up to the V _{DD1} in the LSI.
POL	Polarity input	I	POL = L: The S _{2n-1} output uses V ₀ to V ₇ as the reference supply. The S _{2n} output uses V ₈ to V ₁₅ as the reference supply. POL = H: The S _{2n-1} output uses V ₈ to V ₁₅ as the reference supply. The S _{2n} output uses V ₀ to V ₇ as the reference supply. S _{2n-1} indicates the odd output and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge. When it switches such as POL = H→L or L→H, all output pins are output reset during STB = H. When it does not switch, all output pins become Hi-Z during STB = H. Refer to 7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM for details.

(2/2)

Pin Symbol	Pin Name	I/O	Description
MODE	Output reset control	I	MODE = H or open: Output reset MODE = L: No output reset MODE is pulled up to the V _{DD1} in the LSI.
POL21, POL22	Data inversion	I	Select of inversion or no inversion for input data. POL21: Data inversion or no inversion of Port1. POL22: Data inversion or no inversion of Port2 POL21/22 = H: Data are inverted in the LSI. POL21/22 = L: Data are not inverted in the LSI.
V _{SEL}	Driver voltage select	I	The driver voltage can be switched by controlling the stationary bias current of the output amplifier via V _{SEL} . V _{SEL} = H: V _{DD2} = 13.0 V (large bias current) V _{SEL} = L or open: V _{DD2} = 15.0 V (small bias current) LPC is pulled down to the V _{SS1} in the LSI.
V ₀ to V ₁₅	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. Make sure to maintain the following relationships. V _{DD2} –0.2 V ≥ V ₀ > V ₁ > V ₂ > > V ₆ > V ₇ ≥ 0.5 V _{DD2} + 0.5 V 0.5 V _{DD2} –0.5 V ≥ V ₈ > V ₉ > V ₁₀ > V ₁₄ > V ₁₅ ≥ V _{SS2} + 0.2 V
TEST	Test	I	Normally, set the TEST pin to high level or leave open. This pin is pulled up to V _{DD1} in the LSI.
V _{DD1}	Logic power supply	–	2.5 to 3.4 V
V _{DD2}	Driver power supply	–	13.0 ± 0.5 V or 15.0 ± 0.5 V
V _{SS1}	Logic ground	–	Grounding
V _{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V₀ to V₁₅ in that order. Reverse this sequence to shut down.

2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between V_{DD1} to V_{SS1} and V_{DD2} to V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.1 μF is also advised between the γ-corrected power supply terminals (V₀, V₁, V₂,....., V₁₅) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD16721 incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r253) are designed so that the ratio of LCD panel (γ-compensated voltages to V_{0'} to V_{255'} and V_{0''} to V_{255''}) is almost equivalent as shown in Figure 5-2 and 5-3. For the 2 sets of eight γ-compensated power supplies, V₀ to V₇ and V₈ to V₁₅, respectively, input gray scale voltages of the same polarity with respect to the 0.5 V_{DD2}.

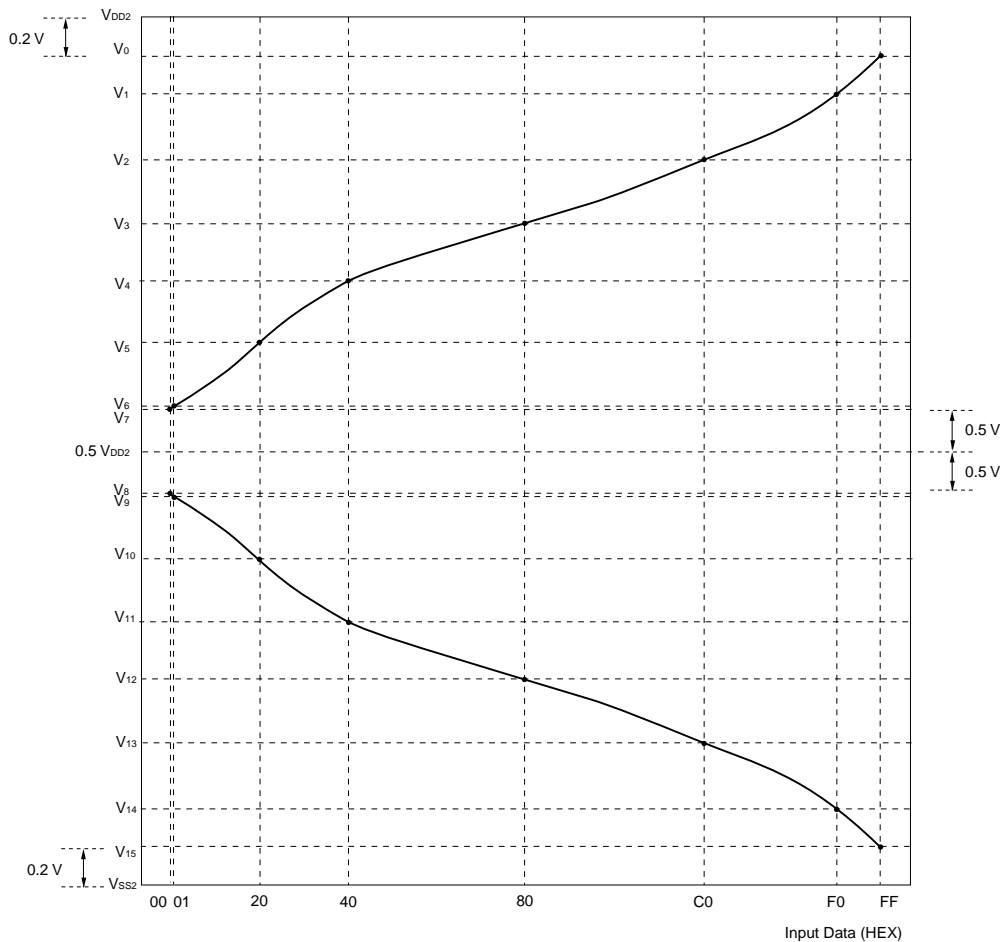
Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2}, V_{SS2} and 0.5 V_{DD2}, and γ-corrected voltages V₀ to V₁₅ and the input data. Be sure to maintain the voltage relationships below.

- ★ $V_{DD2} - 0.2\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5\text{ V}_{DD2} + 0.5\text{ V}$
- $0.5\text{ V}_{DD2} - 0.5\text{ V} \geq V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} \geq 0.5\text{ V}_{SS2} + 0.2\text{ V}$

Also, V₆ to V₇ and V₈ to V₉ are left open in the LSI. Be sure to input the gray scale level power supply at a constant level to the all pins, as V₀ to V₁₅.

Figures 5-2 and 5-3 show the relationship between the input data and the output voltage and the resistance values of the resistor strings.

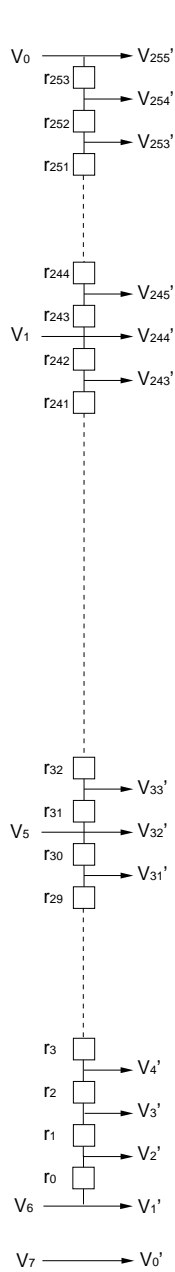
Figure 5-1. Relationship between Input Data and γ-corrected Power Supplies



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Figure 5-2. Relationship between Input Data and Output Voltage (1/4)

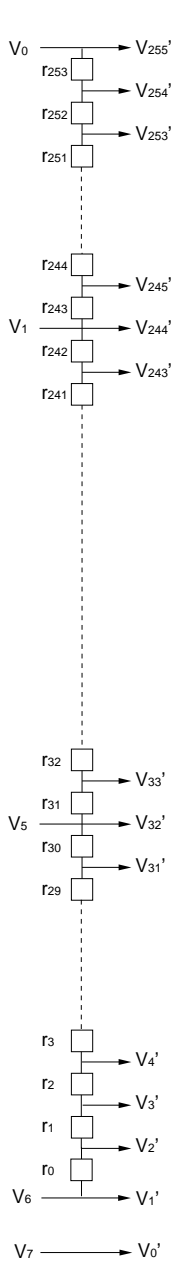
$V_{DD2} - 0.2 V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5 V$, POL21/22 = L



Input data	D _{x7}	D _{x6}	D _{x5}	D _{x4}	D _{x3}	D _{x2}	D _{x1}	D _{x0}	Output voltage	
									V _{0'}	V ₇
00H	0	0	0	0	0	0	0	0	V _{0'}	V ₇
01H	0	0	0	0	0	0	0	1	V _{1'}	V ₆
02H	0	0	0	0	0	0	1	0	V _{2'}	V _{6+(V5-V6) X}
03H	0	0	0	0	0	0	1	1	V _{3'}	V _{6+(V5-V6) X}
04H	0	0	0	0	0	1	0	0	V _{4'}	V _{6+(V5-V6) X}
05H	0	0	0	0	0	1	0	1	V _{5'}	V _{6+(V5-V6) X}
06H	0	0	0	0	0	1	1	0	V _{6'}	V _{6+(V5-V6) X}
07H	0	0	0	0	0	1	1	1	V _{7'}	V _{6+(V5-V6) X}
08H	0	0	0	0	1	0	0	0	V _{8'}	V _{6+(V5-V6) X}
09H	0	0	0	0	1	0	0	1	V _{9'}	V _{6+(V5-V6) X}
0AH	0	0	0	0	1	0	1	0	V _{10'}	V _{6+(V5-V6) X}
0BH	0	0	0	0	1	0	1	1	V _{11'}	V _{6+(V5-V6) X}
0CH	0	0	0	0	1	1	0	0	V _{12'}	V _{6+(V5-V6) X}
0DH	0	0	0	0	1	1	0	1	V _{13'}	V _{6+(V5-V6) X}
0EH	0	0	0	0	1	1	1	0	V _{14'}	V _{6+(V5-V6) X}
0FH	0	0	0	0	1	1	1	1	V _{15'}	V _{6+(V5-V6) X}
10H	0	0	0	1	0	0	0	0	V _{16'}	V _{6+(V5-V6) X}
11H	0	0	0	1	0	0	0	1	V _{17'}	V _{6+(V5-V6) X}
12H	0	0	0	1	0	0	1	0	V _{18'}	V _{6+(V5-V6) X}
13H	0	0	0	1	0	0	1	1	V _{19'}	V _{6+(V5-V6) X}
14H	0	0	0	1	0	1	0	0	V _{20'}	V _{6+(V5-V6) X}
15H	0	0	0	1	0	1	0	1	V _{21'}	V _{6+(V5-V6) X}
16H	0	0	0	1	0	1	1	0	V _{22'}	V _{6+(V5-V6) X}
17H	0	0	0	1	0	1	1	1	V _{23'}	V _{6+(V5-V6) X}
18H	0	0	0	1	1	0	0	0	V _{24'}	V _{6+(V5-V6) X}
19H	0	0	0	1	1	0	0	1	V _{25'}	V _{6+(V5-V6) X}
1AH	0	0	0	1	1	0	1	0	V _{26'}	V _{6+(V5-V6) X}
1BH	0	0	0	1	1	0	1	1	V _{27'}	V _{6+(V5-V6) X}
1CH	0	0	0	1	1	1	0	0	V _{28'}	V _{6+(V5-V6) X}
1DH	0	0	0	1	1	1	0	1	V _{29'}	V _{6+(V5-V6) X}
1EH	0	0	0	1	1	1	1	0	V _{30'}	V _{6+(V5-V6) X}
1FH	0	0	0	1	1	1	1	1	V _{31'}	V _{6+(V5-V6) X}
20H	0	0	1	0	0	0	0	0	V _{32'}	V ₅
21H	0	0	1	0	0	0	0	1	V _{33'}	V _{5+(V4-V5) X}
22H	0	0	1	0	0	0	1	0	V _{34'}	V _{5+(V4-V5) X}
23H	0	0	1	0	0	0	1	1	V _{35'}	V _{5+(V4-V5) X}
24H	0	0	1	0	0	1	0	0	V _{36'}	V _{5+(V4-V5) X}
25H	0	0	1	0	0	1	0	1	V _{37'}	V _{5+(V4-V5) X}
26H	0	0	1	0	0	1	1	0	V _{38'}	V _{5+(V4-V5) X}
27H	0	0	1	0	0	1	1	1	V _{39'}	V _{5+(V4-V5) X}
28H	0	0	1	0	1	0	0	0	V _{40'}	V _{5+(V4-V5) X}
29H	0	0	1	0	1	0	0	1	V _{41'}	V _{5+(V4-V5) X}
2AH	0	0	1	0	1	0	1	0	V _{42'}	V _{5+(V4-V5) X}
2BH	0	0	1	0	1	0	1	1	V _{43'}	V _{5+(V4-V5) X}
2CH	0	0	1	0	1	1	0	0	V _{44'}	V _{5+(V4-V5) X}
2DH	0	0	1	0	1	1	0	1	V _{45'}	V _{5+(V4-V5) X}
2EH	0	0	1	0	1	1	1	0	V _{46'}	V _{5+(V4-V5) X}
2FH	0	0	1	0	1	1	1	1	V _{47'}	V _{5+(V4-V5) X}
30H	0	0	1	1	0	0	0	0	V _{48'}	V _{5+(V4-V5) X}
31H	0	0	1	1	0	0	0	1	V _{49'}	V _{5+(V4-V5) X}
32H	0	0	1	1	0	0	1	0	V _{50'}	V _{5+(V4-V5) X}
33H	0	0	1	1	0	0	1	1	V _{51'}	V _{5+(V4-V5) X}
34H	0	0	1	1	0	1	0	0	V _{52'}	V _{5+(V4-V5) X}
35H	0	0	1	1	0	1	0	1	V _{53'}	V _{5+(V4-V5) X}
36H	0	0	1	1	0	1	1	0	V _{54'}	V _{5+(V4-V5) X}
37H	0	0	1	1	0	1	1	1	V _{55'}	V _{5+(V4-V5) X}
38H	0	0	1	1	1	0	0	0	V _{56'}	V _{5+(V4-V5) X}
39H	0	0	1	1	1	0	0	1	V _{57'}	V _{5+(V4-V5) X}
3AH	0	0	1	1	1	0	1	0	V _{58'}	V _{5+(V4-V5) X}
3BH	0	0	1	1	1	0	1	1	V _{59'}	V _{5+(V4-V5) X}
3CH	0	0	1	1	1	1	0	0	V _{60'}	V _{5+(V4-V5) X}
3DH	0	0	1	1	1	1	0	1	V _{61'}	V _{5+(V4-V5) X}
3EH	0	0	1	1	1	1	1	0	V _{62'}	V _{5+(V4-V5) X}
3FH	0	0	1	1	1	1	1	1	V _{63'}	V _{5+(V4-V5) X}

rn	(Ω)
r0	86
r1	86
r2	86
r3	86
r4	86
r5	84
r6	84
r7	82
r8	82
r9	80
r10	78
r11	78
r12	76
r13	74
r14	74
r15	72
r16	70
r17	68
r18	68
r19	66
r20	64
r21	64
r22	62
r23	60
r24	60
r25	58
r26	56
r27	56
r28	54
r29	54
r30	52
r31	52
r32	50
r33	50
r34	48
r35	48
r36	46
r37	46
r38	46
r39	44
r40	44
r41	44
r42	42
r43	42
r44	42
r45	40
r46	40
r47	40
r48	40
r49	38
r50	38
r51	38
r52	38
r53	36
r54	36
r55	36
r56	36
r57	34
r58	34
r59	34
r60	34
r61	34
r62	34

★ **Figure 5-2. Relationship between Input Data and Output Voltage (2/4)**
 $V_{DD2} - 0.2\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5\text{ V}$, POL21/22 = L



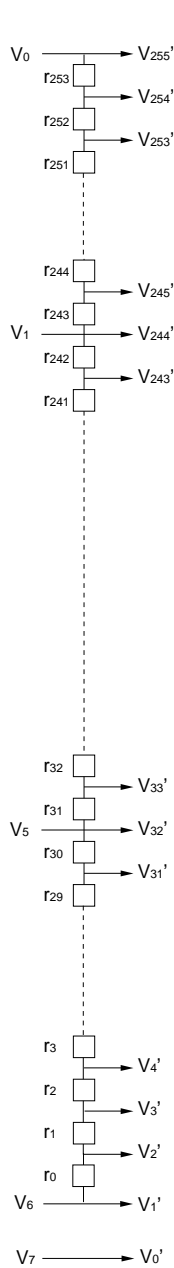
Input data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage	
40H	0	1	0	0	0	0	0	0	V64'	V4
41H	0	1	0	0	0	0	0	1	V65'	V4+(V3-V4) X 32 / 1772
42H	0	1	0	0	0	0	1	0	V66'	V4+(V3-V4) X 64 / 1772
43H	0	1	0	0	0	0	1	1	V67'	V4+(V3-V4) X 96 / 1772
44H	0	1	0	0	0	0	1	0	V68'	V4+(V3-V4) X 128 / 1772
45H	0	1	0	0	0	0	1	0	V69'	V4+(V3-V4) X 160 / 1772
46H	0	1	0	0	0	0	1	1	V70'	V4+(V3-V4) X 192 / 1772
47H	0	1	0	0	0	0	1	1	V71'	V4+(V3-V4) X 224 / 1772
48H	0	1	0	0	1	0	0	0	V72'	V4+(V3-V4) X 254 / 1772
49H	0	1	0	0	1	0	0	1	V73'	V4+(V3-V4) X 284 / 1772
4AH	0	1	0	0	1	0	1	0	V74'	V4+(V3-V4) X 314 / 1772
4BH	0	1	0	0	1	0	1	1	V75'	V4+(V3-V4) X 344 / 1772
4CH	0	1	0	0	1	1	0	0	V76'	V4+(V3-V4) X 374 / 1772
4DH	0	1	0	0	1	1	0	1	V77'	V4+(V3-V4) X 404 / 1772
4EH	0	1	0	0	1	1	1	0	V78'	V4+(V3-V4) X 434 / 1772
4FH	0	1	0	0	1	1	1	1	V79'	V4+(V3-V4) X 464 / 1772
50H	0	1	0	1	0	0	0	0	V80'	V4+(V3-V4) X 494 / 1772
51H	0	1	0	1	0	0	0	1	V81'	V4+(V3-V4) X 524 / 1772
52H	0	1	0	1	0	0	1	0	V82'	V4+(V3-V4) X 552 / 1772
53H	0	1	0	1	0	0	1	1	V83'	V4+(V3-V4) X 580 / 1772
54H	0	1	0	1	0	1	0	0	V84'	V4+(V3-V4) X 608 / 1772
55H	0	1	0	1	0	1	0	1	V85'	V4+(V3-V4) X 636 / 1772
56H	0	1	0	1	0	1	1	0	V86'	V4+(V3-V4) X 664 / 1772
57H	0	1	0	1	0	1	1	1	V87'	V4+(V3-V4) X 692 / 1772
58H	0	1	0	1	1	0	0	0	V88'	V4+(V3-V4) X 720 / 1772
59H	0	1	0	1	1	0	0	1	V89'	V4+(V3-V4) X 748 / 1772
5AH	0	1	0	1	1	0	1	0	V90'	V4+(V3-V4) X 776 / 1772
5BH	0	1	0	1	1	0	1	1	V91'	V4+(V3-V4) X 804 / 1772
5CH	0	1	0	1	1	1	0	0	V92'	V4+(V3-V4) X 832 / 1772
5DH	0	1	0	1	1	1	0	1	V93'	V4+(V3-V4) X 860 / 1772
5EH	0	1	0	1	1	1	1	0	V94'	V4+(V3-V4) X 888 / 1772
5FH	0	1	0	1	1	1	1	1	V95'	V4+(V3-V4) X 914 / 1772
60H	0	1	1	0	0	0	0	0	V96'	V4+(V3-V4) X 940 / 1772
61H	0	1	1	0	0	0	0	1	V97'	V4+(V3-V4) X 966 / 1772
62H	0	1	1	0	0	0	1	0	V98'	V4+(V3-V4) X 992 / 1772
63H	0	1	1	0	0	0	1	1	V99'	V4+(V3-V4) X 1018 / 1772
64H	0	1	1	0	0	1	0	0	V100'	V4+(V3-V4) X 1044 / 1772
65H	0	1	1	0	0	1	0	1	V101'	V4+(V3-V4) X 1070 / 1772
66H	0	1	1	0	0	1	1	0	V102'	V4+(V3-V4) X 1096 / 1772
67H	0	1	1	0	0	1	1	1	V103'	V4+(V3-V4) X 1122 / 1772
68H	0	1	1	0	1	0	0	0	V104'	V4+(V3-V4) X 1148 / 1772
69H	0	1	1	0	1	0	0	1	V105'	V4+(V3-V4) X 1174 / 1772
6AH	0	1	1	0	1	0	1	0	V106'	V4+(V3-V4) X 1200 / 1772
6BH	0	1	1	0	1	0	1	1	V107'	V4+(V3-V4) X 1226 / 1772
6CH	0	1	1	0	1	1	0	0	V108'	V4+(V3-V4) X 1252 / 1772
6DH	0	1	1	0	1	1	0	1	V109'	V4+(V3-V4) X 1278 / 1772
6EH	0	1	1	0	1	1	1	0	V110'	V4+(V3-V4) X 1304 / 1772
6FH	0	1	1	0	1	1	1	1	V111'	V4+(V3-V4) X 1330 / 1772
70H	0	1	1	1	0	0	0	0	V112'	V4+(V3-V4) X 1356 / 1772
71H	0	1	1	1	0	0	0	1	V113'	V4+(V3-V4) X 1382 / 1772
72H	0	1	1	1	0	0	1	0	V114'	V4+(V3-V4) X 1408 / 1772
73H	0	1	1	1	0	0	1	1	V115'	V4+(V3-V4) X 1434 / 1772
74H	0	1	1	1	0	1	0	0	V116'	V4+(V3-V4) X 1460 / 1772
75H	0	1	1	1	0	1	0	1	V117'	V4+(V3-V4) X 1486 / 1772
76H	0	1	1	1	0	1	1	0	V118'	V4+(V3-V4) X 1512 / 1772
77H	0	1	1	1	0	1	1	1	V119'	V4+(V3-V4) X 1538 / 1772
78H	0	1	1	1	1	0	0	0	V120'	V4+(V3-V4) X 1564 / 1772
79H	0	1	1	1	1	0	0	1	V121'	V4+(V3-V4) X 1590 / 1772
7AH	0	1	1	1	1	0	1	0	V122'	V4+(V3-V4) X 1616 / 1772
7BH	0	1	1	1	1	0	1	1	V123'	V4+(V3-V4) X 1642 / 1772
7CH	0	1	1	1	1	1	0	0	V124'	V4+(V3-V4) X 1668 / 1772
7DH	0	1	1	1	1	1	0	1	V125'	V4+(V3-V4) X 1694 / 1772
7EH	0	1	1	1	1	1	1	0	V126'	V4+(V3-V4) X 1720 / 1772
7FH	0	1	1	1	1	1	1	1	V127'	V4+(V3-V4) X 1746 / 1772

r n	(Ω)
r63	32
r64	32
r65	32
r66	32
r67	32
r68	32
r69	32
r70	30
r71	30
r72	30
r73	30
r74	30
r75	30
r76	30
r77	30
r78	30
r79	30
r80	28
r81	28
r82	28
r83	28
r84	28
r85	28
r86	28
r87	28
r88	28
r89	28
r90	28
r91	28
r92	28
r93	26
r94	26
r95	26
r96	26
r97	26
r98	26
r99	26
r100	26
r101	26
r102	26
r103	26
r104	26
r105	26
r106	26
r107	26
r108	26
r109	26
r110	26
r111	26
r112	26
r113	26
r114	26
r115	26
r116	26
r117	26
r118	26
r119	26
r120	26
r121	26
r122	26
r123	26
r124	26
r125	26
r126	26

★

Figure 5-2. Relationship between Input Data and Output Voltage (3/4)

$V_{DD2} - 0.2\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5\text{ V}$, POL21/22 = L



Input data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage		
80H	1	0	0	0	0	0	0	0	V126'	V3	
81H	1	0	0	0	0	0	0	1	V126'	V3+(V2-V3) X 26 / 1710	
82H	1	0	0	0	0	0	1	0	V130'	V3+(V2-V3) X 50 / 1710	
83H	1	0	0	0	0	0	1	1	V131'	V3+(V2-V3) X 76 / 1710	
84H	1	0	0	0	0	1	0	0	V132'	V3+(V2-V3) X 100 / 1710	
85H	1	0	0	0	0	0	1	0	1	V133'	V3+(V2-V3) X 124 / 1710
86H	1	0	0	0	0	1	1	0	V134'	V3+(V2-V3) X 148 / 1710	
87H	1	0	0	0	0	1	1	1	V135'	V3+(V2-V3) X 172 / 1710	
88H	1	0	0	0	1	0	0	0	V136'	V3+(V2-V3) X 198 / 1710	
89H	1	0	0	0	1	0	0	1	V137'	V3+(V2-V3) X 224 / 1710	
8AH	1	0	0	0	1	0	1	0	V138'	V3+(V2-V3) X 250 / 1710	
8BH	1	0	0	0	1	0	1	1	V139'	V3+(V2-V3) X 276 / 1710	
8CH	1	0	0	0	1	1	0	0	V140'	V3+(V2-V3) X 302 / 1710	
8DH	1	0	0	0	1	1	0	1	V141'	V3+(V2-V3) X 328 / 1710	
8EH	1	0	0	0	1	1	1	0	V142'	V3+(V2-V3) X 354 / 1710	
8FH	1	0	0	0	1	1	1	1	V143'	V3+(V2-V3) X 380 / 1710	
90H	1	0	0	1	0	0	0	0	V144'	V3+(V2-V3) X 406 / 1710	
91H	1	0	0	1	0	0	0	1	V145'	V3+(V2-V3) X 432 / 1710	
92H	1	0	0	1	0	0	1	0	V146'	V3+(V2-V3) X 458 / 1710	
93H	1	0	0	1	0	0	1	1	V147'	V3+(V2-V3) X 484 / 1710	
94H	1	0	0	1	0	1	0	0	V148'	V3+(V2-V3) X 510 / 1710	
95H	1	0	0	1	0	1	0	1	V149'	V3+(V2-V3) X 536 / 1710	
96H	1	0	0	1	0	1	1	0	V150'	V3+(V2-V3) X 562 / 1710	
97H	1	0	0	1	0	1	1	1	V151'	V3+(V2-V3) X 588 / 1710	
98H	1	0	0	1	1	0	0	0	V152'	V3+(V2-V3) X 614 / 1710	
99H	1	0	0	1	1	0	0	1	V153'	V3+(V2-V3) X 640 / 1710	
9AH	1	0	0	1	1	0	1	0	V154'	V3+(V2-V3) X 666 / 1710	
9BH	1	0	0	1	1	0	1	1	V155'	V3+(V2-V3) X 692 / 1710	
9CH	1	0	0	1	1	1	0	0	V156'	V3+(V2-V3) X 718 / 1710	
9DH	1	0	0	1	1	1	0	1	V157'	V3+(V2-V3) X 744 / 1710	
9EH	1	0	0	1	1	1	1	0	V158'	V3+(V2-V3) X 770 / 1710	
9FH	1	0	0	1	1	1	1	1	V159'	V3+(V2-V3) X 796 / 1710	
A0H	1	0	1	0	0	0	0	0	V160'	V3+(V2-V3) X 822 / 1710	
A1H	1	0	1	0	0	0	0	1	V161'	V3+(V2-V3) X 848 / 1710	
A2H	1	0	1	0	0	0	1	0	V162'	V3+(V2-V3) X 874 / 1710	
A3H	1	0	1	0	0	0	1	1	V163'	V3+(V2-V3) X 900 / 1710	
A4H	1	0	1	0	0	1	0	0	V164'	V3+(V2-V3) X 926 / 1710	
A5H	1	0	1	0	0	1	0	1	V165'	V3+(V2-V3) X 952 / 1710	
A6H	1	0	1	0	0	1	1	0	V166'	V3+(V2-V3) X 978 / 1710	
A7H	1	0	1	0	0	1	1	1	V167'	V3+(V2-V3) X 1004 / 1710	
A8H	1	0	1	0	1	0	0	0	V168'	V3+(V2-V3) X 1030 / 1710	
A9H	1	0	1	0	1	0	0	1	V169'	V3+(V2-V3) X 1056 / 1710	
AAH	1	0	1	0	1	0	1	0	V170'	V3+(V2-V3) X 1082 / 1710	
ABH	1	0	1	0	1	0	1	1	V171'	V3+(V2-V3) X 1108 / 1710	
ACH	1	0	1	0	1	1	0	0	V172'	V3+(V2-V3) X 1136 / 1710	
ADH	1	0	1	0	1	1	0	1	V173'	V3+(V2-V3) X 1164 / 1710	
AEH	1	0	1	0	1	1	1	0	V174'	V3+(V2-V3) X 1192 / 1710	
AFH	1	0	1	0	1	1	1	1	V175'	V3+(V2-V3) X 1220 / 1710	
B0H	1	0	1	1	0	0	0	0	V176'	V3+(V2-V3) X 1248 / 1710	
B1H	1	0	1	1	0	0	0	1	V177'	V3+(V2-V3) X 1276 / 1710	
B2H	1	0	1	1	0	0	1	0	V178'	V3+(V2-V3) X 1304 / 1710	
B3H	1	0	1	1	0	0	1	1	V179'	V3+(V2-V3) X 1332 / 1710	
B4H	1	0	1	1	0	1	0	0	V180'	V3+(V2-V3) X 1360 / 1710	
B5H	1	0	1	1	0	1	0	1	V181'	V3+(V2-V3) X 1388 / 1710	
B6H	1	0	1	1	0	1	1	0	V182'	V3+(V2-V3) X 1416 / 1710	
B7H	1	0	1	1	0	1	1	1	V183'	V3+(V2-V3) X 1444 / 1710	
B8H	1	0	1	1	1	0	0	0	V184'	V3+(V2-V3) X 1472 / 1710	
B9H	1	0	1	1	1	0	0	1	V185'	V3+(V2-V3) X 1500 / 1710	
BAH	1	0	1	1	1	0	1	0	V186'	V3+(V2-V3) X 1530 / 1710	
BBH	1	0	1	1	1	0	1	1	V187'	V3+(V2-V3) X 1560 / 1710	
BCH	1	0	1	1	1	1	0	0	V188'	V3+(V2-V3) X 1590 / 1710	
BDH	1	0	1	1	1	1	0	1	V189'	V3+(V2-V3) X 1620 / 1710	
BEH	1	0	1	1	1	1	1	0	V190'	V3+(V2-V3) X 1650 / 1710	
BFH	1	0	1	1	1	1	1	1	V191'	V3+(V2-V3) X 1680 / 1710	

rn	(Ω)
r127	26
r128	24
r129	26
r130	24
r131	24
r132	24
r133	24
r134	26
r135	26
r136	26
r137	26
r138	26
r139	26
r140	26
r141	26
r142	26
r143	26
r144	26
r145	26
r146	26
r147	26
r148	26
r149	26
r150	26
r151	26
r152	26
r153	26
r154	26
r155	26
r156	26
r157	26
r158	26
r159	26
r160	26
r161	26
r162	26
r163	26
r164	26
r165	26
r166	26
r167	26
r168	26
r169	26
r170	28
r171	28
r172	28
r173	28
r174	28
r175	28
r176	28
r177	28
r178	28
r179	28
r180	28
r181	28
r182	28
r183	28
r184	30
r185	30
r186	30
r187	30
r188	30
r189	30
r190	30

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Figure 5-2. Relationship between Input Data and Output Voltage (4/4)

$$V_{DD2} - 0.2 \text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 \geq 0.5 V_{DD2} + 0.5 \text{ V, POL21/22} = L$$

Input data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage		rn	(Ω)
C0H	1	1	0	0	0	0	0	0	V192'	V2		
C1H	1	1	0	0	0	0	0	1	V193'	V2+(V1-V2) X	30 /	1966
C2H	1	1	0	0	0	0	1	0	V194'	V2+(V1-V2) X	60 /	1966
C3H	1	1	0	0	0	0	1	1	V195'	V2+(V1-V2) X	90 /	1966
C4H	1	1	0	0	0	1	0	0	V196'	V2+(V1-V2) X	122 /	1966
C5H	1	1	0	0	0	1	0	1	V197'	V2+(V1-V2) X	154 /	1966
C6H	1	1	0	0	0	1	1	0	V198'	V2+(V1-V2) X	186 /	1966
C7H	1	1	0	0	0	1	1	1	V199'	V2+(V1-V2) X	218 /	1966
C8H	1	1	0	0	1	0	0	0	V200'	V2+(V1-V2) X	250 /	1966
C9H	1	1	0	0	1	0	0	1	V201'	V2+(V1-V2) X	282 /	1966
CAH	1	1	0	0	1	0	1	0	V202'	V2+(V1-V2) X	314 /	1966
CBH	1	1	0	0	1	0	1	1	V203'	V2+(V1-V2) X	348 /	1966
CCH	1	1	0	0	1	1	0	0	V204'	V2+(V1-V2) X	382 /	1966
CDH	1	1	0	0	1	1	0	1	V205'	V2+(V1-V2) X	416 /	1966
CEH	1	1	0	0	1	1	1	0	V206'	V2+(V1-V2) X	450 /	1966
CFH	1	1	0	0	1	1	1	1	V207'	V2+(V1-V2) X	484 /	1966
D0H	1	1	0	1	0	0	0	0	V208'	V2+(V1-V2) X	518 /	1966
D1H	1	1	0	1	0	0	0	1	V209'	V2+(V1-V2) X	554 /	1966
D2H	1	1	0	1	0	0	1	0	V210'	V2+(V1-V2) X	590 /	1966
D3H	1	1	0	1	0	0	1	1	V211'	V2+(V1-V2) X	626 /	1966
D4H	1	1	0	1	0	1	0	0	V212'	V2+(V1-V2) X	662 /	1966
D5H	1	1	0	1	0	1	0	1	V213'	V2+(V1-V2) X	698 /	1966
D6H	1	1	0	1	0	1	1	0	V214'	V2+(V1-V2) X	736 /	1966
D7H	1	1	0	1	0	1	1	1	V215'	V2+(V1-V2) X	774 /	1966
D8H	1	1	0	1	1	0	0	0	V216'	V2+(V1-V2) X	812 /	1966
D9H	1	1	0	1	1	0	0	1	V217'	V2+(V1-V2) X	850 /	1966
DAH	1	1	0	1	1	0	1	0	V218'	V2+(V1-V2) X	890 /	1966
DBH	1	1	0	1	1	0	1	1	V219'	V2+(V1-V2) X	930 /	1966
DCH	1	1	0	1	1	1	0	0	V220'	V2+(V1-V2) X	970 /	1966
DDH	1	1	0	1	1	1	0	1	V221'	V2+(V1-V2) X	1012 /	1966
DEH	1	1	0	1	1	1	1	0	V222'	V2+(V1-V2) X	1054 /	1966
DFH	1	1	0	1	1	1	1	1	V223'	V2+(V1-V2) X	1096 /	1966
E0H	1	1	1	0	0	0	0	0	V224'	V2+(V1-V2) X	1140 /	1966
E1H	1	1	1	0	0	0	0	1	V225'	V2+(V1-V2) X	1184 /	1966
E2H	1	1	1	0	0	0	1	0	V226'	V2+(V1-V2) X	1228 /	1966
E3H	1	1	1	0	0	0	1	1	V227'	V2+(V1-V2) X	1274 /	1966
E4H	1	1	1	0	0	1	0	0	V228'	V2+(V1-V2) X	1320 /	1966
E5H	1	1	1	0	0	1	0	1	V229'	V2+(V1-V2) X	1368 /	1966
E6H	1	1	1	0	0	1	1	0	V230'	V2+(V1-V2) X	1416 /	1966
E7H	1	1	1	0	0	1	1	1	V231'	V2+(V1-V2) X	1466 /	1966
E8H	1	1	1	0	1	0	0	0	V232'	V2+(V1-V2) X	1516 /	1966
E9H	1	1	1	0	1	0	0	1	V233'	V2+(V1-V2) X	1568 /	1966
EAH	1	1	1	0	1	0	1	0	V234'	V2+(V1-V2) X	1620 /	1966
EBH	1	1	1	0	1	0	1	1	V235'	V2+(V1-V2) X	1674 /	1966
ECH	1	1	1	0	1	1	0	0	V236'	V2+(V1-V2) X	1730 /	1966
EDH	1	1	1	0	1	1	0	1	V237'	V2+(V1-V2) X	1786 /	1966
EEH	1	1	1	0	1	1	1	0	V238'	V2+(V1-V2) X	1844 /	1966
EFH	1	1	1	0	1	1	1	1	V239'	V2+(V1-V2) X	1904 /	1966
F0H	1	1	1	1	0	0	0	0	V240'	V1		
F1H	1	1	1	1	0	0	0	1	V241'	V1+(V0-V1) X	64 /	1322
F2H	1	1	1	1	0	0	1	0	V242'	V1+(V0-V1) X	130 /	1322
F3H	1	1	1	1	0	0	1	1	V243'	V1+(V0-V1) X	198 /	1322
F4H	1	1	1	1	0	1	0	0	V244'	V1+(V0-V1) X	268 /	1322
F5H	1	1	1	1	0	1	0	1	V245'	V1+(V0-V1) X	340 /	1322
F6H	1	1	1	1	0	1	1	0	V246'	V1+(V0-V1) X	416 /	1322
F7H	1	1	1	1	0	1	1	1	V247'	V1+(V0-V1) X	496 /	1322
F8H	1	1	1	1	1	0	0	0	V248'	V1+(V0-V1) X	578 /	1322
F9H	1	1	1	1	1	0	0	1	V249'	V1+(V0-V1) X	664 /	1322
FAH	1	1	1	1	1	0	1	0	V250'	V1+(V0-V1) X	756 /	1322
FBH	1	1	1	1	1	0	1	1	V251'	V1+(V0-V1) X	854 /	1322
FCH	1	1	1	1	1	1	0	0	V252'	V1+(V0-V1) X	958 /	1322
FDH	1	1	1	1	1	1	0	1	V253'	V1+(V0-V1) X	1070 /	1322
FEH	1	1	1	1	1	1	1	0	V254'	V1+(V0-V1) X	1190 /	1322
FFH	1	1	1	1	1	1	1	1	V255'	V0		
TOTAL												10280

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Figure 5-3. Relationship between Input Data and Output Voltage (1/4)

0.5 V_{DD2}-0.5 V ≥ V₈ > V₉ > V₁₀ > V₁₁ > V₁₂ > V₁₃ > V₁₄ > V₁₅ ≥ V_{SS2}+0.2 V, POL21/22 = L

Input data	Dx7	Dx8	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage		rn	(Ω)
									V ₀ ''	V ₈		
00H	0	0	0	0	0	0	0	0	V ₀ ''	V ₈		
01H	0	0	0	0	0	0	0	1	V ₁ ''	V ₉	r0	86
02H	0	0	0	0	0	0	1	0	V ₂ ''	V ₁₀ +(V ₉ -V ₁₀) X	r1	86
03H	0	0	0	0	0	0	1	1	V ₃ ''	V ₁₀ +(V ₉ -V ₁₀) X	r2	86
04H	0	0	0	0	0	0	1	0	V ₄ ''	V ₁₀ +(V ₉ -V ₁₀) X	r3	86
05H	0	0	0	0	0	1	0	1	V ₅ ''	V ₁₀ +(V ₉ -V ₁₀) X	r4	86
06H	0	0	0	0	0	1	1	0	V ₆ ''	V ₁₀ +(V ₉ -V ₁₀) X	r5	84
07H	0	0	0	0	0	1	1	1	V ₇ ''	V ₁₀ +(V ₉ -V ₁₀) X	r6	84
08H	0	0	0	0	1	0	0	0	V ₈ ''	V ₁₀ +(V ₉ -V ₁₀) X	r7	82
09H	0	0	0	0	1	0	0	1	V ₉ ''	V ₁₀ +(V ₉ -V ₁₀) X	r8	82
0AH	0	0	0	0	1	0	1	0	V ₁₀ ''	V ₁₀ +(V ₉ -V ₁₀) X	r9	80
0BH	0	0	0	0	1	0	1	1	V ₁₁ ''	V ₁₀ +(V ₉ -V ₁₀) X	r10	78
0CH	0	0	0	0	1	1	0	0	V ₁₂ ''	V ₁₀ +(V ₉ -V ₁₀) X	r11	78
0DH	0	0	0	0	1	1	0	1	V ₁₃ ''	V ₁₀ +(V ₉ -V ₁₀) X	r12	76
0EH	0	0	0	0	1	1	1	0	V ₁₄ ''	V ₁₀ +(V ₉ -V ₁₀) X	r13	74
0FH	0	0	0	0	1	1	1	1	V ₁₅ ''	V ₁₀ +(V ₉ -V ₁₀) X	r14	74
10H	0	0	0	1	0	0	0	0	V ₁₆ ''	V ₁₀ +(V ₉ -V ₁₀) X	r15	72
11H	0	0	0	1	0	0	0	1	V ₁₇ ''	V ₁₀ +(V ₉ -V ₁₀) X	r16	70
12H	0	0	0	1	0	0	1	0	V ₁₈ ''	V ₁₀ +(V ₉ -V ₁₀) X	r17	68
13H	0	0	0	1	0	0	1	1	V ₁₉ ''	V ₁₀ +(V ₉ -V ₁₀) X	r18	68
14H	0	0	0	1	0	1	0	0	V ₂₀ ''	V ₁₀ +(V ₉ -V ₁₀) X	r19	66
15H	0	0	0	1	0	1	0	1	V ₂₁ ''	V ₁₀ +(V ₉ -V ₁₀) X	r20	64
16H	0	0	0	1	0	1	1	0	V ₂₂ ''	V ₁₀ +(V ₉ -V ₁₀) X	r21	64
17H	0	0	0	1	0	1	1	1	V ₂₃ ''	V ₁₀ +(V ₉ -V ₁₀) X	r22	62
18H	0	0	0	1	1	0	0	0	V ₂₄ ''	V ₁₀ +(V ₉ -V ₁₀) X	r23	60
19H	0	0	0	1	1	0	0	1	V ₂₅ ''	V ₁₀ +(V ₉ -V ₁₀) X	r24	60
1AH	0	0	0	1	1	0	1	0	V ₂₆ ''	V ₁₀ +(V ₉ -V ₁₀) X	r25	58
1BH	0	0	0	1	1	0	1	1	V ₂₇ ''	V ₁₀ +(V ₉ -V ₁₀) X	r26	56
1CH	0	0	0	1	1	1	0	0	V ₂₈ ''	V ₁₀ +(V ₉ -V ₁₀) X	r27	56
1DH	0	0	0	1	1	1	0	1	V ₂₉ ''	V ₁₀ +(V ₉ -V ₁₀) X	r28	54
1EH	0	0	0	1	1	1	1	0	V ₃₀ ''	V ₁₀ +(V ₉ -V ₁₀) X	r29	54
1FH	0	0	0	1	1	1	1	1	V ₃₁ ''	V ₁₀ +(V ₉ -V ₁₀) X	r30	52
20H	0	0	1	0	0	0	0	0	V ₃₂ ''	V ₁₀	r31	52
21H	0	0	1	0	0	0	0	1	V ₃₃ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r32	50
22H	0	0	1	0	0	0	1	0	V ₃₄ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r33	50
23H	0	0	1	0	0	0	1	1	V ₃₅ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r34	48
24H	0	0	1	0	0	1	0	0	V ₃₆ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r35	48
25H	0	0	1	0	0	1	0	1	V ₃₇ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r36	46
26H	0	0	1	0	0	1	1	0	V ₃₈ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r37	46
27H	0	0	1	0	0	1	1	1	V ₃₉ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r38	46
28H	0	0	1	0	1	0	0	0	V ₄₀ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r39	44
29H	0	0	1	0	1	0	0	1	V ₄₁ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r40	44
2AH	0	0	1	0	1	0	1	0	V ₄₂ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r41	44
2BH	0	0	1	0	1	0	1	1	V ₄₃ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r42	42
2CH	0	0	1	0	1	1	0	0	V ₄₄ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r43	42
2DH	0	0	1	0	1	1	0	1	V ₄₅ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r44	42
2EH	0	0	1	0	1	1	1	0	V ₄₆ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r45	40
2FH	0	0	1	0	1	1	1	1	V ₄₇ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r46	40
30H	0	0	1	1	0	0	0	0	V ₄₈ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r47	40
31H	0	0	1	1	0	0	0	1	V ₄₉ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r48	40
32H	0	0	1	1	0	0	1	0	V ₅₀ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r49	38
33H	0	0	1	1	0	0	1	1	V ₅₁ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r50	38
34H	0	0	1	1	0	1	0	0	V ₅₂ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r51	38
35H	0	0	1	1	0	1	0	1	V ₅₃ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r52	38
36H	0	0	1	1	0	1	1	0	V ₅₄ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r53	36
37H	0	0	1	1	0	1	1	1	V ₅₅ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r54	36
38H	0	0	1	1	1	0	0	0	V ₅₆ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r55	36
39H	0	0	1	1	1	0	0	1	V ₅₇ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r56	36
3AH	0	0	1	1	1	0	1	0	V ₅₈ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r57	34
3BH	0	0	1	1	1	0	1	1	V ₅₉ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r58	34
3CH	0	0	1	1	1	1	0	0	V ₆₀ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r59	34
3DH	0	0	1	1	1	1	0	1	V ₆₁ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r60	34
3EH	0	0	1	1	1	1	1	0	V ₆₂ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r61	34
3FH	0	0	1	1	1	1	1	1	V ₆₃ ''	V ₁₁ +(V ₁₀ -V ₁₁) X	r62	34

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Figure 5-3. Relationship between Input Data and Output Voltage (2/4)

0.5 V_{DD2}-0.5 V ≥ V₈ > V₉ > V₁₀ > V₁₁ > V₁₂ > V₁₃ > V₁₄ > V₁₅ ≥ V_{SS2}+0.2 V, POL21/22 = L

Input data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage		rn	(Ω)
40H	0	1	0	0	0	0	0	0	V64 ⁿ	V11	r63	32
41H	0	1	0	0	0	0	0	1	V65 ⁿ	V12+(V11-V12) X	r64	32
42H	0	1	0	0	0	0	1	0	V66 ⁿ	V12+(V11-V12) X	r65	32
43H	0	1	0	0	0	0	1	1	V67 ⁿ	V12+(V11-V12) X	r66	32
44H	0	1	0	0	0	1	0	0	V68 ⁿ	V12+(V11-V12) X	r67	32
45H	0	1	0	0	0	1	0	1	V69 ⁿ	V12+(V11-V12) X	r68	32
46H	0	1	0	0	0	1	1	0	V70 ⁿ	V12+(V11-V12) X	r69	32
47H	0	1	0	0	0	1	1	1	V71 ⁿ	V12+(V11-V12) X	r70	30
48H	0	1	0	0	1	0	0	0	V72 ⁿ	V12+(V11-V12) X	r71	30
49H	0	1	0	0	1	0	0	1	V73 ⁿ	V12+(V11-V12) X	r72	30
4AH	0	1	0	0	1	0	1	0	V74 ⁿ	V12+(V11-V12) X	r73	30
4BH	0	1	0	0	1	0	1	1	V75 ⁿ	V12+(V11-V12) X	r74	30
4CH	0	1	0	0	1	1	0	0	V76 ⁿ	V12+(V11-V12) X	r75	30
4DH	0	1	0	0	1	1	0	1	V77 ⁿ	V12+(V11-V12) X	r76	30
4EH	0	1	0	0	1	1	1	0	V78 ⁿ	V12+(V11-V12) X	r77	30
4FH	0	1	0	0	1	1	1	1	V79 ⁿ	V12+(V11-V12) X	r78	30
50H	0	1	0	1	0	0	0	0	V80 ⁿ	V12+(V11-V12) X	r79	30
51H	0	1	0	1	0	0	0	1	V81 ⁿ	V12+(V11-V12) X	r80	28
52H	0	1	0	1	0	0	1	0	V82 ⁿ	V12+(V11-V12) X	r81	28
53H	0	1	0	1	0	0	1	1	V83 ⁿ	V12+(V11-V12) X	r82	28
54H	0	1	0	1	0	1	0	0	V84 ⁿ	V12+(V11-V12) X	r83	28
55H	0	1	0	1	0	1	0	1	V85 ⁿ	V12+(V11-V12) X	r84	28
56H	0	1	0	1	0	1	1	0	V86 ⁿ	V12+(V11-V12) X	r85	28
57H	0	1	0	1	0	1	1	1	V87 ⁿ	V12+(V11-V12) X	r86	28
58H	0	1	0	1	1	0	0	0	V88 ⁿ	V12+(V11-V12) X	r87	28
59H	0	1	0	1	1	0	0	1	V89 ⁿ	V12+(V11-V12) X	r88	28
5AH	0	1	0	1	1	0	1	0	V90 ⁿ	V12+(V11-V12) X	r89	28
5BH	0	1	0	1	1	0	1	1	V91 ⁿ	V12+(V11-V12) X	r90	28
5CH	0	1	0	1	1	1	0	0	V92 ⁿ	V12+(V11-V12) X	r91	28
5DH	0	1	0	1	1	1	0	1	V93 ⁿ	V12+(V11-V12) X	r92	28
5EH	0	1	0	1	1	1	1	0	V94 ⁿ	V12+(V11-V12) X	r93	26
5FH	0	1	0	1	1	1	1	1	V95 ⁿ	V12+(V11-V12) X	r94	26
60H	0	1	1	0	0	0	0	0	V96 ⁿ	V12+(V11-V12) X	r95	26
61H	0	1	1	0	0	0	0	1	V97 ⁿ	V12+(V11-V12) X	r96	26
62H	0	1	1	0	0	0	1	0	V98 ⁿ	V12+(V11-V12) X	r97	26
63H	0	1	1	0	0	0	1	1	V99 ⁿ	V12+(V11-V12) X	r98	26
64H	0	1	1	0	0	1	0	0	V100 ⁿ	V12+(V11-V12) X	r99	26
65H	0	1	1	0	0	1	0	1	V101 ⁿ	V12+(V11-V12) X	r100	26
66H	0	1	1	0	0	1	1	0	V102 ⁿ	V12+(V11-V12) X	r101	26
67H	0	1	1	0	0	1	1	1	V103 ⁿ	V12+(V11-V12) X	r102	26
68H	0	1	1	0	1	0	0	0	V104 ⁿ	V12+(V11-V12) X	r103	26
69H	0	1	1	0	1	0	0	1	V105 ⁿ	V12+(V11-V12) X	r104	26
6AH	0	1	1	0	1	0	1	0	V106 ⁿ	V12+(V11-V12) X	r105	26
6BH	0	1	1	0	1	0	1	1	V107 ⁿ	V12+(V11-V12) X	r106	26
6CH	0	1	1	0	1	1	0	0	V108 ⁿ	V12+(V11-V12) X	r107	26
6DH	0	1	1	0	1	1	0	1	V109 ⁿ	V12+(V11-V12) X	r108	26
6EH	0	1	1	0	1	1	1	0	V110 ⁿ	V12+(V11-V12) X	r109	26
6FH	0	1	1	0	1	1	1	1	V111 ⁿ	V12+(V11-V12) X	r110	26
70H	0	1	1	1	0	0	0	0	V112 ⁿ	V12+(V11-V12) X	r111	26
71H	0	1	1	1	0	0	0	1	V113 ⁿ	V12+(V11-V12) X	r112	26
72H	0	1	1	1	0	0	1	0	V114 ⁿ	V12+(V11-V12) X	r113	26
73H	0	1	1	1	0	0	1	1	V115 ⁿ	V12+(V11-V12) X	r114	26
74H	0	1	1	1	0	1	0	0	V116 ⁿ	V12+(V11-V12) X	r115	26
75H	0	1	1	1	0	1	0	1	V117 ⁿ	V12+(V11-V12) X	r116	26
76H	0	1	1	1	0	1	1	0	V118 ⁿ	V12+(V11-V12) X	r117	26
77H	0	1	1	1	0	1	1	1	V119 ⁿ	V12+(V11-V12) X	r118	26
78H	0	1	1	1	1	0	0	0	V120 ⁿ	V12+(V11-V12) X	r119	26
79H	0	1	1	1	1	0	0	1	V121 ⁿ	V12+(V11-V12) X	r120	26
7AH	0	1	1	1	1	0	1	0	V122 ⁿ	V12+(V11-V12) X	r121	26
7BH	0	1	1	1	1	0	1	1	V123 ⁿ	V12+(V11-V12) X	r122	26
7CH	0	1	1	1	1	1	0	0	V124 ⁿ	V12+(V11-V12) X	r123	26
7DH	0	1	1	1	1	1	0	1	V125 ⁿ	V12+(V11-V12) X	r124	26
7EH	0	1	1	1	1	1	1	0	V126 ⁿ	V12+(V11-V12) X	r125	26
7FH	0	1	1	1	1	1	1	1	V127 ⁿ	V12+(V11-V12) X	r126	26

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Figure 5-3. Relationship between Input Data and Output Voltage (3/4)

$0.5 V_{DD2} - 0.5 V \geq V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} \geq V_{SS2} + 0.2 V, POL21/22 = L$

Input data	Dx7	Dx8	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage			rn	(Ω)
80H	1	0	0	0	0	0	0	0	V128''	V12			
81H	1	0	0	0	0	0	0	1	V129''	V13+(V12-V13) X	1684 / 1710	r127	26
82H	1	0	0	0	0	0	1	0	V130''	V13+(V12-V13) X	1660 / 1710	r128	24
83H	1	0	0	0	0	0	1	1	V131''	V13+(V12-V13) X	1634 / 1710	r129	26
84H	1	0	0	0	0	1	0	0	V132''	V13+(V12-V13) X	1610 / 1710	r130	24
85H	1	0	0	0	0	1	0	1	V133''	V13+(V12-V13) X	1586 / 1710	r131	24
86H	1	0	0	0	0	1	1	0	V134''	V13+(V12-V13) X	1562 / 1710	r132	24
87H	1	0	0	0	0	1	1	1	V135''	V13+(V12-V13) X	1538 / 1710	r133	24
88H	1	0	0	0	1	0	0	0	V136''	V13+(V12-V13) X	1512 / 1710	r134	26
89H	1	0	0	0	1	0	0	1	V137''	V13+(V12-V13) X	1486 / 1710	r135	26
8AH	1	0	0	0	1	0	1	0	V138''	V13+(V12-V13) X	1460 / 1710	r136	26
8BH	1	0	0	0	1	0	1	1	V139''	V13+(V12-V13) X	1434 / 1710	r137	26
8CH	1	0	0	0	1	1	0	0	V140''	V13+(V12-V13) X	1408 / 1710	r138	26
8DH	1	0	0	0	1	1	0	1	V141''	V13+(V12-V13) X	1382 / 1710	r139	26
8EH	1	0	0	0	1	1	1	0	V142''	V13+(V12-V13) X	1356 / 1710	r140	26
8FH	1	0	0	0	1	1	1	1	V143''	V13+(V12-V13) X	1330 / 1710	r141	26
90H	1	0	0	1	0	0	0	0	V144''	V13+(V12-V13) X	1304 / 1710	r142	26
91H	1	0	0	1	0	0	0	1	V145''	V13+(V12-V13) X	1278 / 1710	r143	26
92H	1	0	0	1	0	0	1	0	V146''	V13+(V12-V13) X	1252 / 1710	r144	26
93H	1	0	0	1	0	0	1	1	V147''	V13+(V12-V13) X	1226 / 1710	r145	26
94H	1	0	0	1	0	1	0	0	V148''	V13+(V12-V13) X	1200 / 1710	r146	26
95H	1	0	0	1	0	1	0	1	V149''	V13+(V12-V13) X	1174 / 1710	r147	26
96H	1	0	0	1	0	1	1	0	V150''	V13+(V12-V13) X	1148 / 1710	r148	26
97H	1	0	0	1	0	1	1	1	V151''	V13+(V12-V13) X	1122 / 1710	r149	26
98H	1	0	0	1	1	0	0	0	V152''	V13+(V12-V13) X	1096 / 1710	r150	26
99H	1	0	0	1	1	0	0	1	V153''	V13+(V12-V13) X	1070 / 1710	r151	26
9AH	1	0	0	1	1	0	1	0	V154''	V13+(V12-V13) X	1044 / 1710	r152	26
9BH	1	0	0	1	1	0	1	1	V155''	V13+(V12-V13) X	1018 / 1710	r153	26
9CH	1	0	0	1	1	1	0	0	V156''	V13+(V12-V13) X	992 / 1710	r154	26
9DH	1	0	0	1	1	1	0	1	V157''	V13+(V12-V13) X	966 / 1710	r155	26
9EH	1	0	0	1	1	1	1	0	V158''	V13+(V12-V13) X	940 / 1710	r156	26
9FH	1	0	0	1	1	1	1	1	V159''	V13+(V12-V13) X	914 / 1710	r157	26
A0H	1	0	1	0	0	0	0	0	V160''	V13+(V12-V13) X	888 / 1710	r158	26
A1H	1	0	1	0	0	0	0	1	V161''	V13+(V12-V13) X	862 / 1710	r159	26
A2H	1	0	1	0	0	0	1	0	V162''	V13+(V12-V13) X	836 / 1710	r160	26
A3H	1	0	1	0	0	0	1	1	V163''	V13+(V12-V13) X	810 / 1710	r161	26
A4H	1	0	1	0	0	1	0	0	V164''	V13+(V12-V13) X	784 / 1710	r162	26
A5H	1	0	1	0	0	1	0	1	V165''	V13+(V12-V13) X	758 / 1710	r163	26
A6H	1	0	1	0	0	1	1	0	V166''	V13+(V12-V13) X	732 / 1710	r164	26
A7H	1	0	1	0	0	1	1	1	V167''	V13+(V12-V13) X	706 / 1710	r165	26
A8H	1	0	1	0	1	0	0	0	V168''	V13+(V12-V13) X	680 / 1710	r166	26
A9H	1	0	1	0	1	0	0	1	V169''	V13+(V12-V13) X	654 / 1710	r167	26
AAH	1	0	1	0	1	0	1	0	V170''	V13+(V12-V13) X	628 / 1710	r168	26
ABH	1	0	1	0	1	0	1	1	V171''	V13+(V12-V13) X	602 / 1710	r169	26
ACH	1	0	1	0	1	1	0	0	V172''	V13+(V12-V13) X	576 / 1710	r170	28
ADH	1	0	1	0	1	1	0	1	V173''	V13+(V12-V13) X	546 / 1710	r171	28
AEH	1	0	1	0	1	1	1	0	V174''	V13+(V12-V13) X	518 / 1710	r172	28
AFH	1	0	1	0	1	1	1	1	V175''	V13+(V12-V13) X	490 / 1710	r173	28
B0H	1	0	1	1	0	0	0	0	V176''	V13+(V12-V13) X	462 / 1710	r174	28
B1H	1	0	1	1	0	0	0	1	V177''	V13+(V12-V13) X	434 / 1710	r175	28
B2H	1	0	1	1	0	0	1	0	V178''	V13+(V12-V13) X	406 / 1710	r176	28
B3H	1	0	1	1	0	0	1	1	V179''	V13+(V12-V13) X	378 / 1710	r177	28
B4H	1	0	1	1	0	1	0	0	V180''	V13+(V12-V13) X	350 / 1710	r178	28
B5H	1	0	1	1	0	1	0	1	V181''	V13+(V12-V13) X	322 / 1710	r179	28
B6H	1	0	1	1	0	1	1	0	V182''	V13+(V12-V13) X	294 / 1710	r180	28
B7H	1	0	1	1	0	1	1	1	V183''	V13+(V12-V13) X	266 / 1710	r181	28
B8H	1	0	1	1	1	0	0	0	V184''	V13+(V12-V13) X	238 / 1710	r182	28
B9H	1	0	1	1	1	0	0	1	V185''	V13+(V12-V13) X	210 / 1710	r183	28
BAH	1	0	1	1	1	0	1	0	V186''	V13+(V12-V13) X	180 / 1710	r184	30
BBH	1	0	1	1	1	0	1	1	V187''	V13+(V12-V13) X	150 / 1710	r185	30
BCH	1	0	1	1	1	1	0	0	V188''	V13+(V12-V13) X	120 / 1710	r186	30
BDH	1	0	1	1	1	1	0	1	V189''	V13+(V12-V13) X	90 / 1710	r187	30
BEH	1	0	1	1	1	1	1	0	V190''	V13+(V12-V13) X	60 / 1710	r188	30
BFH	1	0	1	1	1	1	1	1	V191''	V13+(V12-V13) X	30 / 1710	r189	30
												r190	30

★

Figure 5-3. Relationship between Input Data and Output Voltage (4/4)

0.5 V_{DD2} - 0.5 V ≥ V₈ > V₉ > V₁₀ > V₁₁ > V₁₂ > V₁₃ > V₁₄ > V₁₅ ≥ V_{SS2} + 0.2 V, POL21/22 = L

Input data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage		rn	(Ω)	
C0H	1	1	0	0	0	0	0	0	V192 ⁿ	V13			
C1H	1	1	0	0	0	0	0	1	V193 ⁿ	V14+(V13-V14) X	1936 / 1966	r191	30
C2H	1	1	0	0	0	0	1	0	V194 ⁿ	V14+(V13-V14) X	1906 / 1966	r192	30
C3H	1	1	0	0	0	0	1	1	V195 ⁿ	V14+(V13-V14) X	1876 / 1966	r193	30
C4H	1	1	0	0	0	1	0	0	V196 ⁿ	V14+(V13-V14) X	1844 / 1966	r194	32
C5H	1	1	0	0	0	1	0	1	V197 ⁿ	V14+(V13-V14) X	1812 / 1966	r195	32
C6H	1	1	0	0	0	1	1	0	V198 ⁿ	V14+(V13-V14) X	1780 / 1966	r196	32
C7H	1	1	0	0	0	1	1	1	V199 ⁿ	V14+(V13-V14) X	1748 / 1966	r197	32
C8H	1	1	0	0	1	0	0	0	V200 ⁿ	V14+(V13-V14) X	1716 / 1966	r198	32
C9H	1	1	0	0	1	0	0	1	V201 ⁿ	V14+(V13-V14) X	1684 / 1966	r199	32
CAH	1	1	0	0	1	0	1	0	V202 ⁿ	V14+(V13-V14) X	1652 / 1966	r200	32
CBH	1	1	0	0	1	0	1	1	V203 ⁿ	V14+(V13-V14) X	1620 / 1966	r201	34
CCH	1	1	0	0	1	1	0	0	V204 ⁿ	V14+(V13-V14) X	1588 / 1966	r202	34
CDH	1	1	0	0	1	1	0	1	V205 ⁿ	V14+(V13-V14) X	1556 / 1966	r203	34
CEH	1	1	0	0	1	1	1	0	V206 ⁿ	V14+(V13-V14) X	1524 / 1966	r204	34
CFH	1	1	0	0	1	1	1	1	V207 ⁿ	V14+(V13-V14) X	1492 / 1966	r205	34
DOH	1	1	0	1	0	0	0	0	V208 ⁿ	V14+(V13-V14) X	1460 / 1966	r206	34
D1H	1	1	0	1	0	0	0	1	V209 ⁿ	V14+(V13-V14) X	1428 / 1966	r207	36
D2H	1	1	0	1	0	0	1	0	V210 ⁿ	V14+(V13-V14) X	1396 / 1966	r208	36
D3H	1	1	0	1	0	0	1	1	V211 ⁿ	V14+(V13-V14) X	1364 / 1966	r209	36
D4H	1	1	0	1	0	1	0	0	V212 ⁿ	V14+(V13-V14) X	1332 / 1966	r210	36
D5H	1	1	0	1	0	1	0	1	V213 ⁿ	V14+(V13-V14) X	1300 / 1966	r211	36
D6H	1	1	0	1	0	1	1	0	V214 ⁿ	V14+(V13-V14) X	1268 / 1966	r212	38
D7H	1	1	0	1	0	1	1	1	V215 ⁿ	V14+(V13-V14) X	1236 / 1966	r213	38
D8H	1	1	0	1	1	0	0	0	V216 ⁿ	V14+(V13-V14) X	1204 / 1966	r214	38
D9H	1	1	0	1	1	0	0	1	V217 ⁿ	V14+(V13-V14) X	1172 / 1966	r215	38
DAH	1	1	0	1	1	0	1	0	V218 ⁿ	V14+(V13-V14) X	1140 / 1966	r216	40
DBH	1	1	0	1	1	0	1	1	V219 ⁿ	V14+(V13-V14) X	1108 / 1966	r217	40
DCH	1	1	0	1	1	1	0	0	V220 ⁿ	V14+(V13-V14) X	1076 / 1966	r218	40
DDH	1	1	0	1	1	1	0	1	V221 ⁿ	V14+(V13-V14) X	1044 / 1966	r219	42
DEH	1	1	0	1	1	1	1	0	V222 ⁿ	V14+(V13-V14) X	1012 / 1966	r220	42
DFH	1	1	0	1	1	1	1	1	V223 ⁿ	V14+(V13-V14) X	980 / 1966	r221	42
E0H	1	1	1	0	0	0	0	0	V224 ⁿ	V14+(V13-V14) X	948 / 1966	r222	44
E1H	1	1	1	0	0	0	0	1	V225 ⁿ	V14+(V13-V14) X	916 / 1966	r223	44
E2H	1	1	1	0	0	0	1	0	V226 ⁿ	V14+(V13-V14) X	884 / 1966	r224	44
E3H	1	1	1	0	0	0	1	1	V227 ⁿ	V14+(V13-V14) X	852 / 1966	r225	46
E4H	1	1	1	0	0	1	0	0	V228 ⁿ	V14+(V13-V14) X	820 / 1966	r226	46
E5H	1	1	1	0	0	1	0	1	V229 ⁿ	V14+(V13-V14) X	788 / 1966	r227	48
E6H	1	1	1	0	0	1	1	0	V230 ⁿ	V14+(V13-V14) X	756 / 1966	r228	48
E7H	1	1	1	0	0	1	1	1	V231 ⁿ	V14+(V13-V14) X	724 / 1966	r229	50
E8H	1	1	1	0	1	0	0	0	V232 ⁿ	V14+(V13-V14) X	692 / 1966	r230	50
E9H	1	1	1	0	1	0	0	1	V233 ⁿ	V14+(V13-V14) X	660 / 1966	r231	52
EAH	1	1	1	0	1	0	1	0	V234 ⁿ	V14+(V13-V14) X	628 / 1966	r232	52
EBH	1	1	1	0	1	0	1	1	V235 ⁿ	V14+(V13-V14) X	596 / 1966	r233	54
ECH	1	1	1	0	1	1	0	0	V236 ⁿ	V14+(V13-V14) X	564 / 1966	r234	56
EDH	1	1	1	0	1	1	0	1	V237 ⁿ	V14+(V13-V14) X	532 / 1966	r235	56
EEH	1	1	1	0	1	1	1	0	V238 ⁿ	V14+(V13-V14) X	500 / 1966	r236	58
EFH	1	1	1	0	1	1	1	1	V239 ⁿ	V14+(V13-V14) X	468 / 1966	r237	60
F0H	1	1	1	1	0	0	0	0	V240 ⁿ	V14		r238	62
F1H	1	1	1	1	0	0	0	1	V241 ⁿ	V15+(V14-V15) X	1258 / 1322	r239	64
F2H	1	1	1	1	0	0	1	0	V242 ⁿ	V15+(V14-V15) X	1192 / 1322	r240	66
F3H	1	1	1	1	0	0	1	1	V243 ⁿ	V15+(V14-V15) X	1126 / 1322	r241	68
F4H	1	1	1	1	0	1	0	0	V244 ⁿ	V15+(V14-V15) X	1060 / 1322	r242	70
F5H	1	1	1	1	0	1	0	1	V245 ⁿ	V15+(V14-V15) X	994 / 1322	r243	72
F6H	1	1	1	1	0	1	1	0	V246 ⁿ	V15+(V14-V15) X	928 / 1322	r244	76
F7H	1	1	1	1	0	1	1	1	V247 ⁿ	V15+(V14-V15) X	862 / 1322	r245	80
F8H	1	1	1	1	1	0	0	0	V248 ⁿ	V15+(V14-V15) X	796 / 1322	r246	82
F9H	1	1	1	1	1	0	0	1	V249 ⁿ	V15+(V14-V15) X	730 / 1322	r247	86
FAH	1	1	1	1	1	0	1	0	V250 ⁿ	V15+(V14-V15) X	664 / 1322	r248	92
FBH	1	1	1	1	1	0	1	1	V251 ⁿ	V15+(V14-V15) X	598 / 1322	r249	98
FCH	1	1	1	1	1	1	0	0	V252 ⁿ	V15+(V14-V15) X	532 / 1322	r250	104
FDH	1	1	1	1	1	1	0	1	V253 ⁿ	V15+(V14-V15) X	466 / 1322	r251	112
FEH	1	1	1	1	1	1	1	0	V254 ⁿ	V15+(V14-V15) X	400 / 1322	r252	120
FFH	1	1	1	1	1	1	1	1	V255 ⁿ	V15		r253	132
											TOTAL	10280	

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 8 bits x 2 RGBs (6 dots)

Input width: 48 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

(2) R,/L = L (Left shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

POL	S _{2n-1} ^{Note}	S _{2n} ^{Note}
L	V ₀ to V ₇	V ₈ to V ₁₅
H	V ₈ to V ₁₅	V ₀ to V ₇

Note S_{2n-1} (Odd output), S_{2n} (Even output), n = 1, 2, ..., 192.

7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM

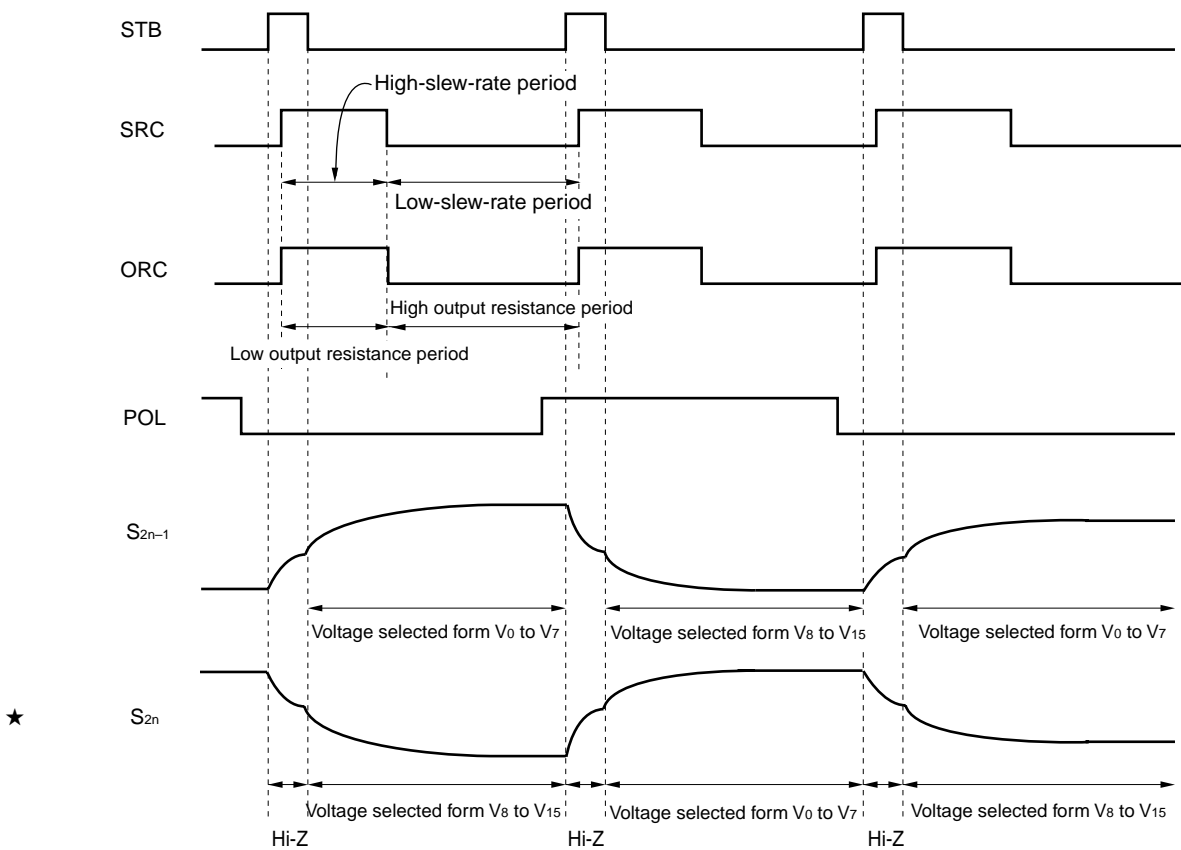
When the MODE pin is high level or left open and STB is high level, all outputs are reset (shorted) and the gray-scale voltage is output to LCD in synchronization with the falling edge of STB.

When the MODE pin is low level and STB is high level, all outputs became Hi-Z and the gray-scale voltage is output to the LCD in synchronization with the falling edge of STB.

Also, setting the SRC pin to high level allows the bias current value of the output amplifier to rise temporarily, and setting the ORC pin to high level allows the output resistance value of the amplifier to lower temporarily.

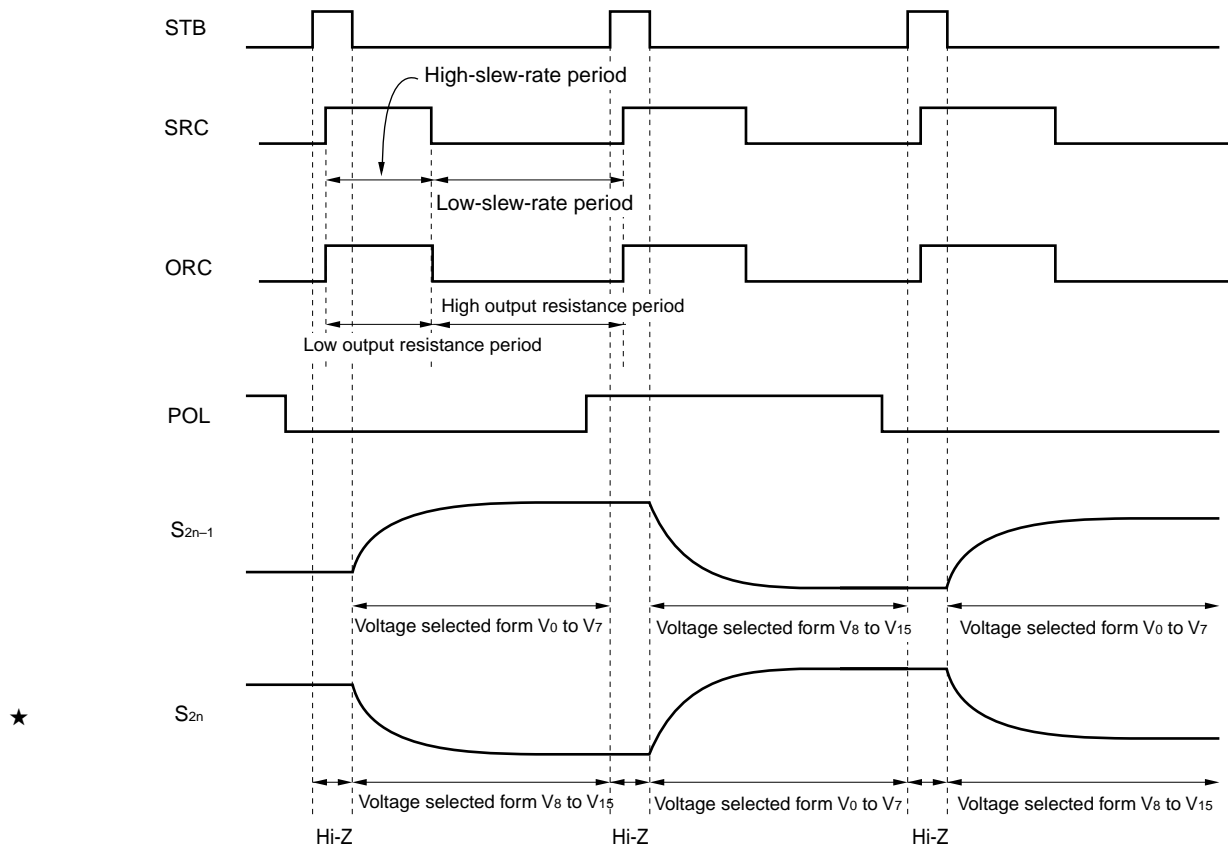
For the timing and the processing of STB, SRC, or ORC during a high-level period, We recommend a thorough evaluation of the LCD panel specifications in advance.

(1) When MODE is high level or left open



★

(2) When MODE is low level



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic part supply voltage	V _{DD1}	-0.5 to +4.0	V
Driver part supply voltage	V _{DD2}	-0.5 to +17.0	V
Logic part input voltage	V _{I1}	-0.5 to V _{DD1} + 0.5	V
Driver part input voltage	V _{I2}	-0.5 to V _{DD2} + 0.5	V
Logic part output voltage	V _{O1}	-0.5 to V _{DD1} + 0.5	V
Driver part output voltage	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Operating ambient temperature	T _A	-10 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Logic part supply voltage	V _{DD1}		2.5		3.4	V
★ Driver part supply voltage	V _{DD2}	V _{SEL} = H	12.5	13.0	13.5	V
		V _{SEL} = L or open	14.5	15.0	15.5	
High-level input voltage	V _{IH}		0.7 V _{DD1}		V _{DD1}	V
Low-level input voltage	V _{IL}		0		0.3 V _{DD1}	V
★ γ-corrected voltage	V ₀ to V ₇		0.5 V _{DD2} +0.5		V _{DD2} -0.2	V
	V ₈ to V ₁₅		0.2		0.5 V _{DD2} -0.5	V
Driver part output voltage	V _O		0.2		V _{DD2} -0.2	V
★ Clock frequency	f _{CLK}	2.5 V ≤ V _{DD1} ≤ 3.0 V			55	MHz
		3.0 V ≤ V _{DD1} ≤ 3.4 V			70	MHz

★ **Electrical Characteristics (T_A = -10 to +75°C, V_{DD1} = 2.5 to 3.4 V, V_{DD2} = 12.5 to 15.5 V, V_{SS1} = V_{SS2} = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input leakage current	I _{IL}				±1.0	μA	
High-level output voltage	V _{OH}	STHR (STHL), I _{OH} = 0 mA	V _{DD1} -0.1			V	
Low-level output voltage	V _{OL}	STHR (STHL), I _{OL} = 0 mA			0.1	V	
★ γ-corrected power supply static current consumption	I _γ	V _{DD2} = 15.0 V	V ₀ , V ₈	340	681	1020	mA
		V ₀ to V ₇ = V ₈ to V ₁₅ = 7.0 V	V ₇ , V ₁₅	-1020	-681	-340	mA
★ Driver output current	I _{VOH}	V _X = 12 V, V _{OUT} = 11 V Note			-0.40	mA	
	I _{VOL}	V _X = 1 V, V _{OUT} = 2 V Note	0.65			mA	
★ Output voltage deviation	ΔV _O	T _A = 25°C V _{SS2} + 1.0 V to V _{DD2} - 1.0 V		±10	±20	mV	
★ Output swing voltage difference deviation	ΔV _{P-P1}	V _{DD1} = 3.3 V V _{DD2} = 15.0 V	V _{OUT} = 7.0 to 8.0 V Note		±5	±10	mV
	ΔV _{P-P2}	T _A = 25°C	V _{OUT} = 4.0 to 11.0 V Note		±7	±15	mV
	ΔV _{P-P3}		V _{OUT} = 1.0 to 14.0 V Note		±10	±20	mV
★ Logic part dynamic current consumption	I _{DD1}	V _{DD1}		1.3	10	mA	
★ Driver part dynamic current consumption	I _{DD2}	V _{DD2} , with no load		12	30	mA	

Note V_X refers to the output voltage of analog output pins S₁ to S₃₈₄.

V_{OUT} refers to the voltage applied to analog output pins S₁ to S₃₈₄.

Cautions 1. f_{STB} = 64 kHz, f_{CLK} = 54 MHz

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
3. Refers to the current consumption per driver when cascades are connected under the assumption of SXGA single-sided mounting (10 units).

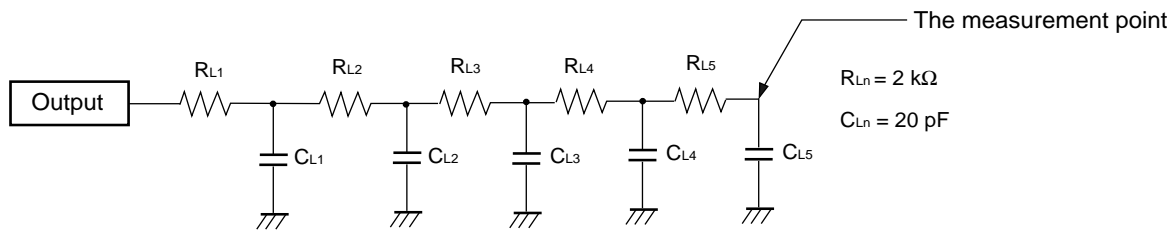
★ **Switching Characteristics** ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 2.5$ to 3.4 V, $V_{DD2} = 12.5$ to 15.5 V, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	$C_L = 15$ pF			12	ns
★ Driver output delay time	t_{PLH2} Note	$C_L = 100$ pF, $R_L = 10$ kΩ			5	μs
	t_{PLH3} Note				10	μs
	t_{PHL2} Note				5	μs
	t_{PHL3} Note				10	μs
Input capacitance	C_{i1}	logic input, except STHR (STHL), $T_A = 25^\circ\text{C}$		5	10	pF
	C_{i2}	STHR (STHL), $T_A = 25^\circ\text{C}$		10	15	pF

Note t_{PLH2} , t_{PHL2} refer to the arrival time from falling edge of STB to target voltage $\pm 10\%$

t_{PLH3} , t_{PHL3} refer to the arrival time from falling edge of STB to target voltage ± 0.02 V (condition: $V_O = 3.0$ V $\leftrightarrow 12.0$ V)

★ **Test Condition**



★ Timing Requirements ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 2.5$ to 3.4 V, $V_{SS1} = 0$ V, $t_r = t_f = 5.0$ ns)

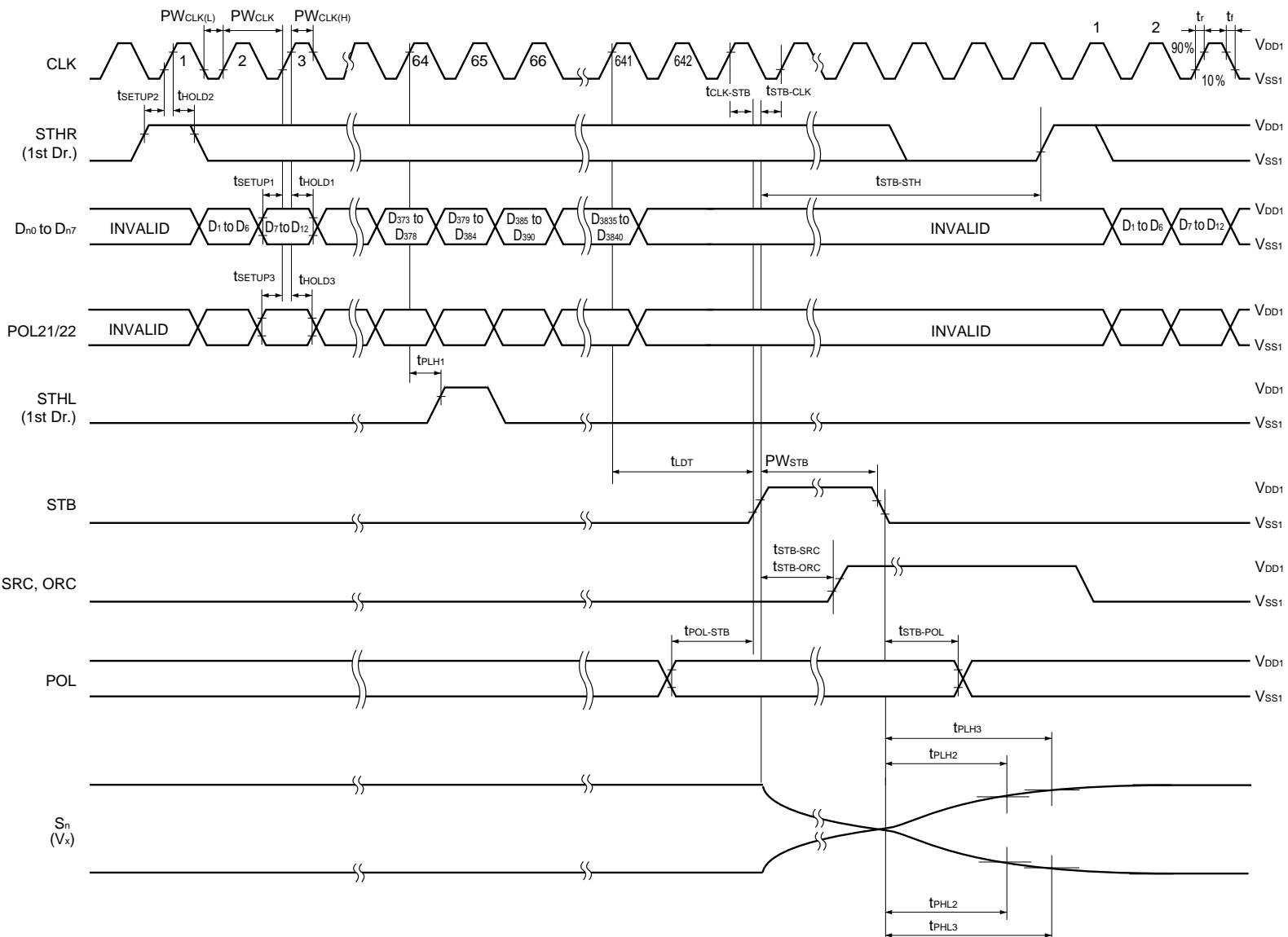
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Clock pulse width	PW_{CLK}	$2.5\text{ V} \leq V_{DD1} \leq 3.0\text{ V}$	18			ns
		$3.0\text{ V} \leq V_{DD1} \leq 3.4\text{ V}$	14			
★ Clock pulse high period	$PW_{CLK(H)}$	$2.5\text{ V} \leq V_{DD1} \leq 3.0\text{ V}$	6			ns
		$3.0\text{ V} \leq V_{DD1} \leq 3.4\text{ V}$	4			
Clock pulse low period	$PW_{CLK(L)}$		4			ns
Data setup time	t_{SETUP1}		0			ns
Data hold time	t_{HOLD1}		4			ns
Start pulse setup time	t_{SETUP2}		0			ns
Start pulse hold time	t_{HOLD2}		4			ns
POL21/22 setup time	t_{SETUP3}		0			ns
POL21/22 hold time	t_{HOLD3}		4			ns
★ STB pulse width	PW_{STB}		1.0			μs
Last data timing	t_{LDT}		2			CLK
CLK-STB time	$t_{CLK-STB}$	CLK $\uparrow \rightarrow$ STB \uparrow	4			ns
STB-CLK time	$t_{STB-CLK}$	STB $\uparrow \rightarrow$ CLK \uparrow	4			ns
Time between STB and start pulse	$t_{STB-STH}$	STB $\uparrow \rightarrow$ STHR (STHL) \uparrow	2			CLK
POL-STB time	$t_{POL-STB}$	POL \uparrow or $\downarrow \rightarrow$ STB \uparrow	4			ns
STB-POL time	$t_{STB-POL}$	STB $\downarrow \rightarrow$ POL \downarrow or \uparrow	4			ns
STB-SRC time	$t_{STB-SRC}$	STB $\uparrow \rightarrow$ SRC \uparrow	0			ns
STB-ORC time	$t_{STB-ORC}$	STB $\downarrow \rightarrow$ ORC \uparrow	0			ns

★ **Remark** Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.

Switching Characteristic Waveform

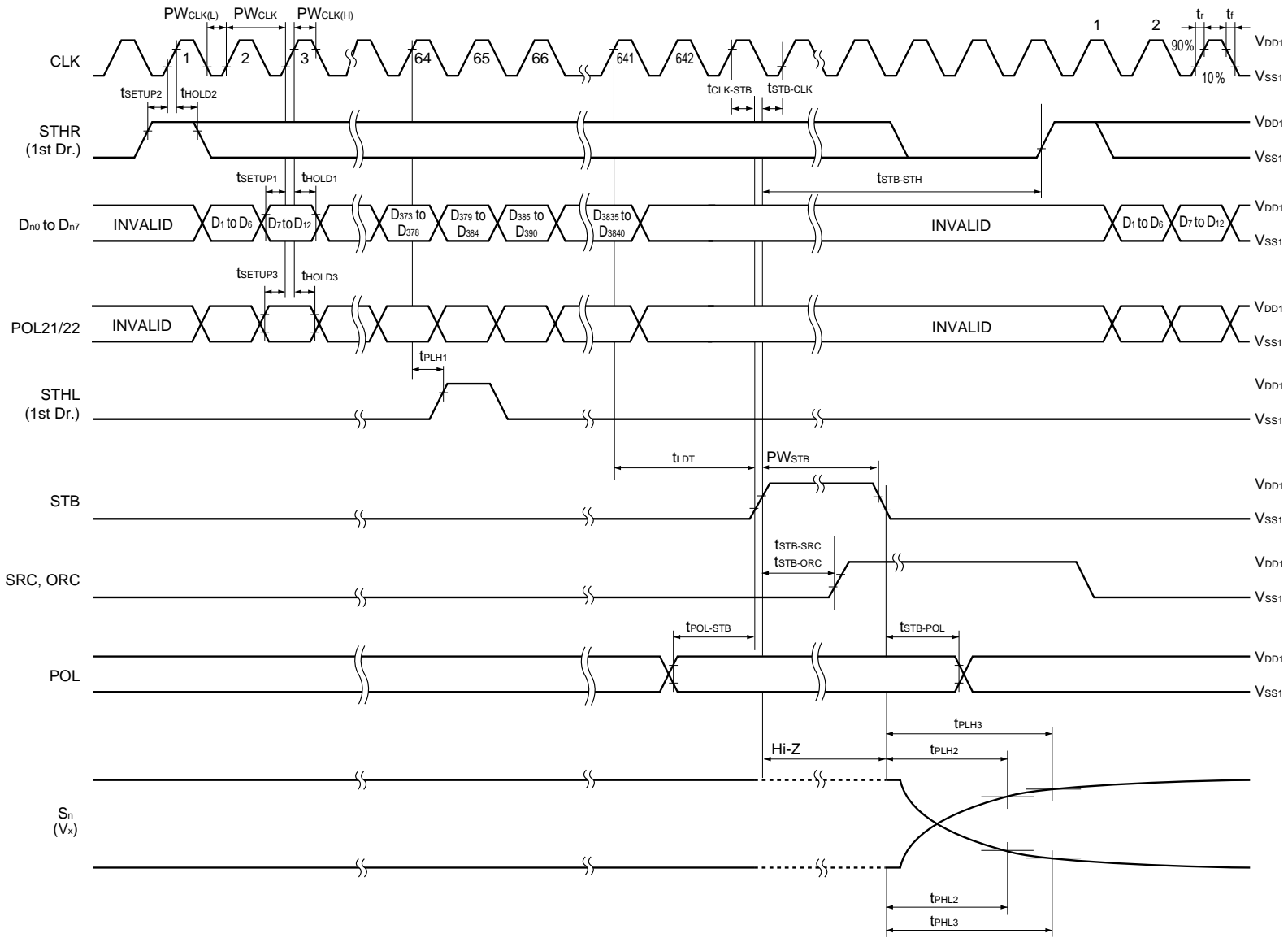
★ (1) R/L=H, MODE = H or open

Unless otherwise specified, V_{IH} , V_{IL} are defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$ (Numbers clock and display data are example when in SXGA).



★ (2) R_L/L = H, MODE = L

Unless otherwise specified, V_H, V_L are defined to be V_H = 0.7 V_{DD1}, V_L = 0.3 V_{DD1} (Numbers clock and display data are example when in SXGA).



9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16721.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16721N-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).
	ACF (Adhesive Conductive Film)	Temporaly bonding 70 to 100°C, pressure 3 to 8 kg/cm ² , time 3 to 5 sec. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm ² , time 30 to 40 sec (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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