NEC

MOS INTEGRATED CIRCUIT

μPD30200, 30210

VR4300™, VR4305™, VR4310™
64-BIT MICROPROCESSOR

DESCRIPTION

The μPD30200-100, 30200-133 (VR4300), 30200-80 (VR4305), and 30210 (VR4310) are high-performance, 64-bit RISC (Reduced Instruction Set Computer) type VR Series™ microprocessors employing the RISC architecture developed by MIPS™ Technologies Inc.

The VR4300, VR4305, and VR4310 are intended for the high-performance embedded device field and have 32-bit system interface buses.

Detailed function descriptions are provided in the following user's manual. Be sure to read this manual before designing.

- **VR4300, VR4305, VR4310 User's Manual (U10504E)**

FEATURES

- Employs 64-bit RISC MIPS architecture
- High-speed operation processing
  - 5-stage pipeline processing
  - High-speed execution of integer and floating-point operations
  - 48 SPECint92, 36 SPECfp92, 106 MIPS, at 80 MHz operation (μPD30200-80)
    60 SPECint92, 45 SPECfp92, 131 MIPS, at 100 MHz operation (μPD30200-100)
    80 SPECint92, 60 SPECfp92, 177 MIPS at 133 MHz operation (μPD30200-133, μPD30210-133)
    100 SPECint92, 75 SPECfp92, 221 MIPS at 167 MHz operation (μPD30210-167)
- Instruction set compatible with VR4000™ Series (conforms to MIPS-I/II/III)
- On-chip cache memory (Instruction: 16 Kbytes, Data: 8 Kbytes)
- 32-bit address/data multiplexed bus facilitating system design
- Low power consumption
  - μPD30200-80: 1.5 W (TYP.) (at 80 MHz operation)
  - μPD30200-100, 30200-133: 1.8 W (TYP.) (at 100 MHz operation), 2.4 W (TYP.) (at 133 MHz operation)
  - μPD30210-×××: 1.9 W (TYP.) (at 133 MHz operation), 2.4 W (TYP.) (at 167 MHz operation)
- Supply voltage: 3.3 ± 0.3 V (μPD30200-80, 30200-100), 3.0 to 3.5 V (μPD30200-133, 30210-×××)

Unless otherwise specified, the VR4300 (μPD30200) is treated as the representative model throughout this document.

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The mark ★ shows major revised points.

APPLICATIONS

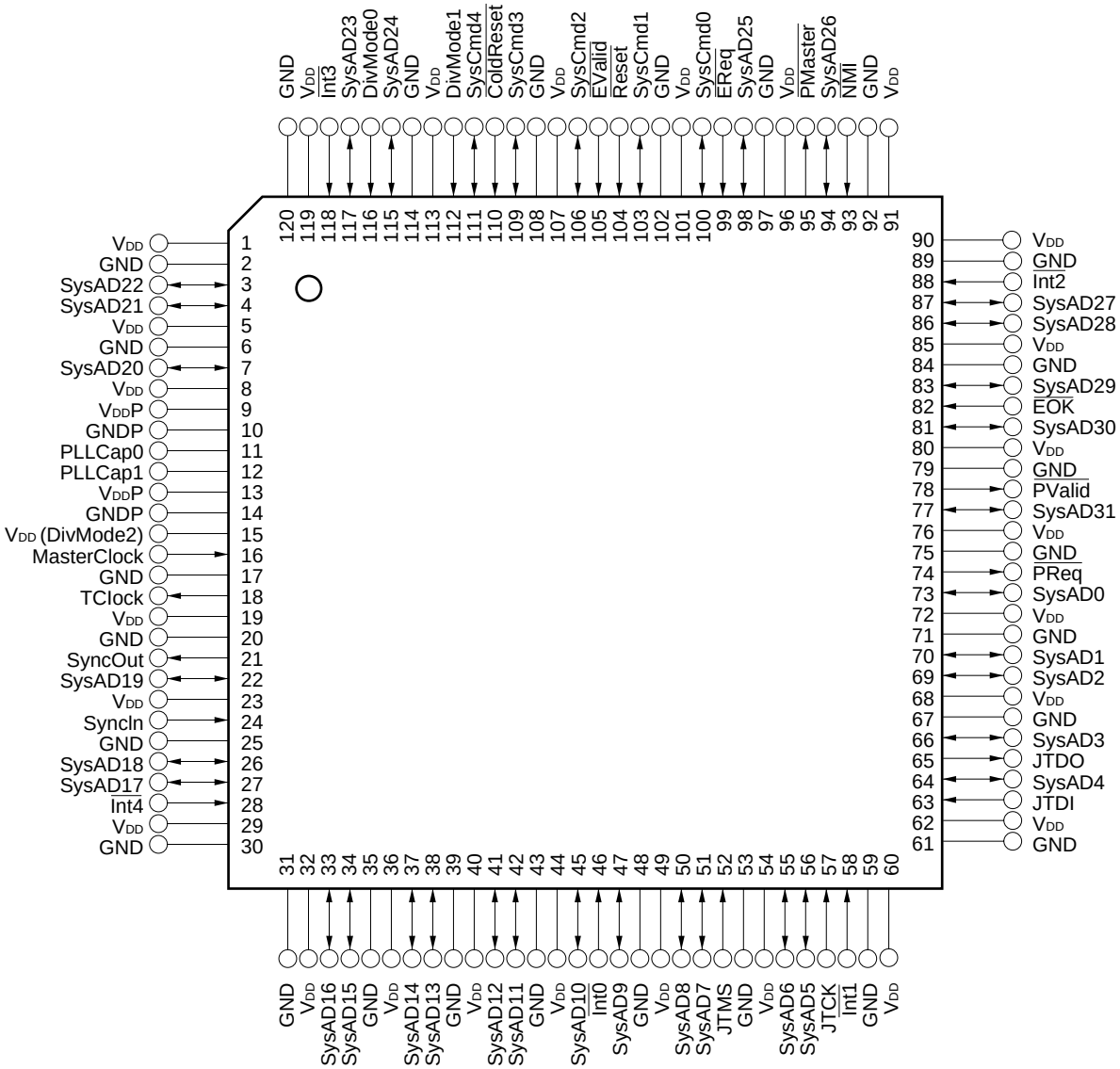
- Embedded controllers
- Page printer controllers
- Amusement game machines, etc.

ORDERING INFORMATION

Part Number	Package	Maximum Internal Operating Frequency (MHz)
μPD30200GD-80-LBB	120-pin plastic QFP (28 × 28)	80
μPD30200GD-100-MBB	120-pin plastic QFP (28 × 28)	100
μPD30200GD-133-MBB	120-pin plastic QFP (28 × 28)	133
μPD30210GD-133-MBB	120-pin plastic QFP (28 × 28)	133
μPD30210GD-167-MBB	120-pin plastic QFP (28 × 28)	167

PIN CONFIGURATION (Top View)

- 120-pin plastic QFP (28 × 28)
  μPD30200GD-80-LBB
  μPD30200GD-100-MBB
  μPD30200GD-133-MBB
  μPD30210GD-133-MBB
  μPD30210GD-167-MBB



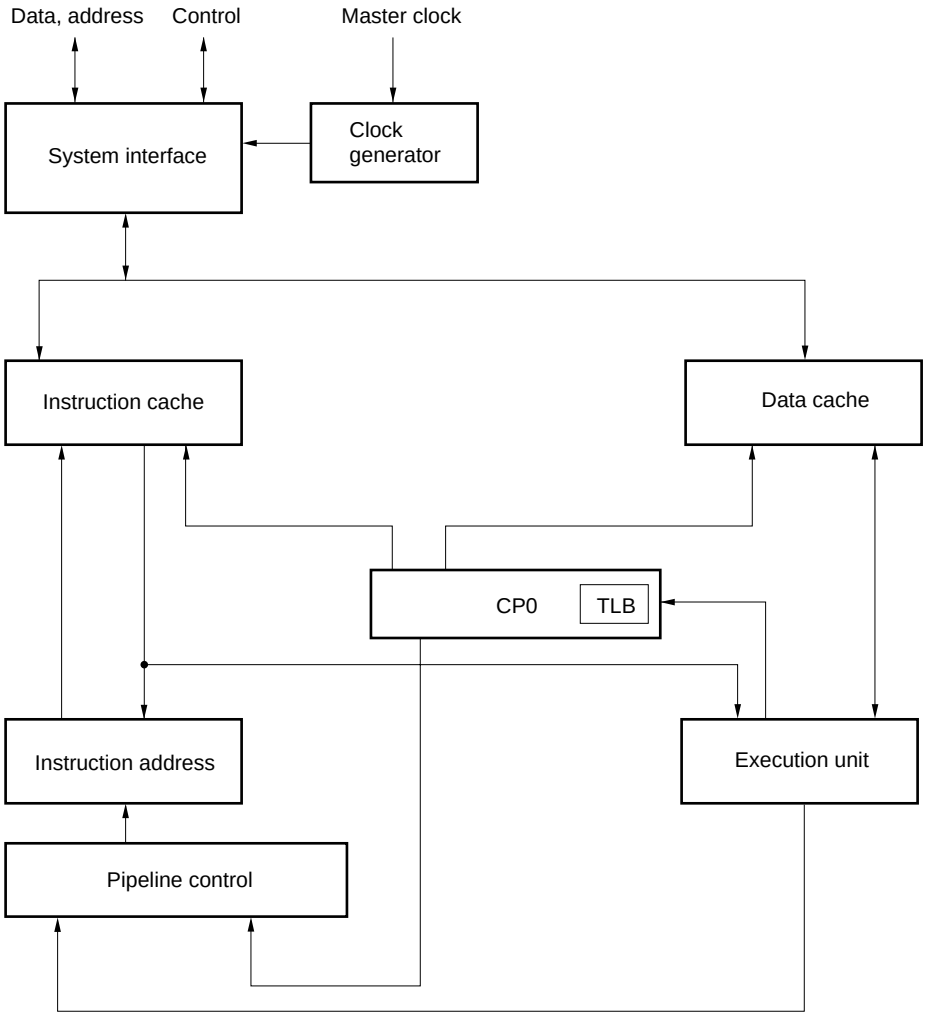
Remark ( ): Pin name in the μPD30210-×××

PIN NAMES

$\overline{\text{ColdReset}}$:	Cold Reset
DivMode (1:0)[Note]:	Divide Mode
$\overline{\text{EOK}}$:	External OK
$\overline{\text{EReq}}$:	External Request
$\overline{\text{EValid}}$:	External Valid
$\overline{\text{Int(4:0)}}$:	Interrupt Request
JTCK:	JTAG Clock Input
JTDI:	JTAG Data In
JTDO:	JTAG Data Out
JTMS:	JTAG Command Signal
MasterClock:	Master Clock
$\overline{\text{NMI}}$:	Non-maskable Interrupt Request
PLLCap (1:0):	Phase Locked Loop Capacitance
$\overline{\text{PMaster}}$:	Processor Master
$\overline{\text{PReq}}$:	Processor Request
$\overline{\text{PValid}}$:	Processor Valid
$\overline{\text{Reset}}$:	Reset
SyncIn:	Synchronization Clock Input
SyncOut:	Synchronization Clock Output
SysAD(31:0):	System Address/Data Bus
SysCmd (4:0):	System Command/Data ID Bus
TClock:	Transmit Clock
V_{DD}:	Power Supply
GND:	Ground
V_{DD}P:	V_{DD} for PLL
GNDP:	GND for PLL

Note In the μPD30200-×××. DivMode (2:0) in the μPD30210-×××.

INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Pin Name	I/O	Function
SysAD (31:0)	I/O	System address/data bus. 32-bit bus for communication between processor and external agent.
SysCmd (4:0)	I/O	System command/data ID bus. 5-bit bus for communication of commands and data identifiers between processor and external agent.
$\overline{\text{EValid}}$	Input	External valid. Signal indicating that external agent has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{PValid}}$	Output	Processor valid. Signal indicating that processor has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{EReq}}$	Input	External request. Signal used by external agent to request use of system interface.
$\overline{\text{PReq}}$	Output	Processor request. Signal used by processor to request use of system interface. If the processor detects a protocol error, this signal oscillates with the same frequency as SClock (internal), and the system interface hangs up.
$\overline{\text{PMaster}}$	Output	Processor master. Signal indicating processor controls system interface.
$\overline{\text{EOK}}$	Input	External OK. Signal indicating that external agent can accept processor request.
$\overline{\text{Int (4:0)}}$	Input	Interrupt. General-purpose processor interrupt requests, the input status of which can be confirmed by bits 14 through 10 of cause register.
$\overline{\text{NMI}}$	Input	Non-maskable interrupt. Interrupt request that cannot be masked.
$\overline{\text{ColdReset}}$	Input	Cold reset. Signal that initializes internal status of processor. It can be made active/inactive without synchronizing with the MasterClock.
$\overline{\text{Reset}}$	Input	Reset. Signal that generates reset exception without initializing internal status of processor.
MasterClock	Input	Master clock. Clock input signal to processor.
TClock	Output	Transmit-receive signal clock This is the basic clock for the system interface and is synchronized with the MasterClock.
SyncOut	Output	Synchronization clock output. Output of synchronization clock.
SyncIn	Input	Synchronization clock input. Input of synchronization clock.
JTDI	Input	JTAG data input. Input of JTAG serial data.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>JTDO</td><td>Output</td><td>JTAG data output.
Output of JTAG serial data.</td></tr>
<tr><td>JTMS</td><td>Input</td><td>JTAG command.
Indicates that input serial data is command data.</td></tr>
<tr><td>JTCK</td><td>Input</td><td>JTAG clock input.
Input of JTAG serial clock. If the JTAG interface is not used, set it to low level.</td></tr>
<tr><td>DivMode</td><td>Input</td><td>Mode setting.
Sets frequency ratio of MasterClock, TClock, and PClock.
• DivMode (1:0) (VR4300)
Example
<table>
<tr><th>DivMode (1:0)</th><th>MasterClock</th><th>PClock</th><th>TClock</th><th>Ratio</th><th></th></tr>
<tr><td>00</td><td>33.3 MHz</td><td>133 MHz</td><td>33.3 MHz</td><td>1:4:1</td><td>Note 1</td></tr>
<tr><td>01</td><td>66.7 MHz</td><td>100.0 MHz</td><td>66.7 MHz</td><td>2:3:2</td><td>Note 2</td></tr>
<tr><td>10</td><td>50.0 MHz</td><td>100.0 MHz</td><td>50.0 MHz</td><td>1:2:1</td><td></td></tr>
<tr><td>11</td><td>33.3 MHz</td><td>100.0 MHz</td><td>33.3 MHz</td><td>1:3:1</td><td></td></tr>
</table>
Notes 1. This setting is allowed with the 133 MHz model only. With the 100 MHz model, this setting is reserved.
2. This setting is allowed with the 100 MHz model only. With the 133 MHz model, this setting is reserved.

• DivMode (1:0) (VR4305)
Example
<table>
<tr><th>DivMode (1:0)</th><th>MasterClock</th><th>PClock</th><th>TClock</th><th>Ratio</th></tr>
<tr><td>00</td><td>66.7 MHz</td><td>66.7 MHz</td><td>66.7 MHz</td><td>1:1:1</td></tr>
<tr><td>01</td><td>–</td><td>–</td><td>–</td><td>Reserved</td></tr>
<tr><td>10</td><td>40 MHz</td><td>80 MHz</td><td>40 MHz</td><td>1:2:1</td></tr>
<tr><td>11</td><td>20 MHz</td><td>60 MHz</td><td>20 MHz</td><td>1:3:1</td></tr>
</table>
• DivMode (2:0) (VR4310)
Example
<table>
<tr><th>DivMode (2:0)</th><th>MasterClock</th><th>PClock</th><th>TClock</th><th>Ratio</th><th></th></tr>
<tr><td>000</td><td>26.7 MHz</td><td>133 MHz</td><td>26.7 MHz</td><td>1:5:1</td><td></td></tr>
<tr><td>001</td><td>22.2 MHz</td><td>133 MHz</td><td>22.2 MHz</td><td>1:6:1</td><td></td></tr>
<tr><td>010</td><td>66.7 MHz</td><td>167 MHz</td><td>66.7 MHz</td><td>2:5:2</td><td>Note</td></tr>
<tr><td>011</td><td>33.3 MHz</td><td>100 MHz</td><td>33.3 MHz</td><td>1:3:1</td><td></td></tr>
<tr><td>100</td><td>33.3 MHz</td><td>133 MHz</td><td>33.3 MHz</td><td>1:4:1</td><td></td></tr>
<tr><td>101</td><td>–</td><td>–</td><td>–</td><td>Reserved</td><td></td></tr>
<tr><td>110</td><td>50.0 MHz</td><td>100 MHz</td><td>50.0 MHz</td><td>1:2:1</td><td></td></tr>
<tr><td>111</td><td>33.3 MHz</td><td>100 MHz</td><td>33.3 MHz</td><td>1:3:1</td><td></td></tr>
</table>
Note This setting is allowed with the 167 MHz model only. With the 133 MHz model, this setting is reserved.

After power application, do not change the value of these pins; otherwise the operation is not guaranteed.</td></tr>
<tr><td>PLLCap (1:0)</td><td>–</td><td>PLL capacitor.
Connect capacitor to adjust internal PLL.</td></tr>
<tr><td>VDDP</td><td>–</td><td>PLL VDD.
Power supply for internal PLL.</td></tr>
<tr><td>GNDP</td><td>–</td><td>PLL GND.
Ground for internal PLL.</td></tr>
<tr><td>VDD</td><td>–</td><td>Positive power supply pin.</td></tr>
<tr><td>GND</td><td>–</td><td>Ground pin.</td></tr>
</table>

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +4.0	V
Input voltage[Note]	V_I		–0.5 to V_{DD} + 0.3	V
		Pulse of less than 10 ns	–1.5 to V_{DD} + 0.3	V
Operating case temperature	T_C		0 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note The upper limit of the input voltage (V_{DD} + 0.3) is +4.0 V.

Cautions 1. Do not short circuit two or more outputs at the same time.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics are the range within which the product can normally operate and the quality can be guaranteed.

DC Characteristics (T_C = 0 to +85°C, V_{DD} = 3.3 ±0.3 V): μPD30200-80, 30200-100
(T_C = 0 to +85°C, V_{DD} = 3.0 to 3.5 V): μPD30200-133, 30210-×××

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Output voltage, high	V_{OH}	I_{OH} = –400 μA		2.4		V
Output voltage, high[Note 1]	V_{OHC}	I_{OH} = –400 μA		2.7		V
Output voltage, low	V_{OL}	I_{OL} = 2.5 mA			0.4	V
Input voltage, high	V_{IH}			2.0	V_{DD} + 0.3	V
Input voltage, low	V_{IL}			–0.5	+0.8	V
		Pulse of less than 10 ns		–1.5	+0.8	V
Input voltage, high[Note 2]	V_{IHC}			0.8V_{DD}	V_{DD} + 0.3	V
Input voltage, low[Note 2]	V_{ILC}			–0.5	0.2V_{DD}	V
		Pulse of less than 10 ns		–1.5	0.2V_{DD}	V
Supply current	I_{DD}	μPD30200	at 80 MHz operation		0.60	A
			at 100 MHz operation		0.67	A
			at 133 MHz operation		0.90	A
		μPD30210	at 133 MHz operation		0.69	A
			at 167 MHz operation		0.85	A
Input leakage current, high	I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low	I_{LIL}	V_I = 0 V			–10	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}			20	μA
Output leakage current, low	I_{LOL}	V_O = 0 V			–20	μA

Notes 1. Applied to the TClock pin.

2. Applied to the MasterClock pin only.

Remark The operating supply current is almost proportional to the operating clock frequency.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{In}	f_C = 1 MHz		10	pF
Output capacitance	C_{out}	Unmeasured pins returned to 0 V.		10	pF

AC Characteristics (T_C = 0 to +85°C, V_{DD} = 3.3 ±0.3 V): μPD30200-80, 30200-100
(T_C = 0 to +85°C, V_{DD} = 3.0 to 3.5 V): μPD30200-133, 30210-×××

Clock Parameters

(1) μPD30200-×××

Parameter	Symbol	Conditions	μPD30200-80		μPD30200-100		μPD30200-133		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Master clock high-level width	$t_{MCkHigh}$		3.5		3.5		3.5		ns
Master clock low-level width	t_{MCkLow}		3.5		3.5		3.5		ns
Master clock frequency[Note]		DivMode = 1:1	20	66.7	–	–	–	–	MHz
		DivMode = 1:2	20	66.7	20	66.7	34	66.7	MHz
		DivMode = 2:3	–	–	20	66.7	–	–	MHz
		DivMode = 1:3	20	66.7	20	66.7	24	66.7	MHz
		DivMode = 1:4	–	–	–	–	20	66.7	MHz
Master clock cycle	t_{MCkP}	DivMode = 1:1	15	50	–	–	–	–	ns
		DivMode = 1:2	15	50	15	50	15	29	ns
		DivMode = 2:3	–	–	15	50	–	–	ns
		DivMode = 1:3	15	50	15	50	15	41	ns
		DivMode = 1:4	–	–	–	–	15	50	ns
Clock jitter	$t_{MCJitter}$			±500		±500		±500	ps
Master clock rise time	t_{MCRise}			4.0		4.0		4.0	ns
Master clock fall time	t_{MCFall}			4.0		4.0		4.0	ns
JTAG clock cycle	$t_{JTAGCkP}$		4 × t_{MCkP}		4 × t_{MCkP}		4 × t_{MCkP}		ns

Note The operation of the internal PLL of the μPD30200-××× is guaranteed. The RP mode is supported only by μPD30200-80 and 30200-100 and guaranteed when the master clock frequency is 40 MHz or higher.

(2) μPD30210-×××

Parameter	Symbol	Conditions	μPD30210-133		μPD30210-167		Unit
			MIN.	MAX.	MIN.	MAX.	
Master clock high-level width	$t_{MCkHigh}$		3.5		3.5		ns
Master clock low-level width	t_{MCkLow}		3.5		3.5		ns
Master clock frequency[Note]		DivMode = 2.0	50	66.7	50	83.3	MHz
		DivMode = 2.5	–	–	40	66.7	MHz
		DivMode = 3.0	33.3	44.4	33.3	55.6	MHz
		DivMode = 4.0	25	33.3	25	41.7	MHz
		DivMode = 5.0	20	26.7	20	33.3	MHz
		DivMode = 6.0	20	22.2	20	27.8	MHz
★ Master clock cycle	t_{MCkP}	DivMode = 2.0	15	20	12	20	ns
		DivMode = 2.5	–	–	15	25	ns
		DivMode = 3.0	22	30	18	30	ns
		DivMode = 4.0	30	40	24	40	ns
		DivMode = 5.0	37	50	30	50	ns
		DivMode = 6.0	45	50	36	50	ns
Clock jitter	$t_{MCJitter}$			±500		±500	ps
Master clock rise time	t_{MCRise}			4.0		4.0	ns
Master clock fall time	t_{MCFall}			4.0		4.0	ns
JTAG clock cycle	$t_{JTAGCkP}$		$4 \times t_{MCkP}$		$4 \times t_{MCkP}$		ns

Note The operation of the internal PLL of the μPD30210-××× is guaranteed. The RP mode is not supported by the μPD30210-×××.

System Interface Parameters

(1) μPD30200-80 (T_C = 0 to 85°C, V_{DD} = 3.3 ±0.3 V)

Parameter	Symbol	Conditions	At 66.7 MHz Input[Note 3]		At 40 MHz Input[Note 3]		At 33.3 MHz Input[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		ns
Clock rise time[Note 2]	t_{CORise}	C_L = 50 pF		4.0		4.0		4.0	ns
Clock fall time[Note 2]	t_{COFall}			4.0		4.0		4.0	ns
Clock high-level width[Note 2]	t_{COHigh}		3.5		8.5		11.0		ns
Clock low-level width[Note 2]	t_{COLow}		3.5		8.5		11.0		ns

Notes 1. Applied to all interface pins.

2. Applied to TClock pin.

3. Master clock frequency (example)

(2) μPD30200-100 (T_C = 0 to 85°C, V_{DD} = 3.3 ±0.3 V)

Parameter	Symbol	Condition	At 66.7 MHz Input[Note 4]		At 62.5 MHz Input[Note 4]		At 50 MHz Input[Note 4]		At 33.3 MHz Input[Note 4]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		1.5		ns
Mode data setup time[Note 2]	t_{MDS}		3.5		3.5		3.5		3.5		ns
Clock rise time[Note 3]	t_{CORise}	C_L = 50 pF		4.0		4.0		4.0		4.0	ns
Clock fall time[Note 3]	t_{COFall}			4.0		4.0		4.0		4.0	ns
Clock high-level width[Note 3]	t_{COHigh}		3.5		4.0		6.0		11.0		ns
Clock low-level width[Note 3]	t_{COLow}		3.5		4.0		6.0		11.0		ns

Notes 1. Applied to all interface pins (except DivMode (1:0) pin).
2. Applied to DivMode (1:0) pin.
3. Applied to TClock pin.
4. Master clock frequency (example)

(3) μPD30200-133 (T_C = 0 to 85°C, V_{DD} = 3.0 to 3.5 V)

Parameter	Symbol	Conditions	At 66.7 MHz Input[Note 4]		At 44.4 MHz Input[Note 4]		At 33.3 MHz Input[Note 4]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		ns
Mode data setup time[Note 2]	t_{MDS}		3.5		3.5		3.5		ns
Clock rise time[Note 3]	t_{CORise}	C_L = 50 pF		4.0		4.0		4.0	ns
Clock fall time[Note 3]	t_{COFall}			4.0		4.0		4.0	ns
Clock high-level width[Note 3]	t_{COHigh}		3.5		7.2		11.0		ns
Clock low-level width[Note 3]	t_{COLow}		3.5		7.2		11.0		ns

Notes 1. Applied to all interface pins (except DivMode (1:0) pin).
2. Applied to DivMode (1:0) pin.
3. Applied to TClock pin.
4. Master clock frequency (example)

(4) μPD30210-133 (T_C = 0 to 85°C, V_{DD} = 3.0 to 3.5 V)

Parameter	Symbol	Conditions	At 66.7 MHz Input[Note 3]		At 33.3 MHz Input[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	2.0	8.0	2.0	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		ns
Clock rise time[Note 2]	t_{CORise}	C_L = 50 pF		4.0		4.0	ns
Clock fall time[Note 2]	t_{COFall}			4.0		4.0	ns
Clock high-level width[Note 2]	t_{COHigh}		3.5		11.0		ns
Clock low-level width[Note 2]	t_{COLow}		3.5		11.0		ns

Notes 1. Applied to all interface pins.
2. Applied to TClock pin.
3. Master clock frequency (example)

★ **(5) μPD30210-167 (T_C = 0 to 85°C, V_{DD} = 3.0 to 3.5 V)**

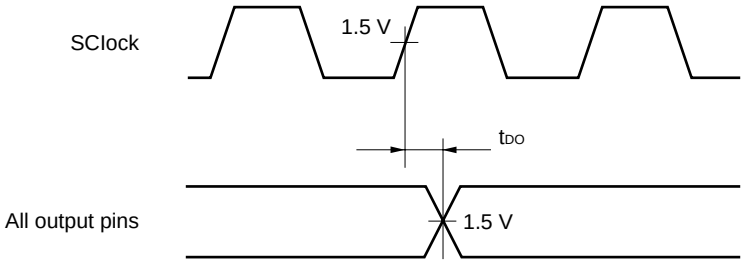
Parameter	Symbol	Conditions	At 83.3 MHz Input[Note 3]		At 66.7 MHz Input[Note 3]		At 33.3 MHz Input[Note 3]		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data output delay time[Note 1]	t_{DO}	C_L = 50 pF	1.5	8.0	1.5	8.0	1.5	8.0	ns
Data setup delay time[Note 1]	t_{DS}		3.5		3.5		3.5		ns
Data hold delay time[Note 1]	t_{DH}		1.5		1.5		1.5		ns
Clock rise time[Note 2]	t_{CORise}	C_L = 50 pF		2.5		4.0		4.0	ns
Clock fall time[Note 2]	t_{COFall}			2.5		4.0		4.0	ns
Clock high-level width[Note 2]	t_{COHigh}		3.5		3.5		11.0		ns
Clock low-level width[Note 2]	t_{COLow}		3.5		3.5		11.0		ns

Notes 1. Applied to all interface pins.
2. Applied to TClock pin.
3. Master clock frequency (example)

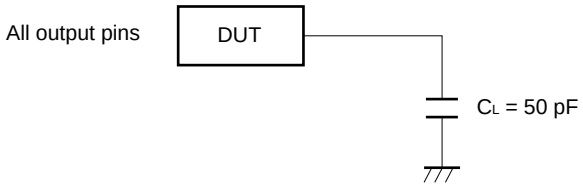
Load Coefficient

Parameter	Symbol	Conditions	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			2	ns/25 pF

Test Conditions

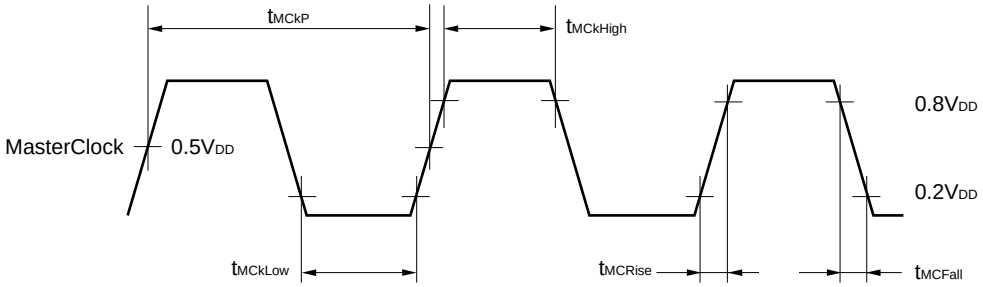


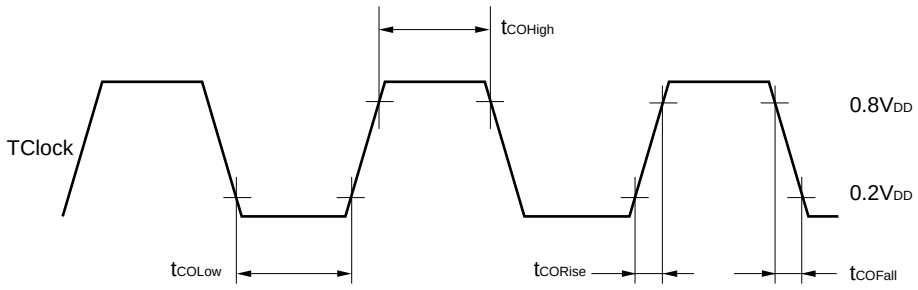
Test Load



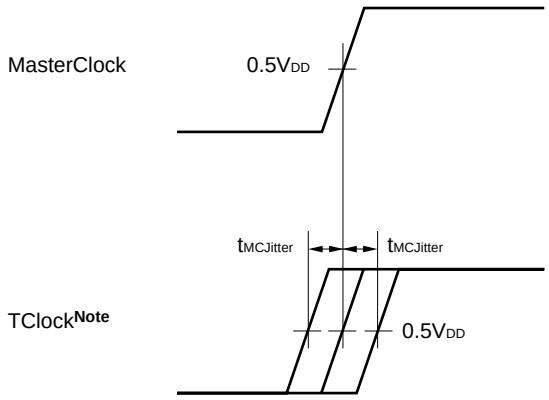
Timing Charts

Clock timing





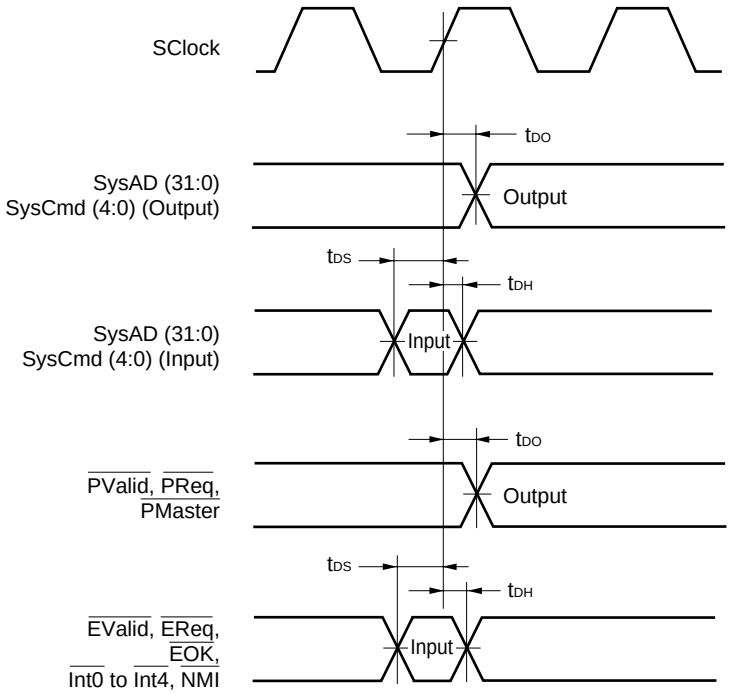
Clock jitter



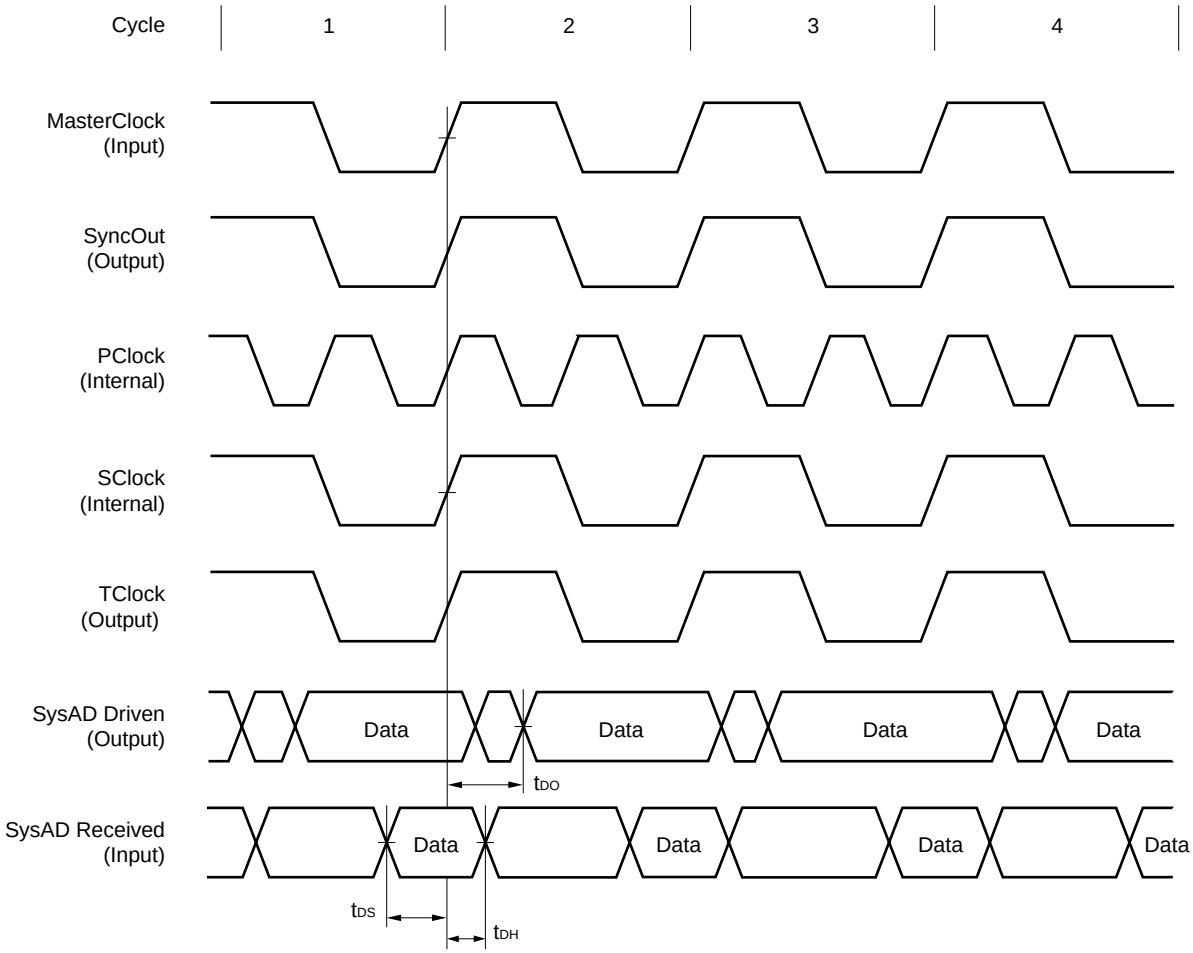
Note If SyncOut and SyncIn are connected with the shortest path, the point of TClock = 50% is the point of MasterClock = 50%.

Remark To match the MasterClock edge, make the load capacitance of the SyncIn/SyncOut path the same as that of TClock.

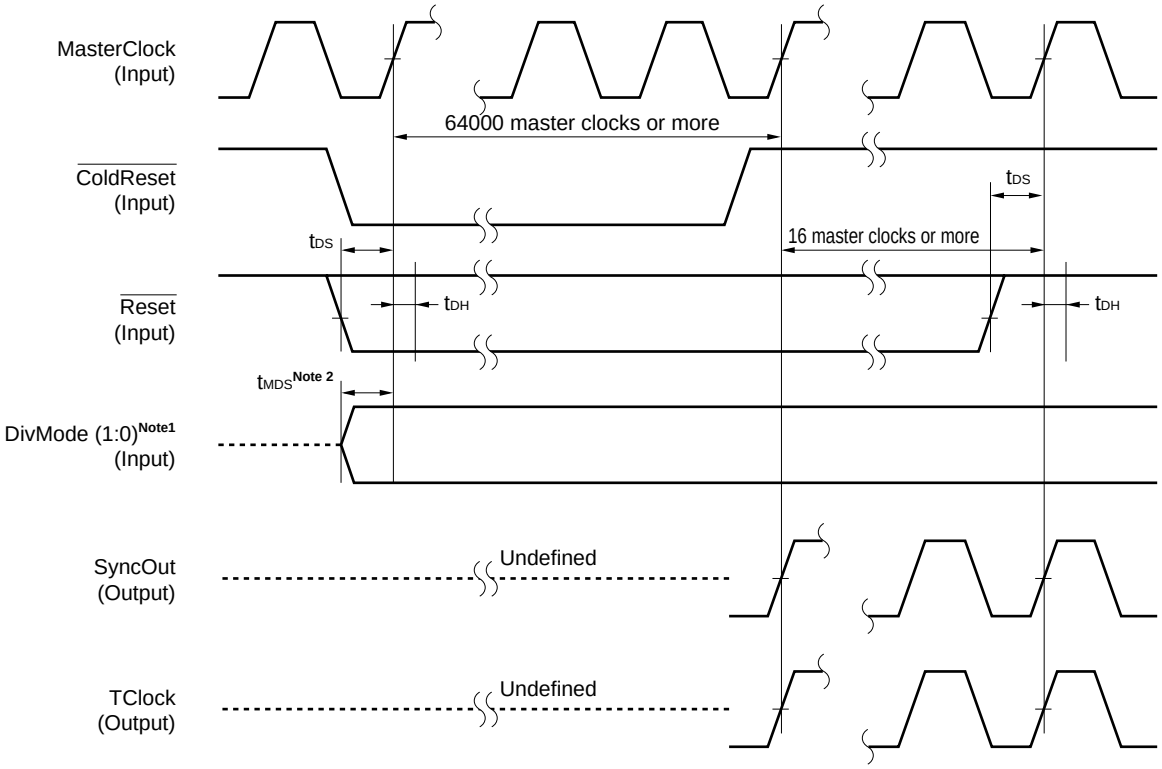
System interface edge timing



Clocking relationships



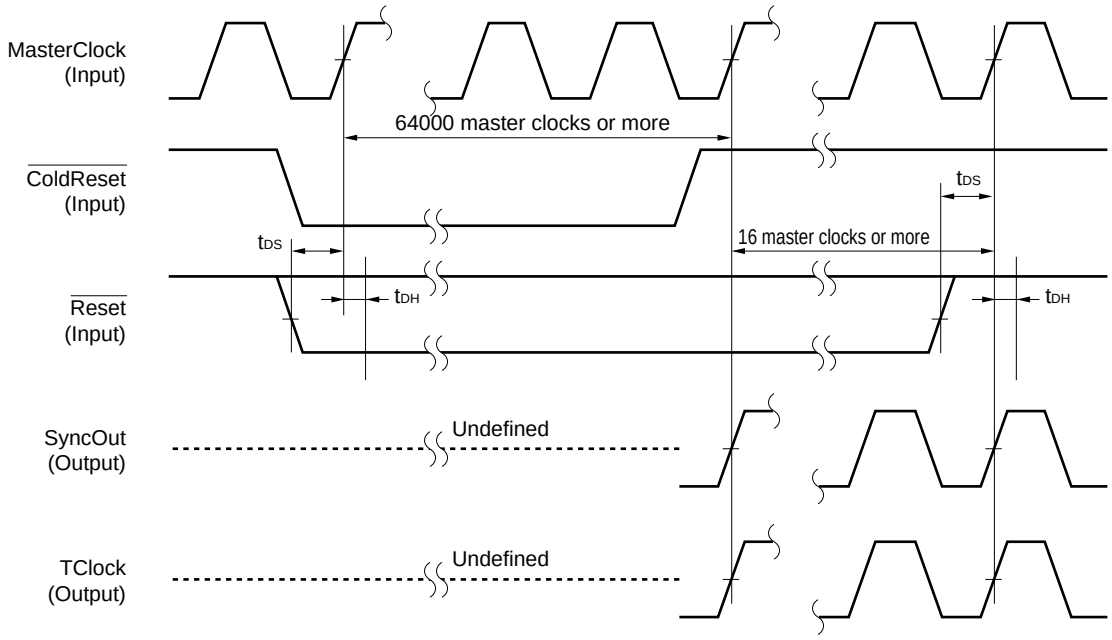
Power-on reset timing



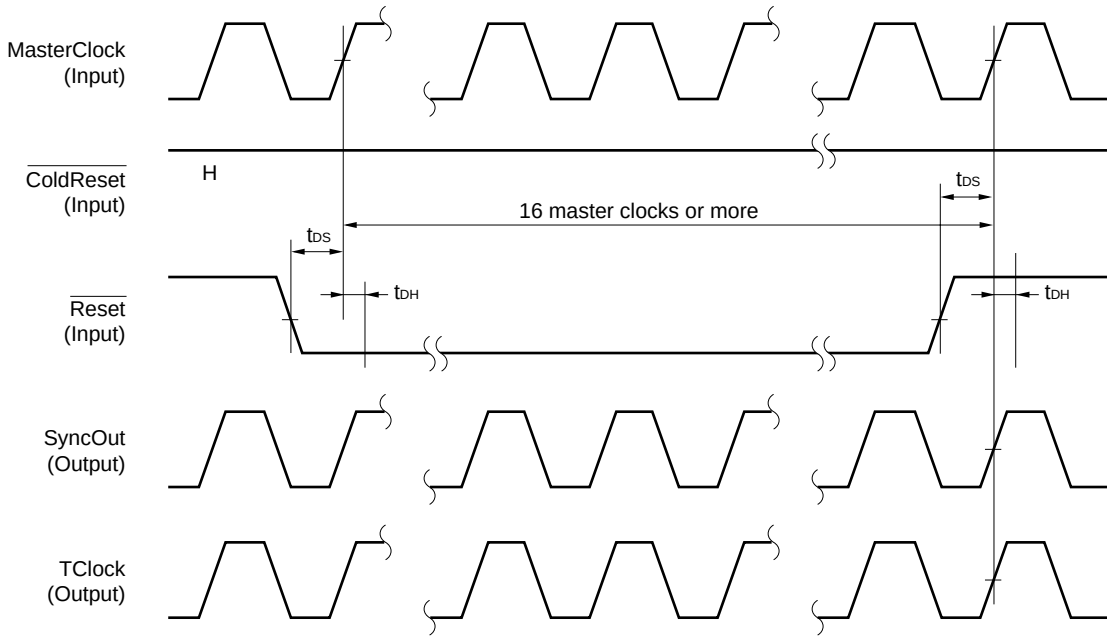
Notes 1. In the μPD30200-×××. DivMode (2:0) in the μPD30210-×××.

2. In the μPD30200-100 and 30200-133. t_{DS} in the μPD30200-80 and 30210-×××.

Cold reset timing

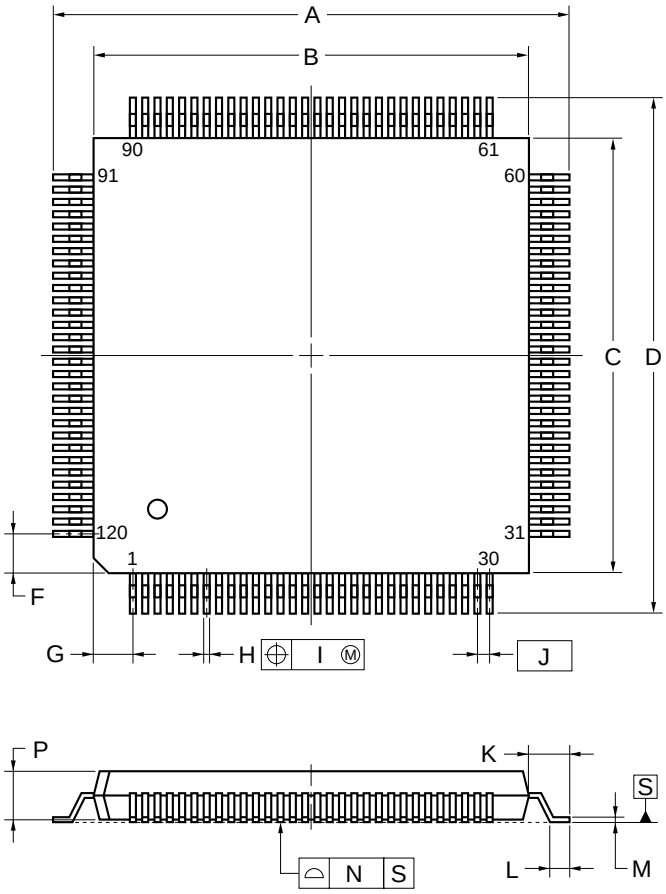


Software reset timing

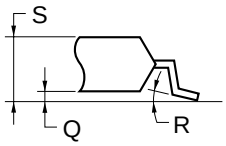


3. PACKAGE DRAWING

120 PIN PLASTIC QFP (28x28)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	32.0±0.3
B	28.0±0.2
C	28.0±0.2
D	32.0±0.3
F	2.4
G	2.4
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	2.0±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.1
P	3.2
Q	0.1±0.1
R	5°±5°
S	3.3±0.2

P120GD-80-LBB, MBB-2

4. RECOMMENDED SOLDERING CONDITIONS

The products should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD30200GD-80-LBB: 120-pin plastic QFP (28 × 28)
μPD30200GD-100-MBB: 120-pin plastic QFP (28 × 28)
μPD30200GD-133-MBB: 120-pin plastic QFP (28 × 28)
μPD30210GD-×××-MBB: 120-pin plastic QFP (28 × 28)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 36 hours.)	IR35-367-2
VPS	Package peak temperature: 215°C, Time: 40 sec. max, (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 36 hours.)	VP15-367-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec. max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 36 hours)	WS60-367-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec. max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX DIFFERENCES BETWEEN THE VR4300, VR4305, VR4310 AND VR4100™

Parameter		VR4300	VR4305	VR4310	VR4100
System bus	Write data transfer	Two buses (D/D××)			Four buses (D/D×/D××/D×××)
	Initial value setting pins at reset time	DivMode (1:0) (Can be set on power application only)		DivMode (2:0) (Can be set on power application only)	BigEndian, $\overline{\text{Div2}}$, HizParity
	Block write access	Sequential ordering			Subblock ordering
	State after final data write	Final data retained in transfer rate setting			End of access
	Non-cache high-speed write	Provided			Provided (Set with a register)
CPU	Corresponding instructions	MIPS I, II, and III instruction sets			MIPS I, II, III instruction sets plus sum-of-products arithmetic
Cache memory	Data protection	None			Word parity (instructions), byte parity (data)
JTAG interface		Provided			None
SyncOut-SyncIn path		Provided			None
Clock interface	Input vs. internal multiplication rate	1.5[Note 1], 2, 3, 4[Note 2]	1, 2, 3	2, 2.5[Note 3], 3, 4, 5, 6	4
	Internal vs. bus frequency division rate	1.5[Note 1], 2, 3, 4[Note 2]	1, 2, 3	2, 2.5[Note 3], 3, 4, 5, 6	1, 2
Power mode	Low-power mode	Pipeline/system bus operated at a quarter of the normal rate[Note4]		None	None
	Wait mode	None			Three types
PRId register		Imp = 0×0B			Imp = 0×0C

Notes 1. The 1.5 times frequency setting is allowed with the 100 MHz model only. (With the 133 MHz model, this setting is reserved.)

2. The 4 times frequency setting is allowed with the 133 MHz model only. (With the 100 MHz model, this setting is reserved.)

3. The 2.5 times frequency setting is allowed with the 167 MHz model only. (With the 133 MHz model, this setting is reserved.)

4. Not supported by the 133 MHz model of the VR 4300.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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