DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD3737

5150 PIXELS CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD3737 is a 5150-pixel high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3737 has high speed CCD register, so it is suitable for high resolution scanners and facsimiles which scan high definition document at high speed.

FEATURES

- Valid photocell : 5150 pixels
- Photocell pitch : 7 μm
- High response sensitivity
- Peak response wavelength : 550 nm (green)
- Resolution : 16 dot/mm A3 (297 × 420 mm) size (shorter side)
  24 dot/mm A4 (210 × 297 mm) size (shorter side)
- High speed scan : 252 μs/line
- Drive clock level : CMOS output under +5 V operation
- Data rate : 20 MHz Max.
- Power supply : +12 V

ORDERING INFORMATION

Part Number	Package
μPD3737D	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

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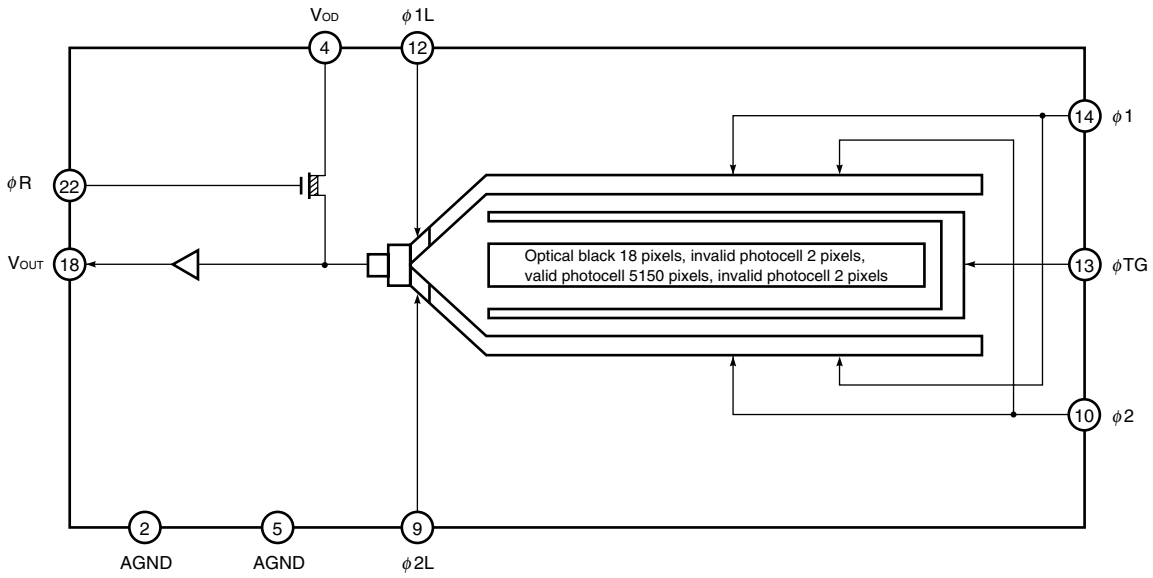
(Previous No. IC-3352)
Date Published February 2003 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

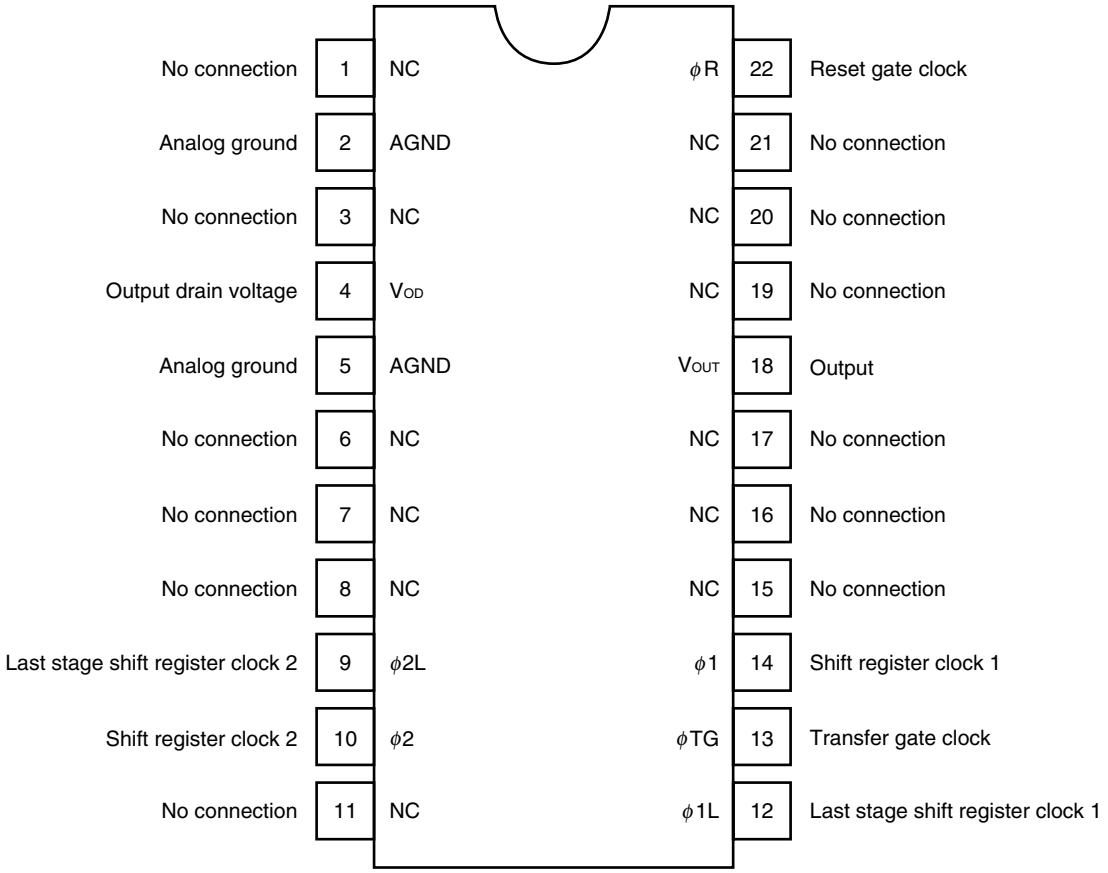
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

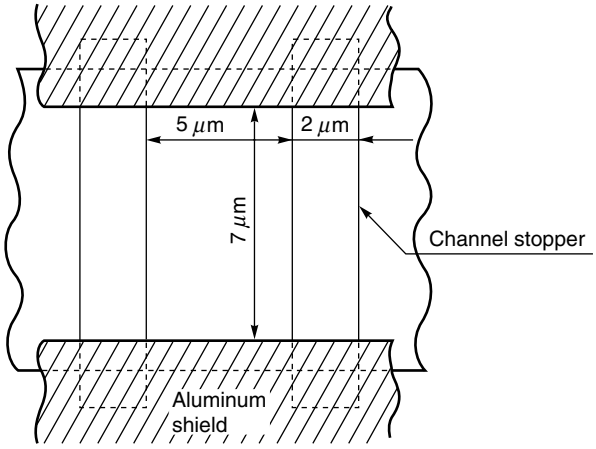
CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

• μPD3737D



★ **Caution Connect the No connection pins (NC) to GND.**

PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	−0.3 to +15	V
Last stage shift register clock voltage	$V_{\phi 1L}$, $V_{\phi 2L}$	−0.3 to +15	V
Reset signal voltage	$V_{\phi R}$	−0.3 to +15	V
Transfer gate clock voltage	$V_{\phi TG}$	−0.3 to +15	V
Operating ambient temperature Note	T_A	−25 to +55	°C
Storage temperature	T_{stg}	−40 to +100	°C

★ **Note** Use at the condition without dew condensation.

★ **Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1\_H}$, $V_{\phi 2\_H}$, $V_{\phi 1LH}$, $V_{\phi 2LH}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1\_L}$, $V_{\phi 2\_L}$, $V_{\phi 1LL}$, $V_{\phi 2LL}$	−0.3	0	+0.5	V
Reset signal ϕR high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset signal ϕR low level	$V_{\phi RBL}$	−0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TGH}$	4.5	$V_{\phi 1\_H}$ Note	$V_{\phi 1\_H}$ Note	V
Transfer gate clock low level	$V_{\phi TGL}$	−0.3	0	+0.5	V
Data rate	$f_{\phi R}$	0.5	1	20	MHz

★ **Note** When Transfer gate clock high level ($V_{\phi TGH}$) is higher than Shift register clock high level ($V_{\phi 1\_H}$), Image lag can increase.

Remarks1. Input reset signal ϕR to pin 22 via capacitor. Concerning the connection method refer to **APPLICATION CIRCUIT EXAMPLE**.

2. Operating conditions of reset signal ϕR is not the condition at device pins but the conditions of the signal which applied to capacitor.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, $f_{\phi 1}$ = 0.5 MHz, data rate = 1 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p}, light source : 3200 K halogen lamp + C500 (infrared cut filter))

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage	V_{sat}		1.0	1.5	–	V
Saturation exposure	SE	Daylight color fluorescent lamp	–	0.2	–	lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV	–	±5	±10	%
Average dark signal	ADS	Light shielding	–	1.0	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	–3	+3 –1	+6	mV
Power consumption	P_W		–	100	–	mW
Output impedance	Z_O		–	0.2	0.5	kΩ
Response	R_F	Daylight color fluorescent lamp	6	7.5	9	V/lx•s
Response peak			–	550	–	nm
Image lag	IL	V_{OUT} = 1.0 V	–	0.3	1	%
Offset level Note 1	V_{OS}		2.0	3.0	5.0	V
Output fall delay time Note 2	t_d	Time from 90% to 10% of ϕ2L fall is 5 ns	–	25	–	ns
Register imbalance	RI	V_{OUT} = 500 mV	–	0	4	%
Total transfer efficiency	TTE	V_{OUT} = 500 mV, data rate ($f_{\phi R1}$) = 20 MHz	92	98	–	%
Dynamic range	DR1	V_{sat}/DSNU	–	500	–	times
Reset feed-through noise Note 1	RFTN	Light shielding	–	250	500	mV

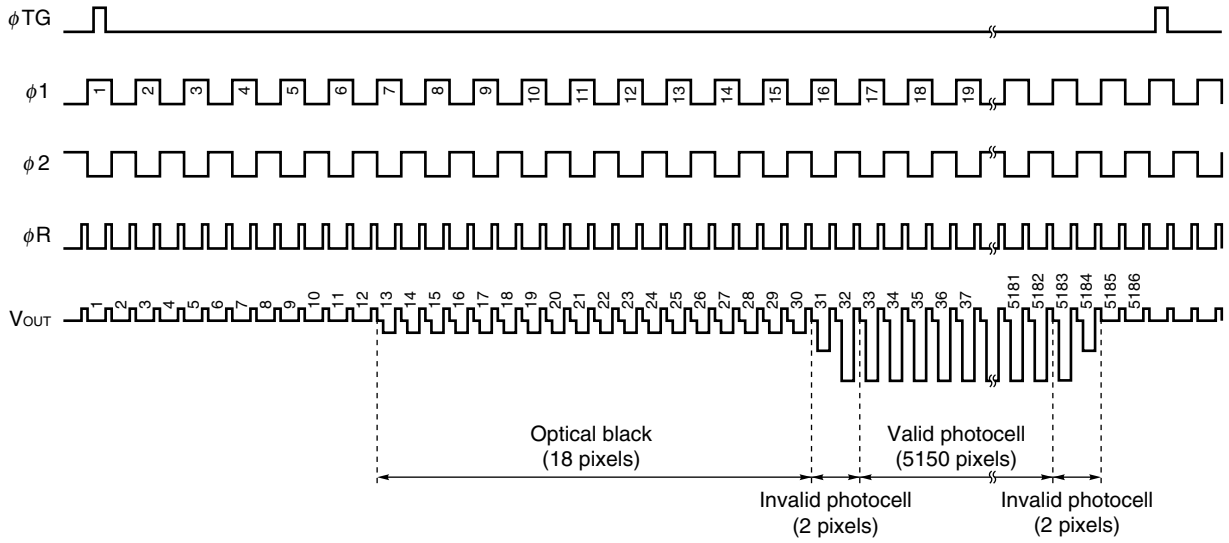
Notes 1. Refer to **TIMING CHART 2**.

2. t_d is defined as a time from 10% of ϕ2L to 10% of V_{OUT}, output after passing through two steps of emitter follower in the **APPLICATION CIRCUIT EXAMPLE**.

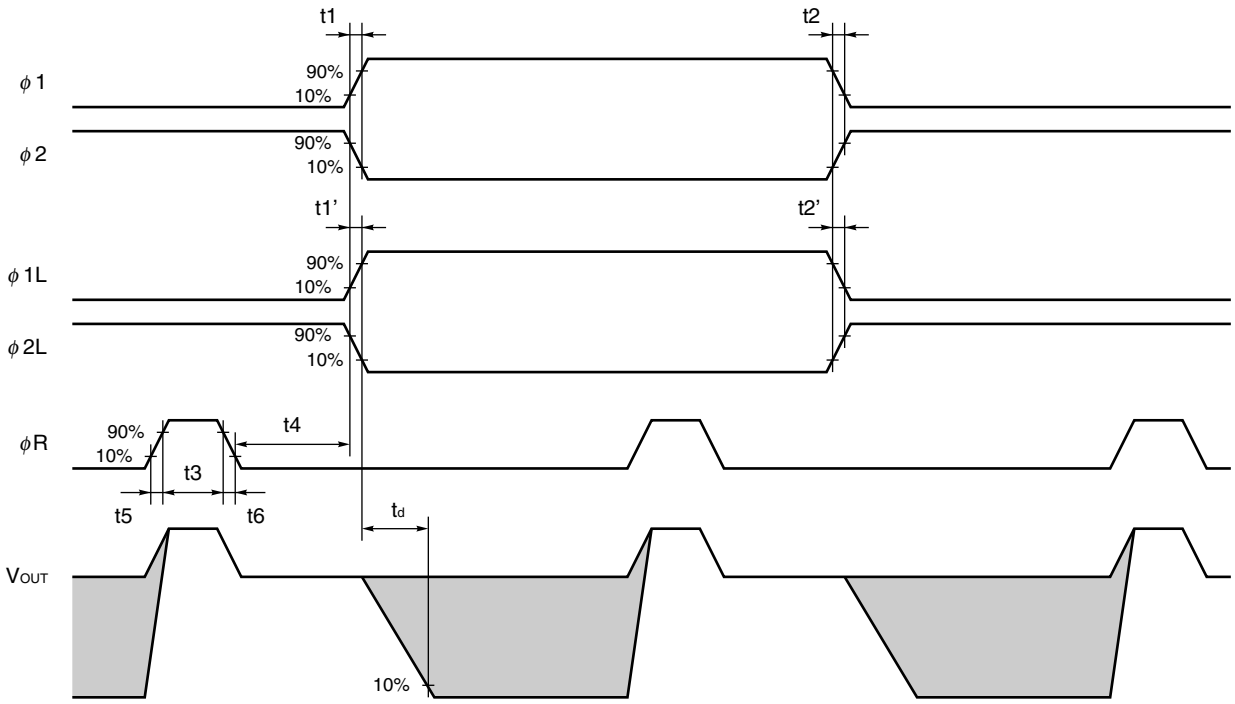
★ INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	14	–	550	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	10	–	550	–	pF
Last stage shift register clock pin capacitance 1	$C_{\phi 1L}$	ϕ1L	12	–	50	–	pF
Last stage shift register clock pin capacitance 2	$C_{\phi 2L}$	ϕ2L	9	–	50	–	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR	22	–	10	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	13	–	150	–	pF

TIMING CHART 1



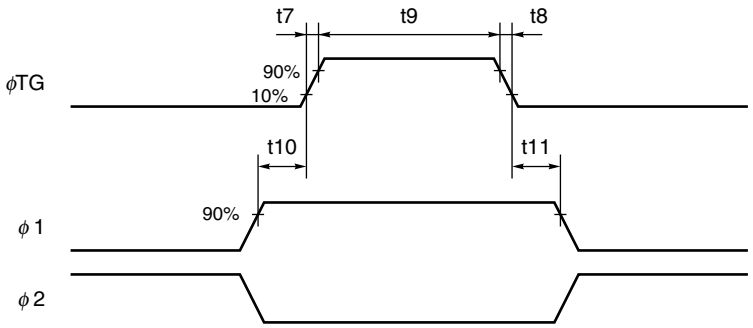
TIMING CHART 2



Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	50	(150)	ns
t1', t2'	0	5	(25)	ns
t3	15	50	(500)	ns
t4	5	20	(500)	ns
t5, t6	0	20	(50)	ns

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD3737 is destroyed.

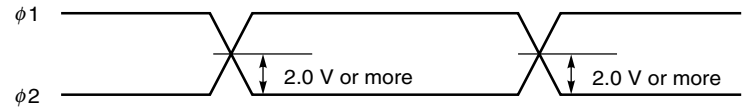
φTG, φ1, φ2 TIMING CHART



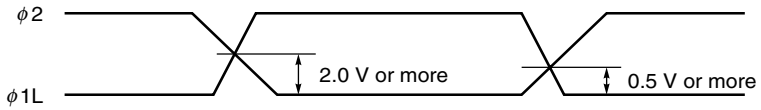
Symbol	Min.	Typ.	Max.	Unit
t7, t8	0	50	(100)	ns
t9	500	1000	(5000)	ns
t10, t11	0	100	(500)	ns

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD3737 is destroyed.

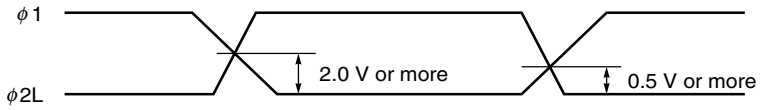
φ1, φ2 cross points



φ1L, φ2 cross points



φ1, φ2L cross points



Remark Adjust cross points (φ1, φ2), (φ1L, φ2) and (φ1, φ2L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
   Output signal voltage at which the response linearity is lost.

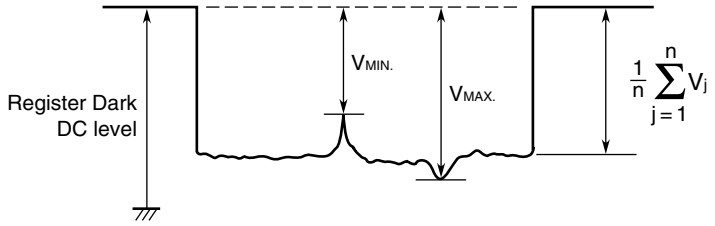
2. Saturation exposure : **SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : **PRNU**
   The peak/bottom ratio to the average output voltage of all the valid pixels calculated by the following formula.

$$PRNU\ (\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

n : Number of valid pixcels

V_j : Output voltage of each pixel

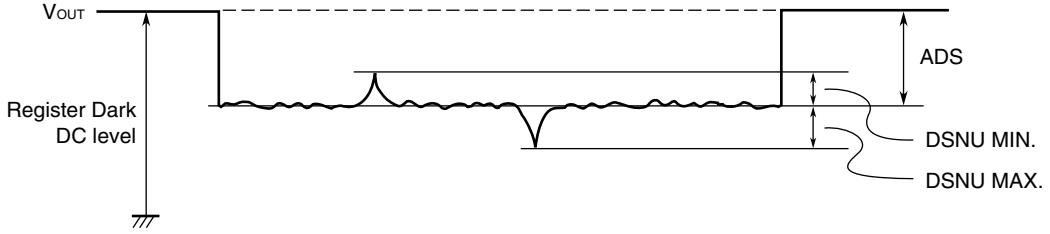


★ 4. Average dark signal : **ADS**
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{5150} d_j}{5150}$$

d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**
   The difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding.



6. Output impedance : **Zo**

   Impedance of the output pins viewed from outside.

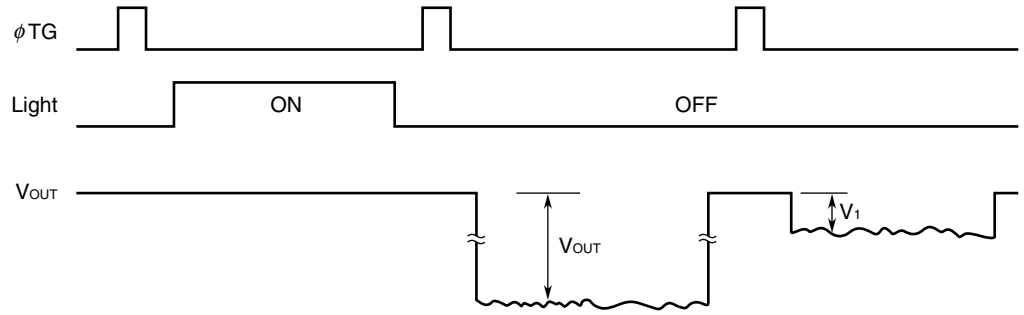
7. Response : **R**

   Output voltage divided by exposure (lx•s).

   Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

   The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance: **RI**

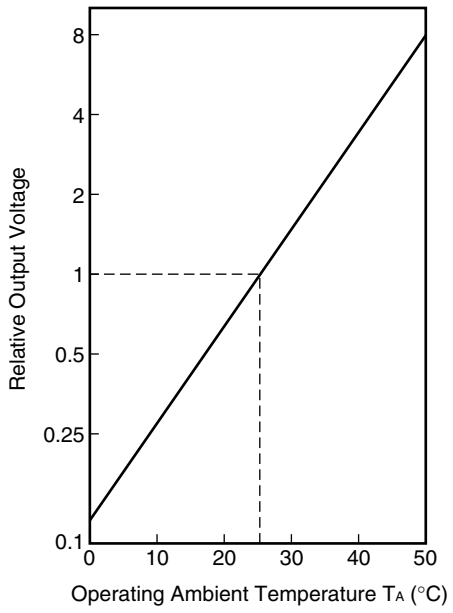
   The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

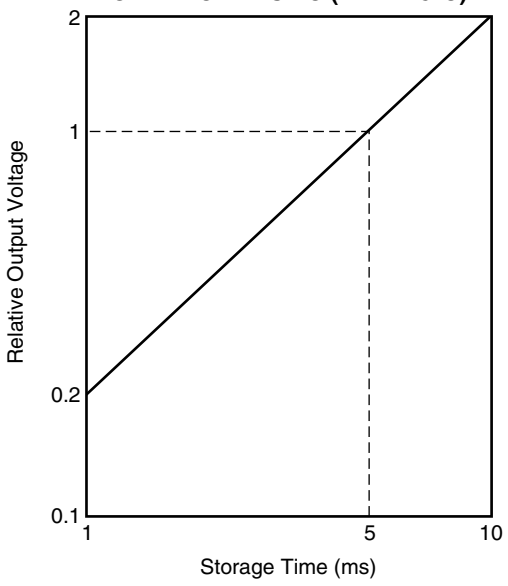
n : Number of valid pixels
V_j : Output voltage of each pixel

STANDARD CHARACTERISTIC CURVES (Reference Value)

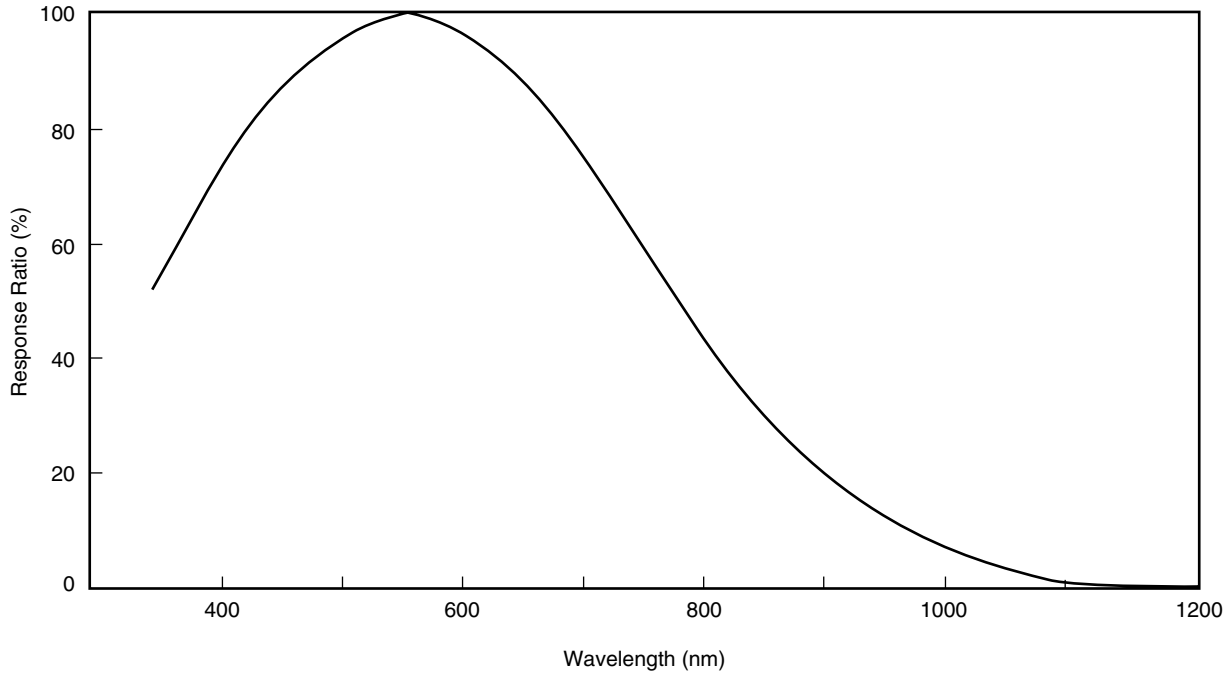
DARK OUTPUT TEMPERATURE CHARACTERISTIC



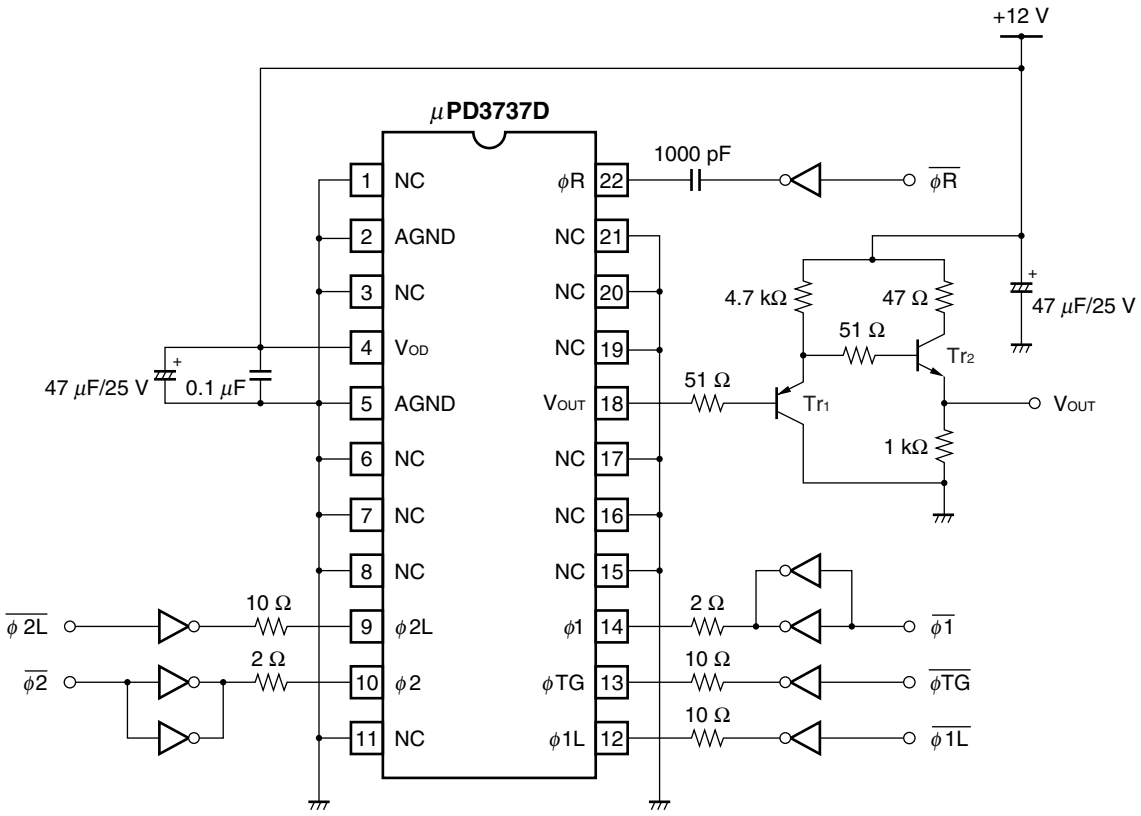
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter) (T_A = +25°C)



★ APPLICATION CIRCUIT EXAMPLE



Caution Connect the No connection pins (NC) to GND.

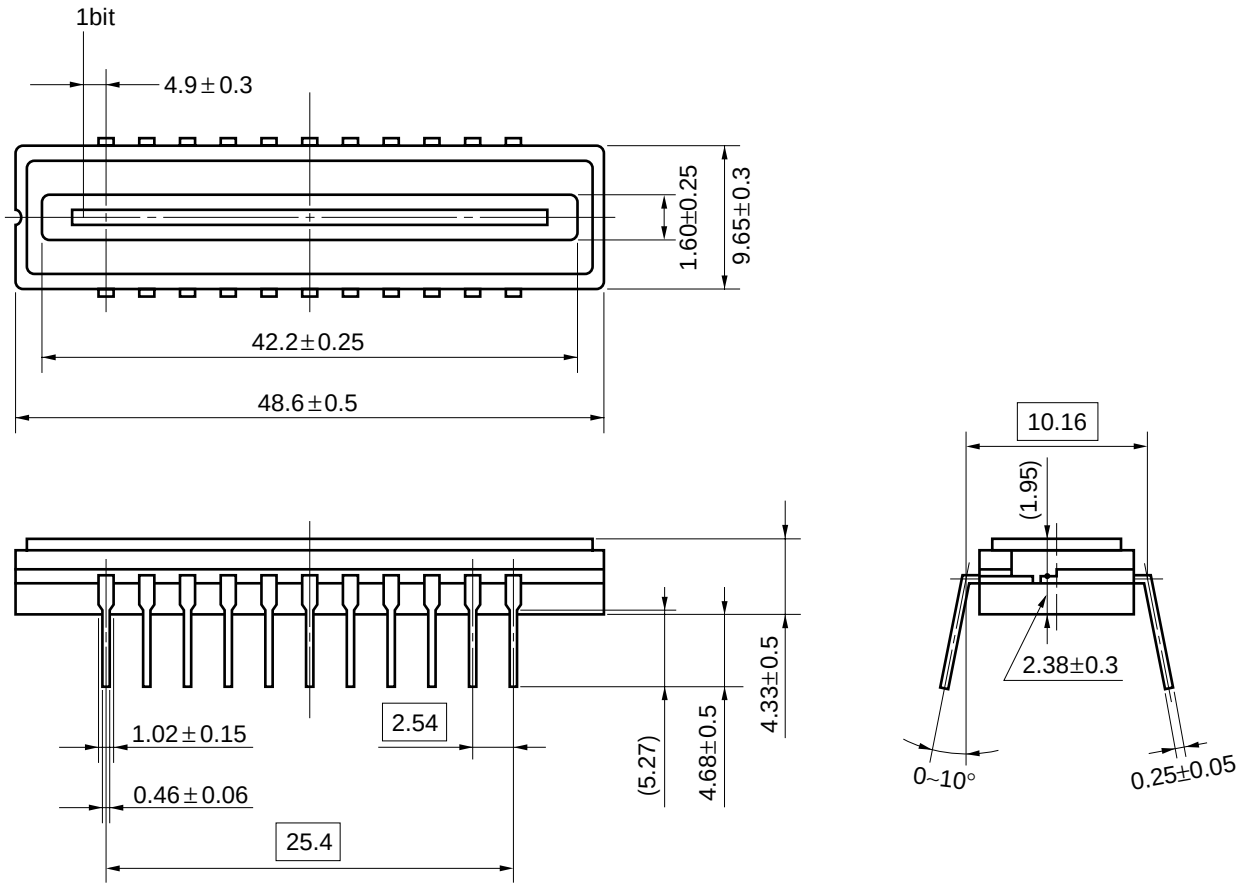
Remarks 1. The inverters shown in the above application circuit example are the 74AC04.

2. Tr_1 : 2SA1005, Tr_2 : 2SC945

★ **PACKAGE DRAWING**

μPD3737D
CCD LINEAR IMAGE SENSOR 22-PIN CERAMIC DIP (CERDIP) (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG7-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD3737D : CCD linear image sensor 22-pin ceramic DIP (CERDIP) (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

★ **Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.**

2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

★

NOTES ON HANDLING THE PACKAGES

① MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

② GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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