NEC

MOS INTEGRATED CIRCUIT

μPD3797

5300 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

The μPD3797 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD3797 has 3 rows of 5300 pixels, and each row has a single-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits, sample and hold circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

- Valid photocell : 5300 pixels × 3
- Photocell's pitch : 7 μm
- Line spacing : 28 μm (4 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 24 dot/mm A4 (210 × 297 mm) size (shorter side)
  600 dpi US letter (8.5" × 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 5 MHz MAX.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Sample and hold circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD3797D	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)

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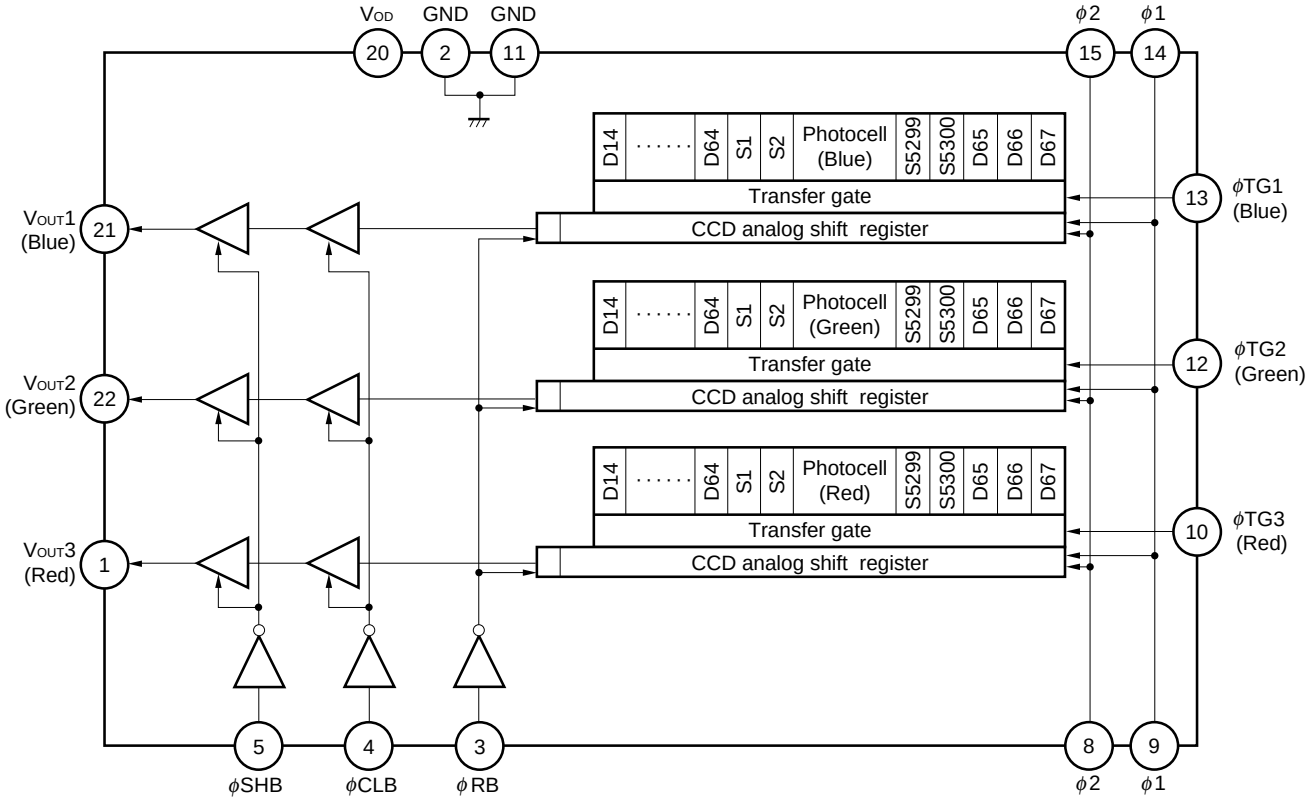
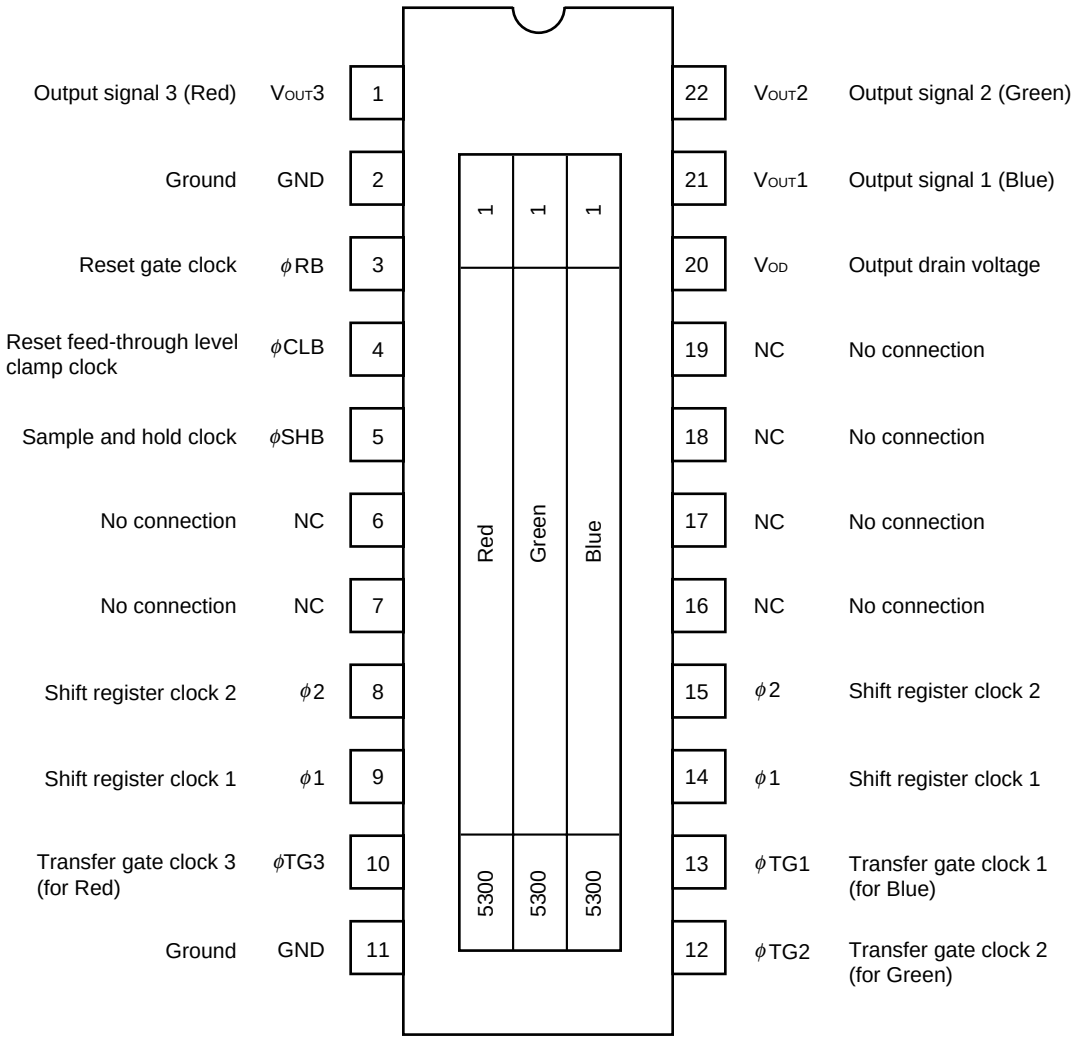
Printed in Japan

BLOCK DIAGRAM

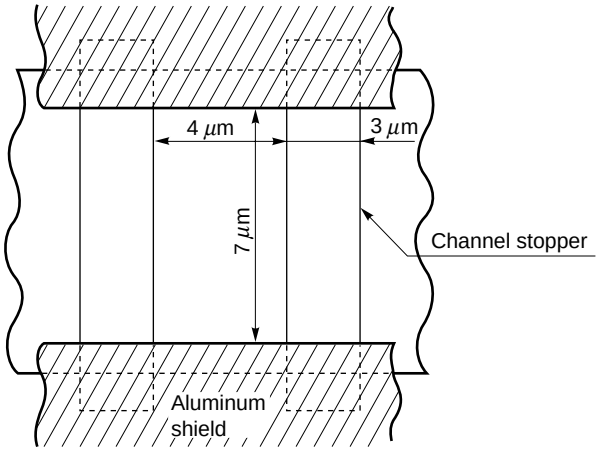


PIN CONFIGURATION (Top View)

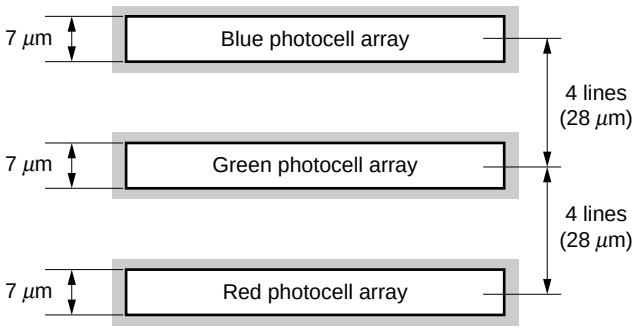
CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi1}$, $V_{\phi2}$	–0.3 to +15	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +15	V
Sample and hold clock voltage	$V_{\phi SHB}$	–0.3 to +15	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	–0.3 to +15	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +15	V
Operating ambient temperature	T_A	–25 to +60	°C
Storage temperature	T_{stg}	–40 to +100	°C

Caution Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS (T_A = +25 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi1H}$, $V_{\phi2H}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi1L}$, $V_{\phi2L}$	–0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	–0.3	0	+0.5	V
Sample and hold clock high level	$V_{\phi SHBH}$	4.5	5.0	5.5	V
Sample and hold clock low level	$V_{\phi SHBL}$	–0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.5	$V_{\phi1H}$**Note**	$V_{\phi1H}$**Note**	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	–0.3	0	+0.5	V
Data rate	$f_{\phi RB}$	–	1.0	5.0	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than Shift register clock high level ($V_{\phi1H}$), Image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25 °C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 1 MHz, storage time = 5.5 ms,
light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1mm), input signal clock = 5 V_{p-p})

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V_{sat}		2.0	3.0	–	V
Saturation exposure	Red	SER			0.268		lx•s
	Green	SEG			0.294		lx•s
	Blue	SEB			0.492		lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V		6	20	%
Average dark signal		ADS	Light shielding		0.2	4.0	mV
Dark signal non-uniformity		DSNU	Light shielding		2.0	4.0	mV
Power consumption		P_W			400	700	mW
Output impedance		Z_O			0.5	1	kΩ
Response	Red	R_R		7.8	11.2	14.6	V/lx•s
	Green	R_G		7.1	10.2	13.3	V/lx•s
	Blue	R_B		4.2	6.1	8.0	V/lx•s
Image lag		IL	V_{OUT} = 1.0 V		3.0	10.0	%
Offset level **Note1**		V_{OS}		4.0	5.5	7.0	V
Output fall delay time **Note2**		t_d	V_{OUT} = 1.0 V		40		ns
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 5 MHz	92	98		%
Response peak	Red				630		nm
	Green				540		nm
	Blue				460		nm
Dynamic range		DR1	V_{sat} /DSNU		1500		times
		DR2	V_{sat} /σ		3000		times
Reset feed-through noise **Note1**		RFTN	Light shielding, Non-sample and hold mode	–1000	–300	+500	mV
Random noise		σ	Light shielding	–	1.0	–	mV

Notes 1. Refer to **TIMING CHART 2**.

2. When the fall time of ϕ1 (t1) is the TYP. value (refer to **TIMING CHART 2**).

INPUT PIN CAPACITANCE (T_A = +25 °C, V_{OD} = 12 V)

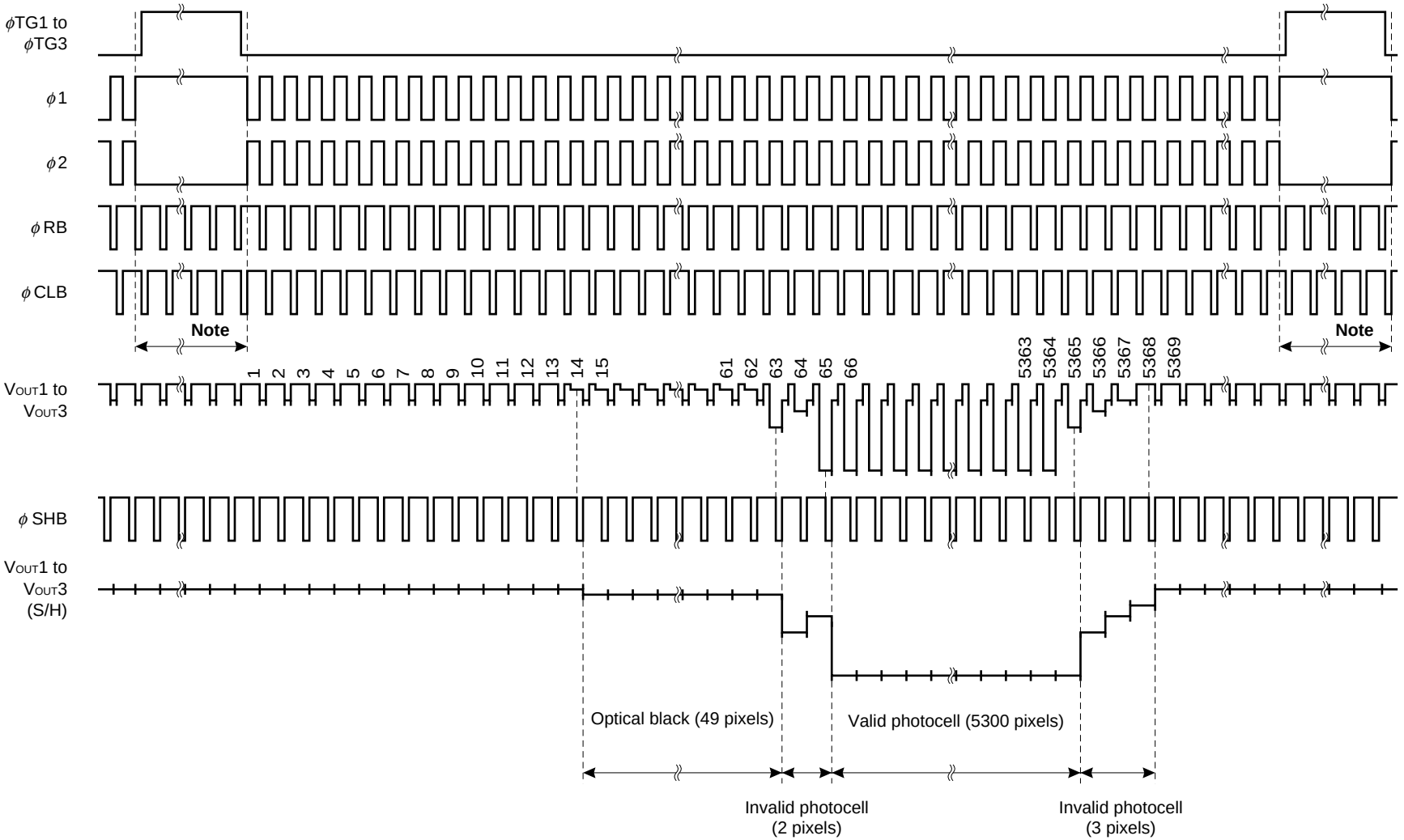
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	9		400		pF
			14		400		pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	8		400		pF
			15		400		pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	3		15		pF
Sample and hold clock pin capacitance	$C_{\phi SHB}$	ϕSHB	5		15		pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	4		15		pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG1	13		100		pF
		ϕTG2	12		100		pF
		ϕTG3	10		100		pF

Remark Pins 9 and 14 (ϕ1), 8 and 15 (ϕ2) are each connected inside of the device.

SAMPLE AND HOLD FUNCTION

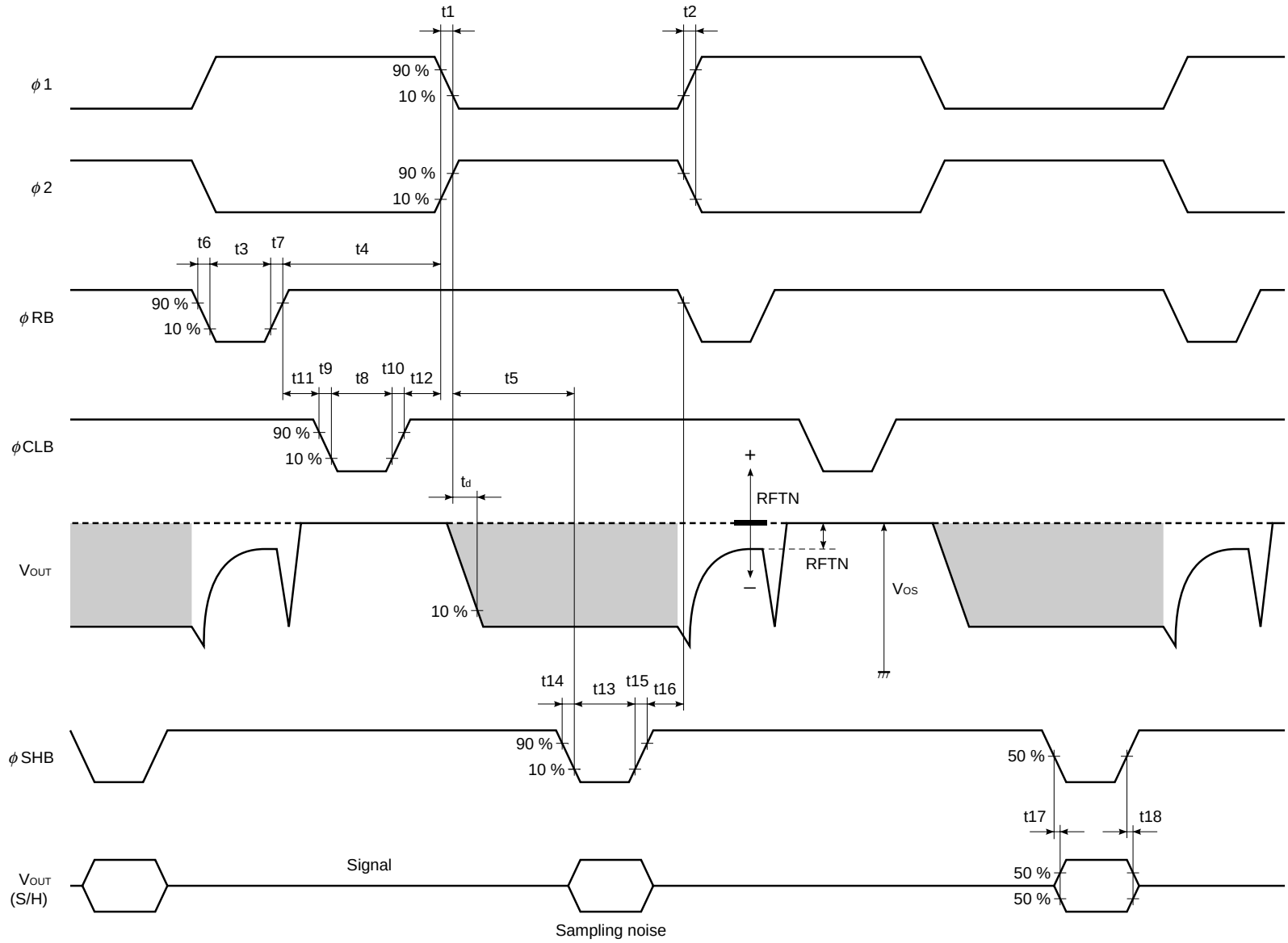
ϕSHB	Output type
Pulse	Sample and hold type
DC low level	Non-sample and hold type
DC high level	Prohibited

TIMING CHART 1 (for each color)

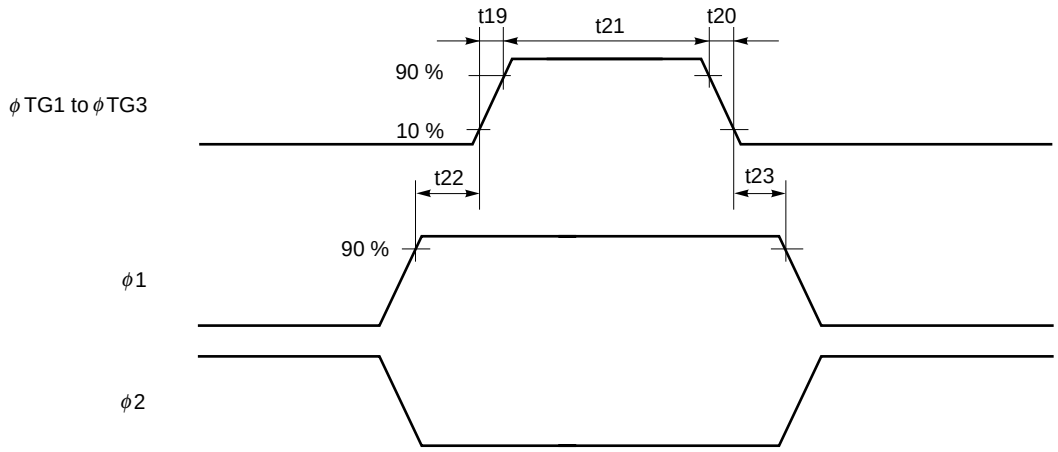


Note Input the φRB and φCLB pulses continuously during this period. And also input the φSHB pulse when the on-chip sample and hold function is used.

TIMING CHART 2 (for each color)

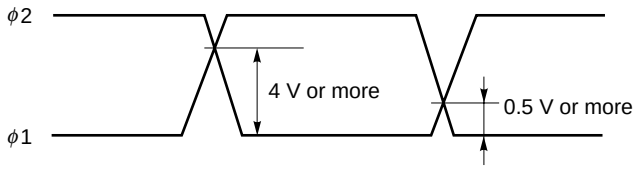


φTG1 to φTG3, φ1, φ2 TIMING CHART



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	25		ns
t3	30	50		ns
t4	60	250		ns
t5	60	200		ns
t6, t7	0	25		ns
t8	40	100		ns
t9, t10	0	25		ns
t11	10	50		ns
t12	0	5		ns
t13	40	150		ns
t14, t15	0	25		ns
t16	0	30		ns
t17, t18	0	10	–	ns
t19, t20	0	50		ns
t21	3000	10000		ns
t22, t23	900	1000		ns

φ1, φ2 cross points



Remark Adjust cross points of φ1 and φ2 with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (I_X) and storage time (s) when saturation of output voltage occurs.

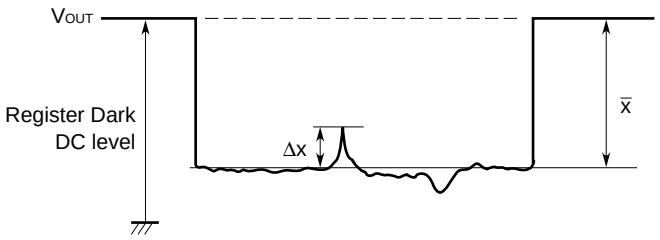
3. Photo response non-uniformity: PRNU
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{5300} x_j}{5300}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal: ADS
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

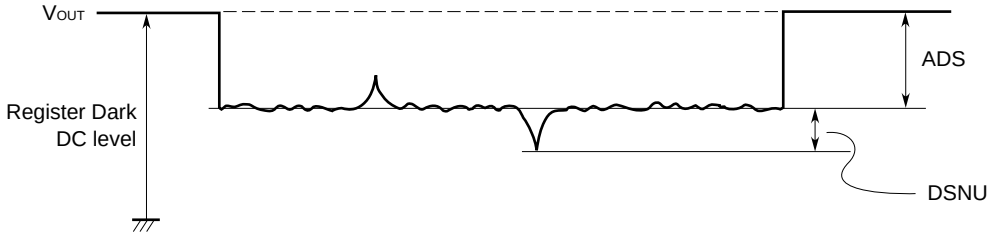
$$\text{ADS (mV)} = \frac{\sum_{j=1}^{5300} d_j}{5300}$$

d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU
   Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV) : maximum of $|d_j - \text{ADS}|_{j = 1 \text{ to } 5300}$

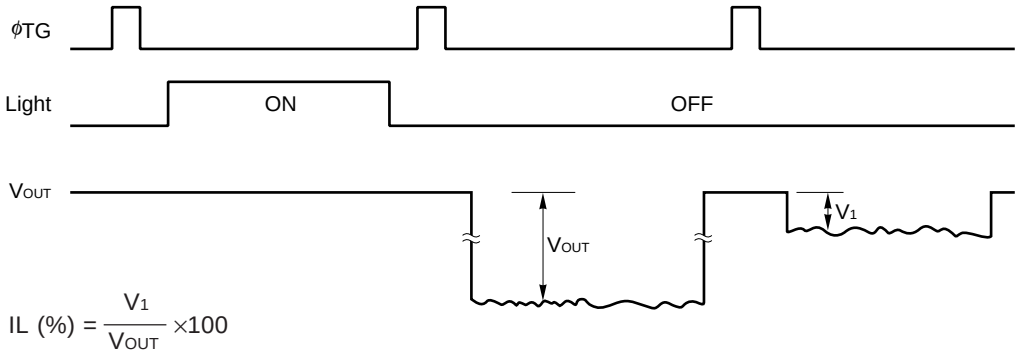
d_j : Dark signal of valid pixel number j



6. Output impedance: Z_O
   Impedance of the output pins viewed from outside.

7. Response: R
   Output voltage divided by exposure (Ix•s).
   Note that the response varies with a light source (spectral characteristic).

8. Image Lag: IL
   The rate between the last output voltage and the next one after read out the data of a line.

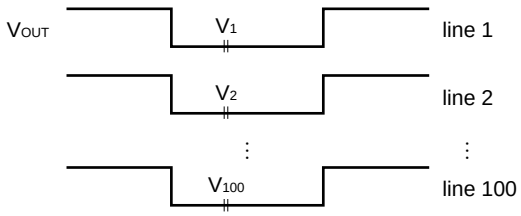


$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Random noise: σ
   Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

$$\sigma\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

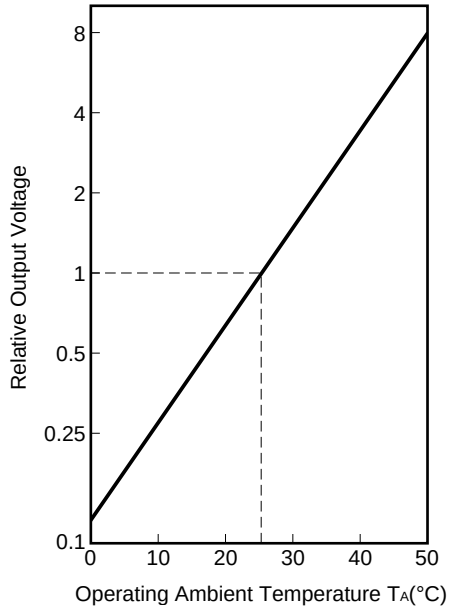
V_i: A valid pixel output signal among all of the valid pixels for each color



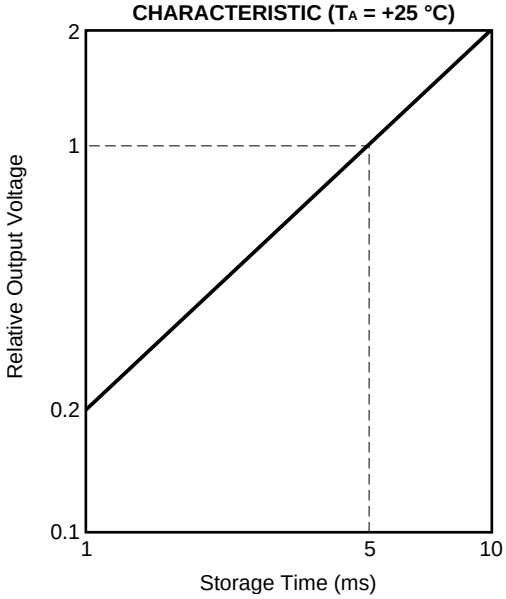
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES

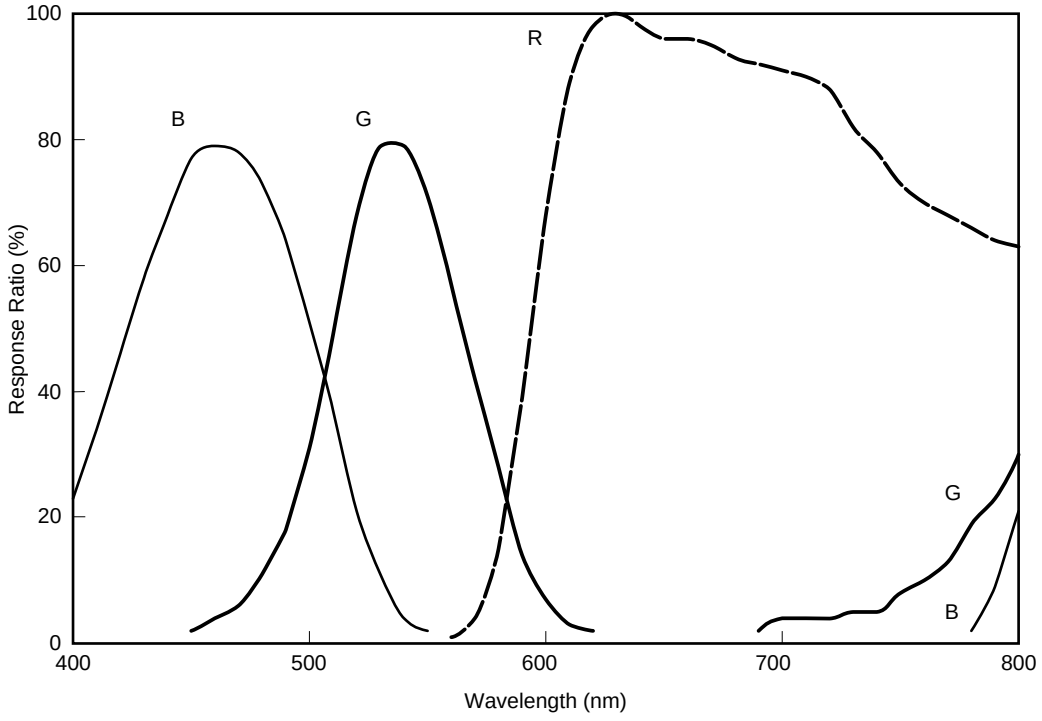
DARK OUTPUT TEMPERATURE CHARACTERISTIC



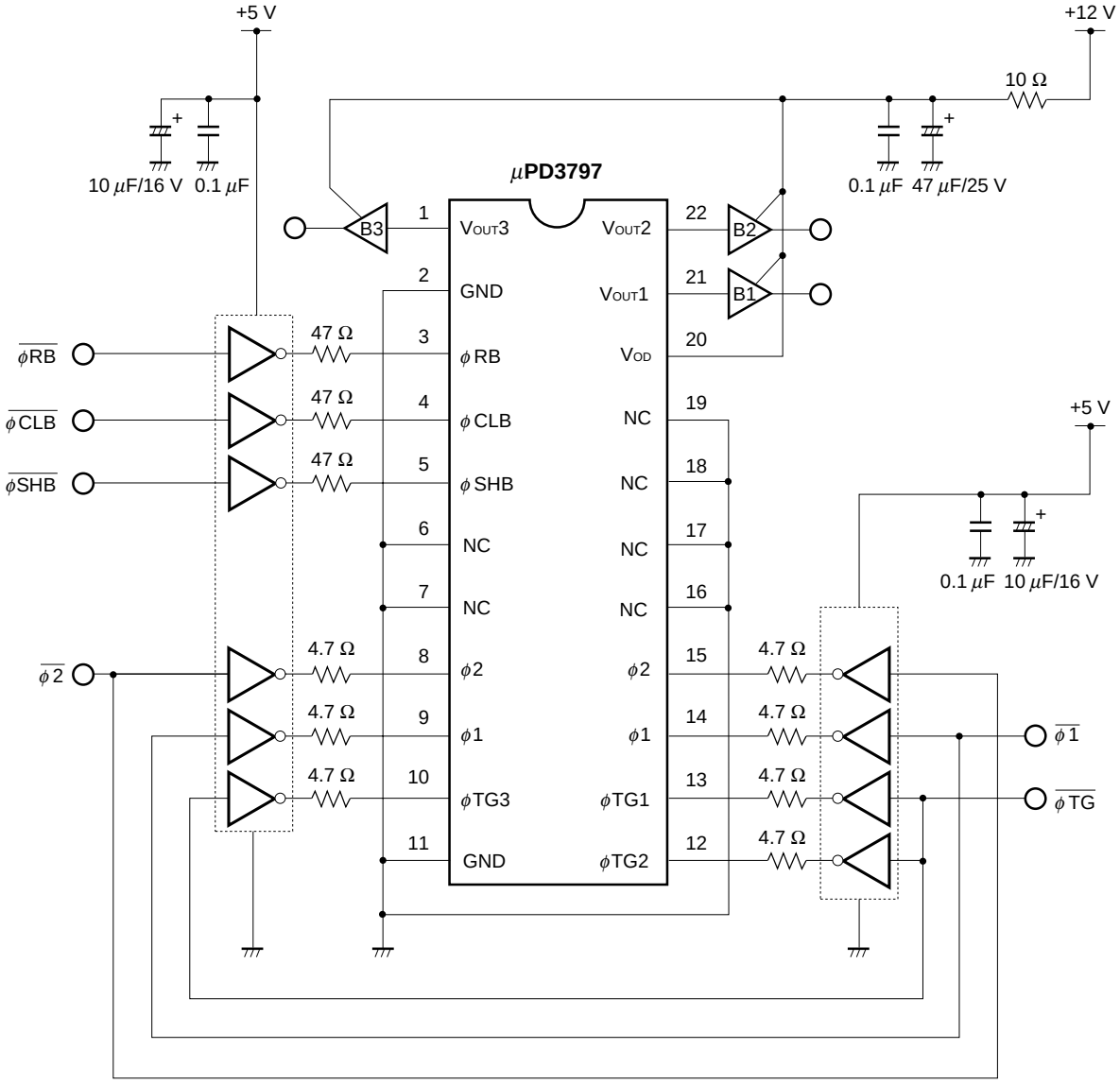
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25 °C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter) (T_A = +25 °C)



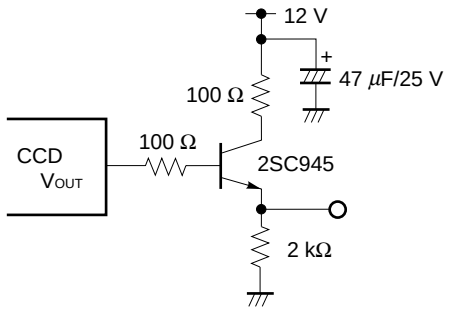
APPLICATION CIRCUIT EXAMPLE



Remarks **1.** When internal sample and hold circuit of the μPD3797 is not necessary, connect pin 5 (φSHB) to GND.

2. The inverters shown in the above application circuit example are the 74HC04.

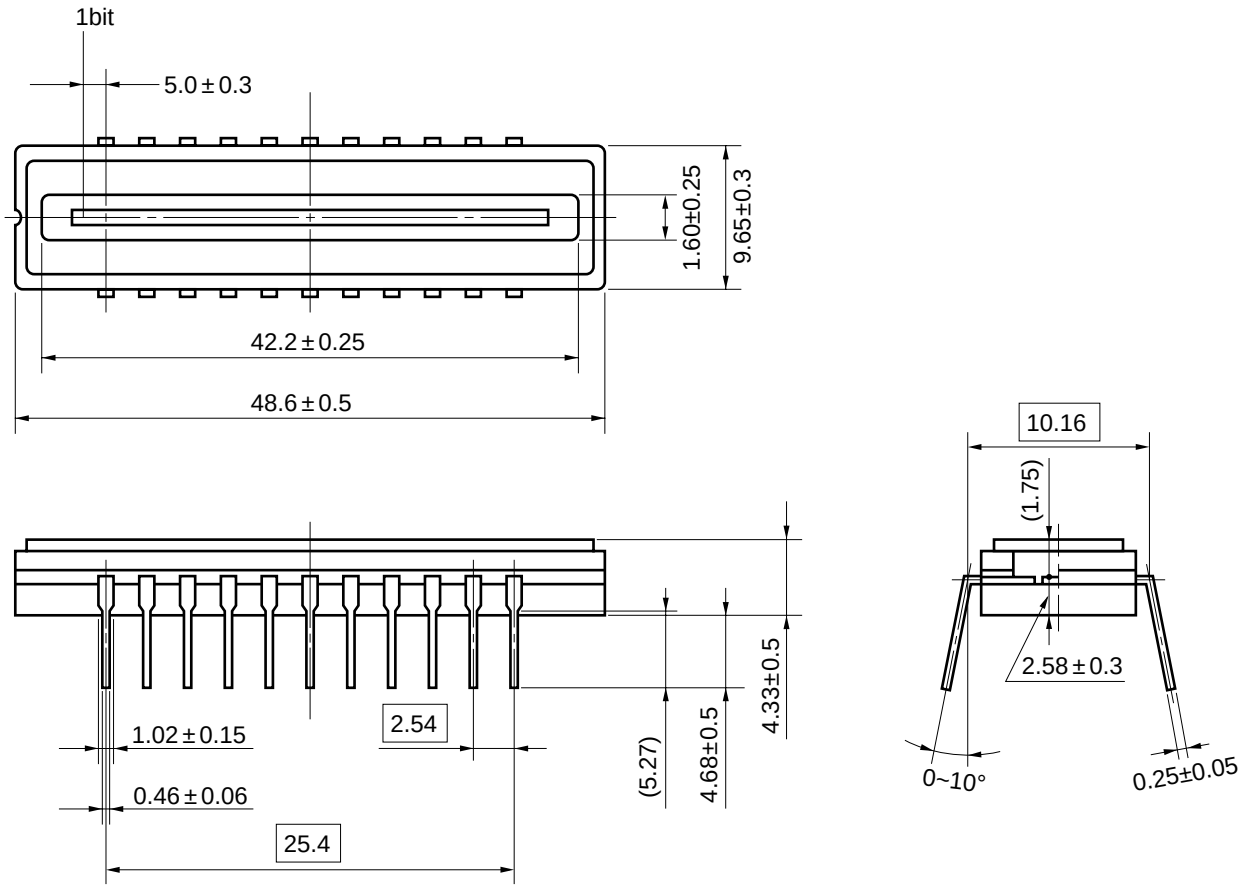
B1 to B3 EQUIVALENT CIRCUIT



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP(CERDIP)(400mil)

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG9

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual"(C10535E)**.

Type of Through-hole Device

μPD3797D: CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)

Process	Conditions
Partial heating method	Pin temperature: 260 °C or below, Heat Time: 10 seconds or less (per pin)

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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