NEC

MOS INTEGRATED CIRCUIT

μPD6376

AUDIO 2-CHANNEL 16-BIT D/A CONVERTER

The μPD6376 is an audio 2-channel 16-bit D/A converter.

The μPD6376 has low sound quality deterioration by employing the resistor string configuration and 0-point offset, and low power consumption by using the CMOS process. It operates on a single 5-V power supply, and it is pin-compatible with the μPD6372 when Pin 1 is low level or open.

FEATURES

- Single 5-V power supply
- CMOS structure
- On-chip output operational amplifier circuit
- On-chip 0-point offset circuit
- Resistor string configuration
- 8 f_S (2 ch × 400 kHz) supported
- On-chip 2-channel DAC
- L-R in-phase output

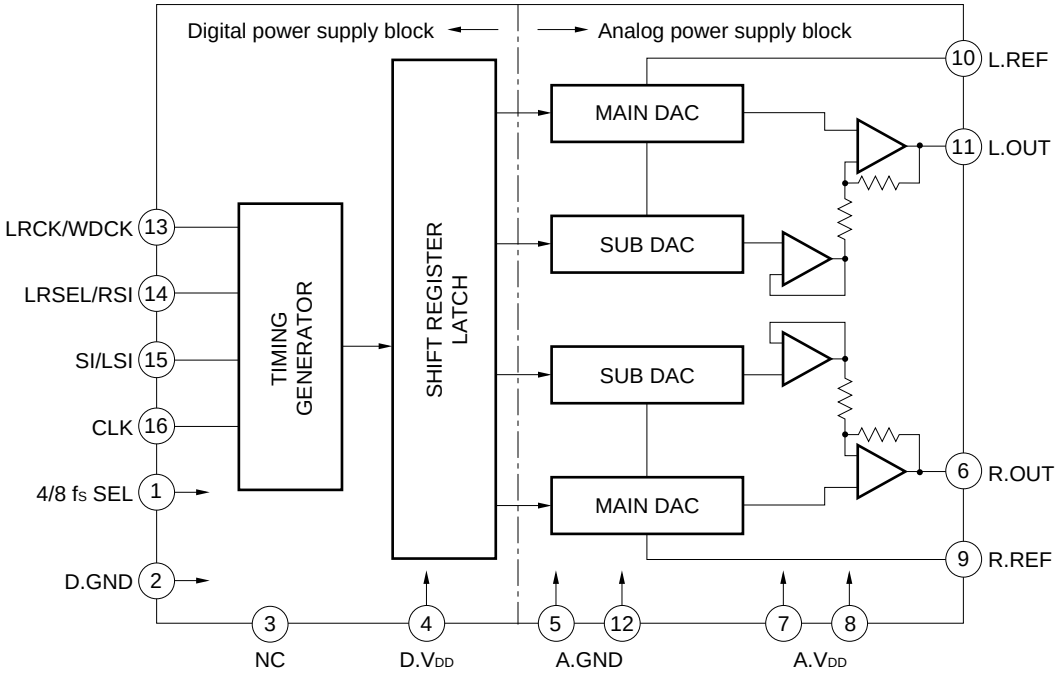
ORDERING INFORMATION

Part Number	Package
μPD6376GS	16-pin plastic SOP 7.62 mm (300)

Document No. S12799EJ6V0DS00 (6th edition)
Date Published June 2002 N CP(K)
Printed in Japan

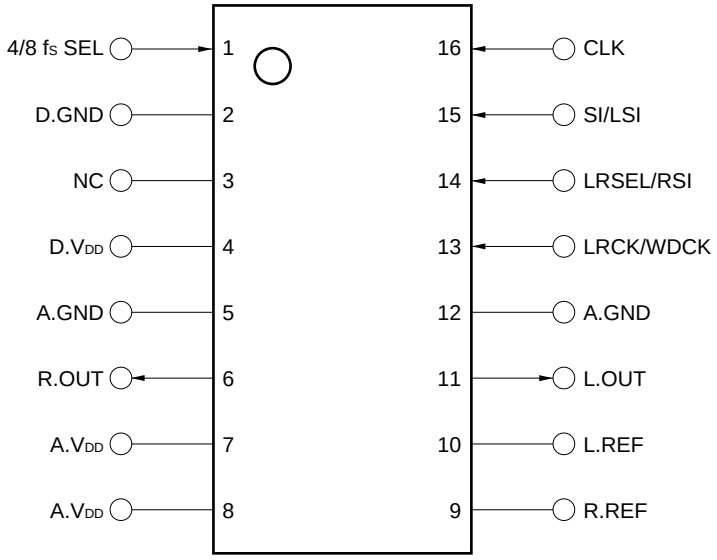
The mark ★ shows major revised points.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

16-Pin Plastic SOP 7.62 mm (300)



1. PIN FUNCTIONS

Pin No.	Symbol	Name	I/O	Function
1	4/8 f_S SEL		Input	When this pin is Low or leaves Open, L-ch data and R-ch data is input in time-division from Pin 15. When this pin is High, L-ch data is input from Pin 15, and R-ch data is input from Pin 14. (Pulled down in IC with 100-kΩ resistor)
2	D.GND	Digital GND	—	GND pin of logic block
3	NC	Non Connection	—	Not connected to internal chip
4	D.V_{DD}	Digital V_{DD}	—	Power supply pin to logic block
5	A.GND	Analog GND	—	GND pin to analog block
6	R.OUT	R-ch OUTPUT	Output	Right analog signal output pin
7	A.V_{DD}	Analog V_{DD}	—	Power supply pin to analog block
8	A.V_{DD}	Analog V_{DD}		
9	R.REF	R-ch Voltage Reference	—	Reference voltage pin. Normally connected to A. GND through via capacitor to lower impedance
10	L.REF	L-ch Voltage Reference		
11	L.OUT	L-ch OUTPUT	Output	Left analog signal output pin
12	A.GND	Analog GND	—	GND pin of analog block
13	LRCK/WDCK	Left/Right Clock WORD Clock	Input	When Pin 1 is Low or leaves Open: Functions as L-R judgment signal input pin. When Pin 1 is High: Functions as input data word judgment signal input pin.
14	LRSEL/RSI	Left/Right Selection R-ch Series Input	Input	When Pin 1 is Low or leaves Open: Functions as pin to select L-R polarity for LRCK signal. When LRCK signal is High, set LRSEL pin to Low to input L-ch data; When LRCK signal is LOW, set LRSEL pin to High to input L-ch data. When Pin 1 is High: Functions as R-ch serial data input pin.
15	SI/LSI	Series Input L-ch Series Input	Input	When Pin 1 is Low or Open: Functions as L-ch and R-ch serial data input pin alternately. When Pin 1 is High: Functions as L-ch serial data input pin.
16	CLK	CLOCK	Input	Input pin for read clock of serial input data

2. INPUT SIGNAL FORMAT

- Input data must be input as 2's complement, MSB first.

  2's complement is a method of expressing both positive numbers and negative numbers as binary numbers. See the table below.

2's Complement (MSB)			(LSB)	Decimal Number	L.OUT, R.OUT Pin Voltage TYP. (V) (Reference Values)[Note]
0111	1111	1111	1111	+32767	2.6
0111	1111	1111	1110	+32766	⋮
⋮	⋮	⋮	⋮	⋮	⋮
0000	0000	0000	0001	+1	⋮
0000	0000	0000	0000	0	1.6
1111	1111	1111	1111	–1	⋮
⋮	⋮	⋮	⋮	⋮	⋮
1000	0000	0000	0001	–32767	⋮
1000	0000	0000	0000	–32768	0.6

Note When $A.V_{DD}$ = 5.0 V

Values differ depending on IC fabrication variations, supply voltage fluctuations, and ambient temperature.

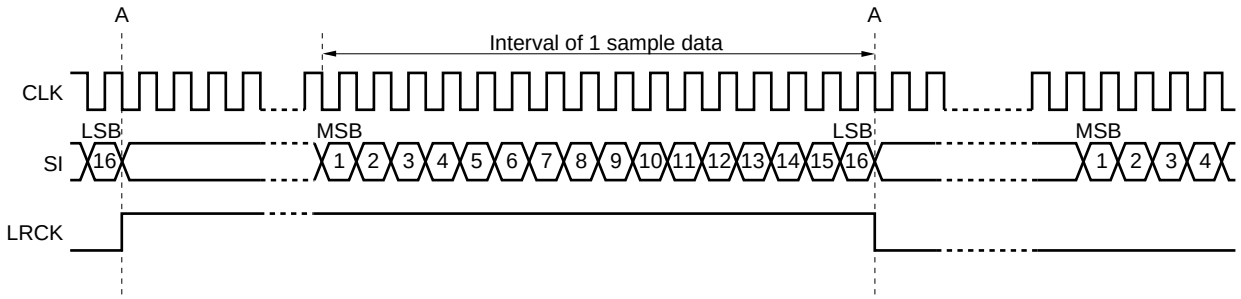
- Synchronize the (SI, LSI, RSI) data bit delimitations and the LRCK, WDCK reverse timing to the falling edge of CLK.
- CLK requires the input of 16 clocks between sample data (16 bits). Also, make the time interval for 1 bit the same as 1 clock cycle.

2.1 Supplying Clock to CLK even outside Sample Data Interval

2.1.1 Serial data input (Pin 1 is Low or Open)

Synchronize the reverse timing of LRCK with the falling edge of CLK upon completion of LSB input (Point A in **Figure 2-1**).

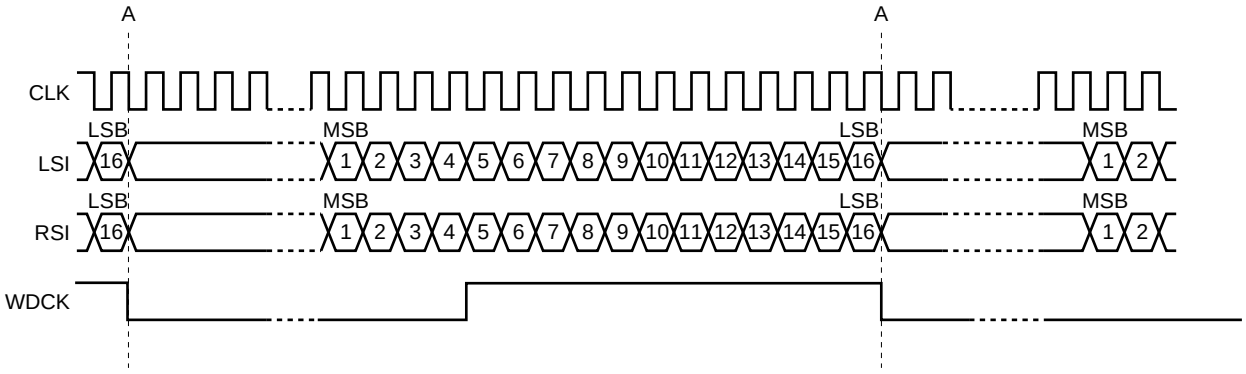
Figure 2-1 Timing Chart for Serial Data Input



2.1.2. Inputting parallel data (Pin 1 is High)

Synchronize the timing of the falling edge of WDCK with the falling edge of CLK upon completion of LSB input of data (LSI, RSI) (Point A in **Figure 2-2**.).

Figure 2-2 Parallel Data Input Timing Chart



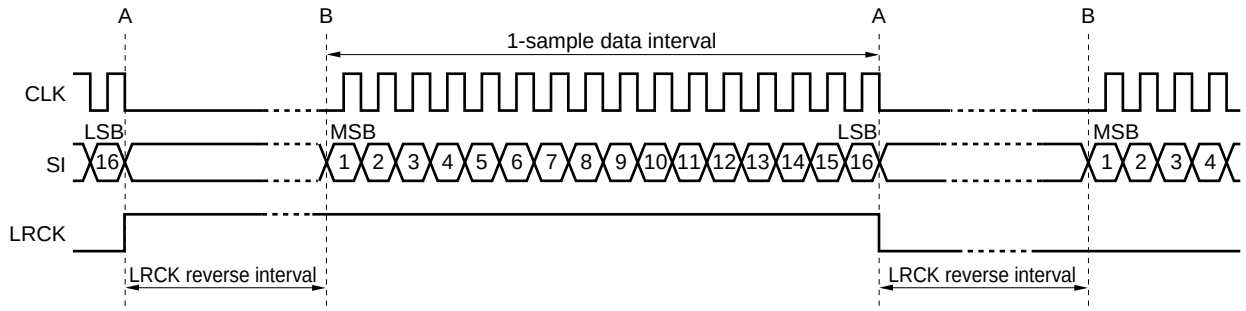
2.2 Supplying Clock to CLK only during Sample Data Interval

The analog outputs of the L.OUT and R.OUT pins are updated after the input of 4.5 clocks following data input. (See **4. ELECTRICAL CHARACTERISTICS, Timing Charts 1 and 2**.)

2.2.1 Inputting serial data (Pin 1 Low or Open)

Place the LRCK reverse timing between the falling edge of CLK at LSB input completion (Point A in **Figure 2-3**) and the next MSB input start time (Point B in **Figure 2-3**) (so as to include Points A and B).

Figure 2-3 Timing Chart of Serial Data Input

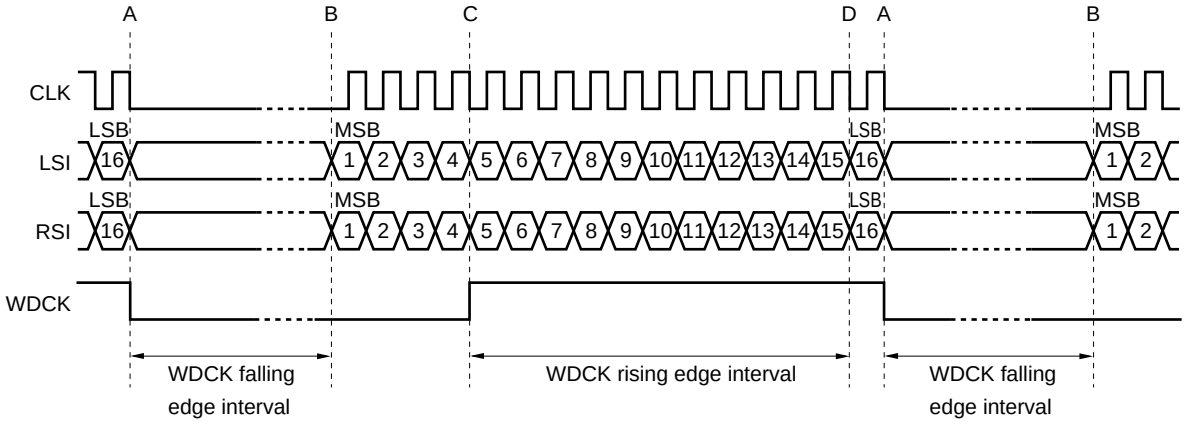


2.2.2 Inputting parallel data (Pin 1 High)

Place the WDCK falling edge timing between the falling edge of CLK at LSB input completion (Point A in **Figure 2-4**) and the next MSB input start time (Point B in **Figure 2-4**) (so as to include Points A and B).

Place the WDCK rising edge timing between the third falling edge of CLK from MSB input completion (Point C in **Figure 2-4**) and the falling edge of CLK upon LSB input start (Point D in **Figure 2-4**) (so as to include Points C and D).

Figure 2-4 Timing Chart of Parallel Data Input



3. USAGE CAUTIONS

Insertion of a muting circuit in the next stage after the μPD6376 is recommended.
If no muting circuit is inserted in the next stage, shock noise may be generated when power is applied.

Remarks 1. The practical value is 1.6±0.2 V (when $A.V_{DD}$ = 5.0 V) for the DC offset at the L.OUT and R.OUT pins (DC voltage value when the input data is 0000H (hexadecimal number)).

2. There is no minimum value for the conversion frequency. The μPD6376 can operate even when one sample data is input.

3. The minimum value of the full scale output voltage is a practical value of 1.7 V_{p-p}.

4. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Output pin voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
Logic input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Operating ambient temperature	T_A	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +125	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the device reliability may be impaired. The absolute maximum ratings are values that may physically damage the product. Be sure to use the product within the ratings.

Recommended Operating Range

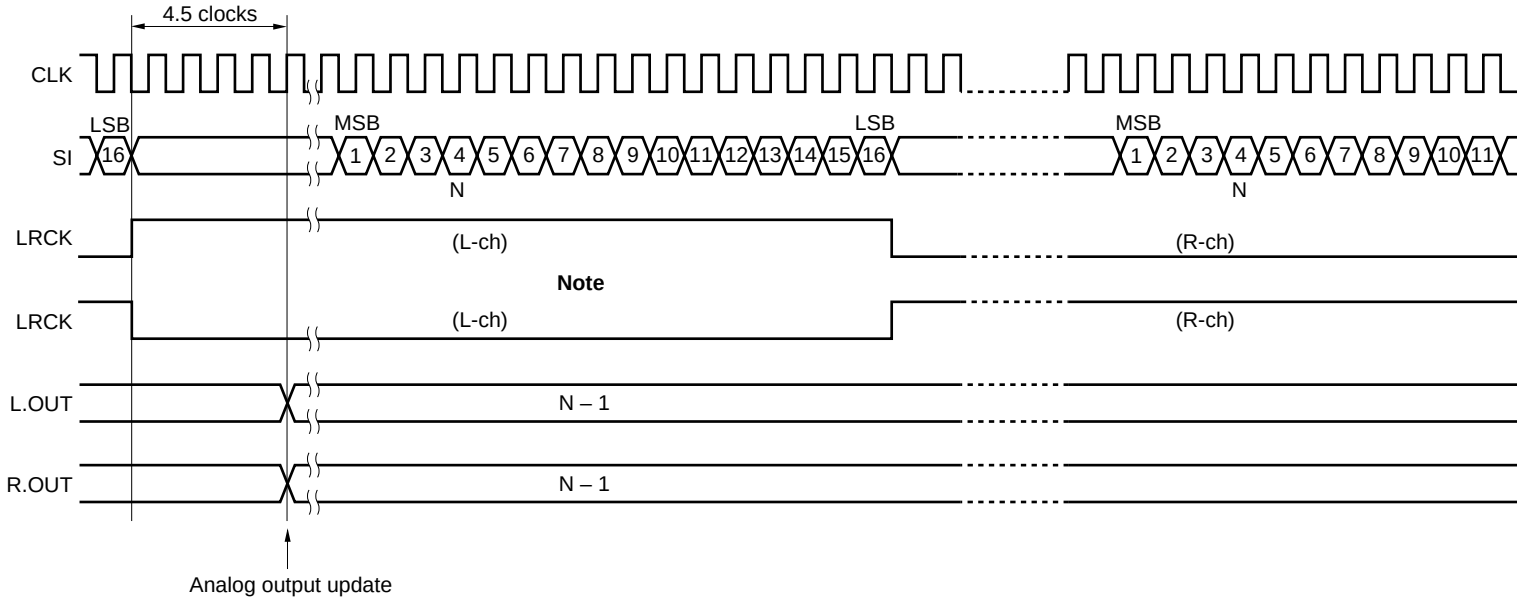
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Logic input voltage (High)	V_{IH}		0.7V_{DD}		V_{DD}	V
Logic input voltage (Low)	V_{IL}		0		0.3V_{DD}	V
Operating temperature range	T_A		–20	+25	+75	°C
Output load resistance	R_L	R.OUT or L.OUT pin	5			kΩ
Conversion frequency	f_S				400	kHz
Clock frequency	f_{CLK}				10	MHz
Clock pulse width	f_{SCK}		40			ns
SI, LRCK set time	t_{DC}		12			ns
SI, LRCK hold time	t_{CD}		12			ns

Electrical Characteristics (T_A = 25°C, V_{DD} = +5 V)

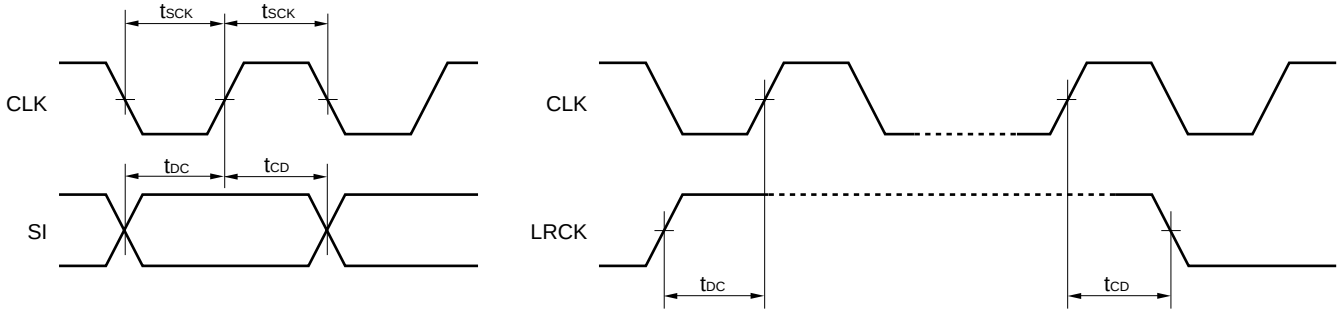
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RES			16		Bit
Total harmonic distortion 1	THD_1	f_{IN} = 1 kHz, 0 dB		0.04	0.09	%
Total harmonic distortion 2	THD_2	f_{IN} = 1 kHz, –20 dB		0.1	0.3	%
★ Full-scale output voltage	V_{FS}		1.7	2.0	2.3	V_{p-p}
Cross talk	C.T	0 dB per channel, f_{IN} = 1 kHz	85	95		dB
S/N ratio	S/N	JIS-A	96			dB
Dynamic range	D.R	f_{IN} = 1 kHz, –60 dB	92			dB
Circuit current	I_{DD}	f_{IN} = 1 kHz, 0 dB		6.0	12	mA

TIMING CHART 1

- When Pin 1 is Low or Open (serial input)

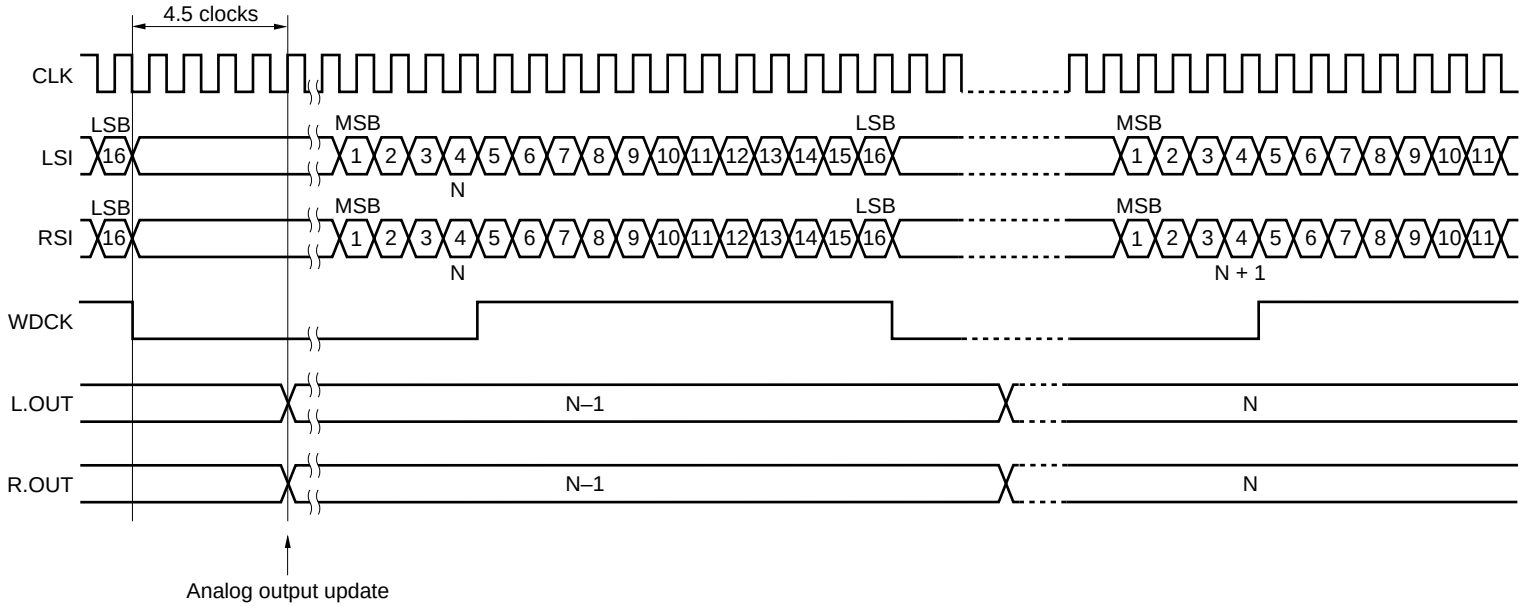


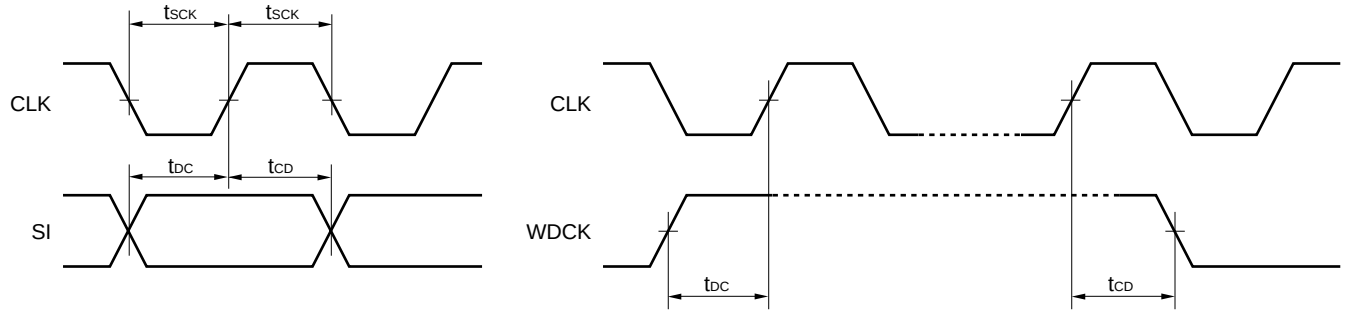
Note When the LRCK signal is High, set the LRSEL pin to Low to input L-ch data. When the LRCK signal is Low, set the LRSEL pin to High to input L-ch data.



TIMING CHART 2

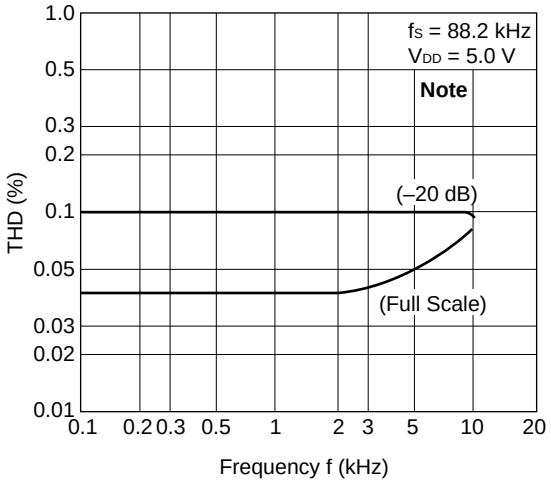
- When Pin 1 is High (parallel input)



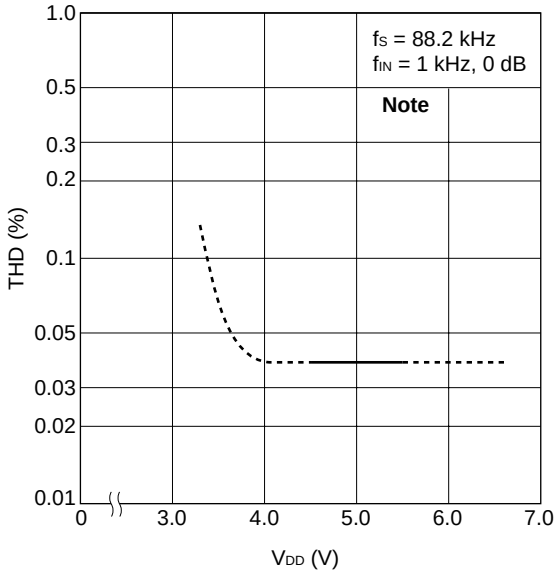


Typical Characteristics (T_A = 25°C)

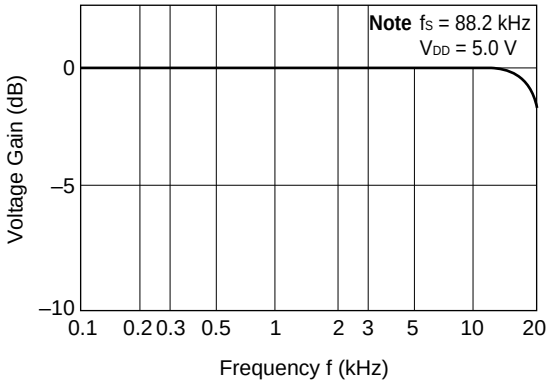
THD vs. Frequency Characteristics



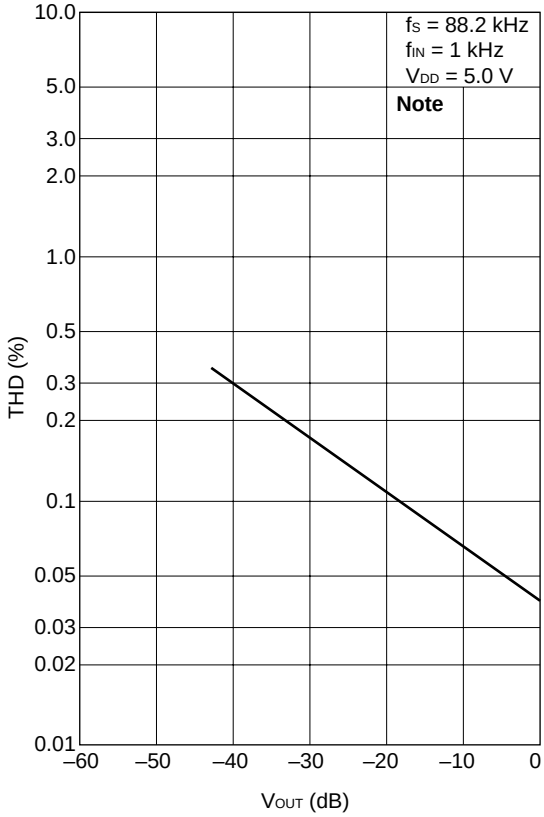
THD vs. V_{DD} Characteristics



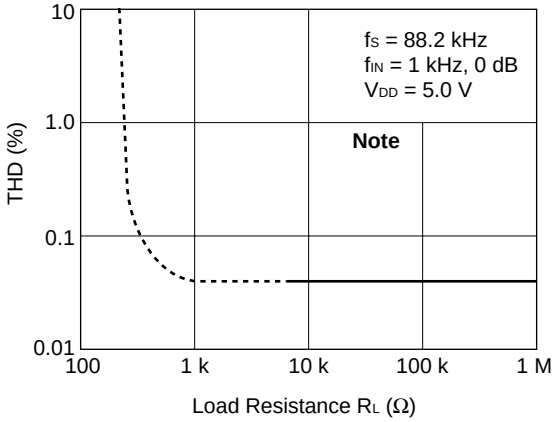
Voltage Gain vs. Frequency Characteristics



THD vs. V_{OUT} Characteristics



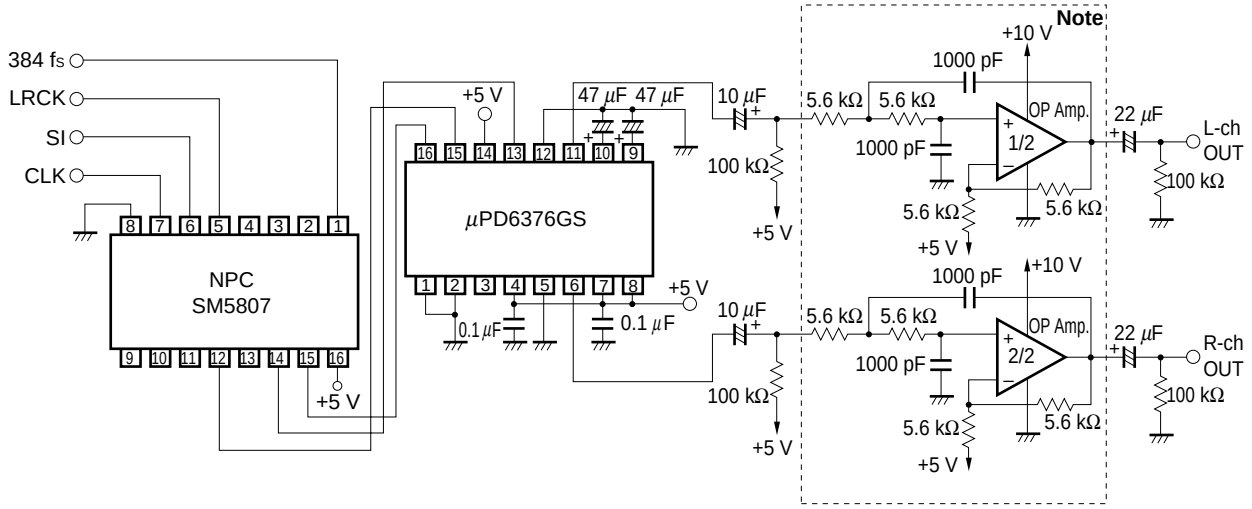
THD vs. R_L Characteristics



Note 20 kHz low-pass filter: 298BLR-010N (Toko) used

5. APPLICATION CIRCUIT EXAMPLE

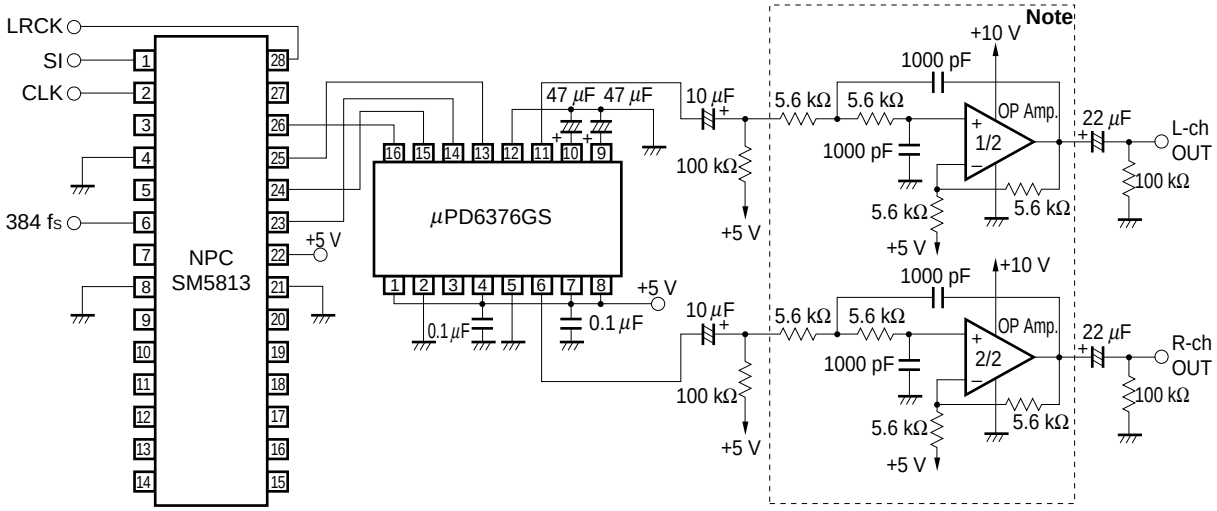
(1) fs to 4 fs mode (L/R data serial input mode)



Note Assuming secondary active LPF (Gain: K = 2, quality factor: Q = 1, cutoff frequency: $f_C \fallingdotseq 30$ kHz) oversampling, the attenuation characteristics are moderate. If oversampling is not performed, use a high-order filter.

Remark Operational amplifier (OP Amp.): μPC4558

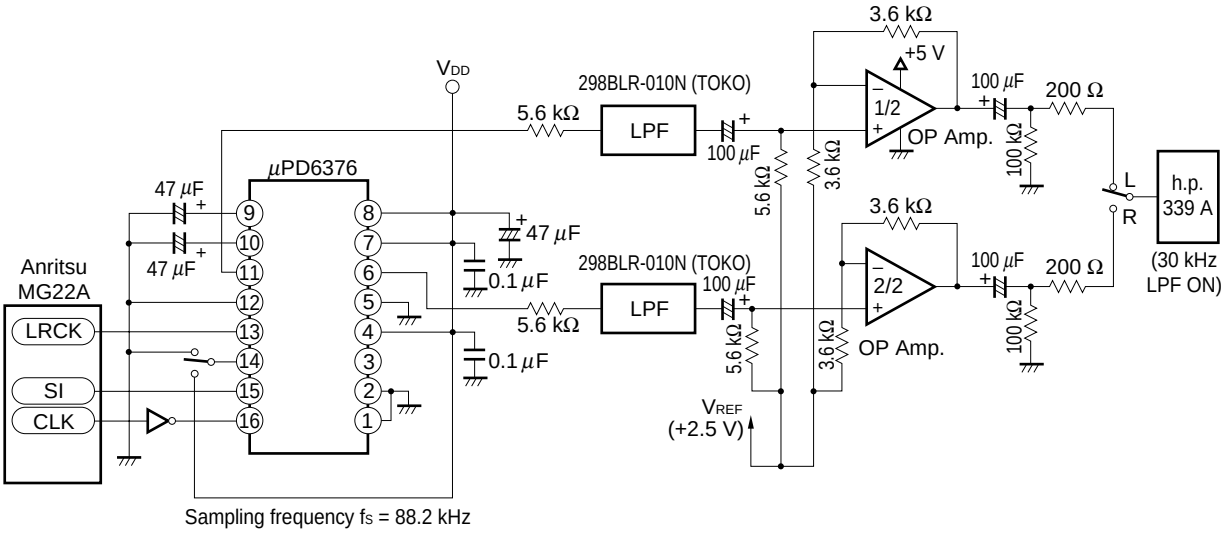
(2) 8 fs mode (L/R data parallel input mode)



Note Secondary active LPF (K = 2, Q = 1, $f_C \fallingdotseq 30$ kHz)

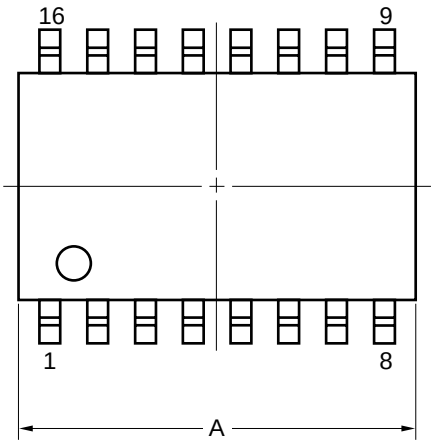
Remark Operational amplifier (OP Amp.): μPC4558

6. MEASURING CIRCUIT EXAMPLE

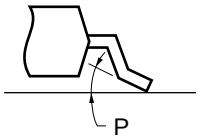


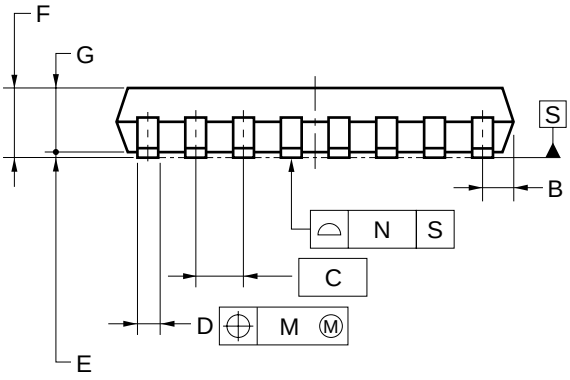
★ 7. PACKAGE DRAWINGS

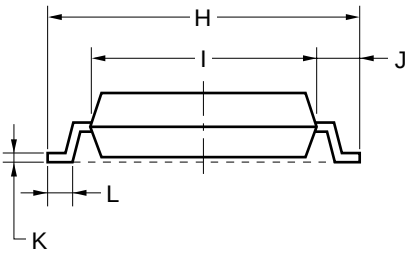
16-PIN PLASTIC SOP (7.62 mm (300))



detail of lead end







NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	10.2±0.2
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.65±0.15
G	1.55
H	7.7±0.3
I	5.6±0.2
J	1.1±0.2
K	$0.22^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P16GM-50-300B-6

8. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when performing soldering for the μPD6376.

For more detailed information, refer to the information document **Semiconductor Device Mounting Technology Manual** (C10535E).

For soldering methods and conditions other than the recommended conditions, please consult with an NEC sales representative.

Surface Mount Type Soldering Conditions

μPD6376GS: 16-pin Plastic SOP 7.62 mm (300)

Soldering Process	Soldering Conditions	Symbol
Infrared reflow	Peak package temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Once	IR30-00-1
VPS	Peak package temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Once	VP-15-00-1
Pin Partial heating	Pin temperature: 300°C or less, Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for pin partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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