NEC

MOS INTEGRATED CIRCUIT

# μPD6P4

## 4-BIT SINGLE-CHIP MICROCONTROLLER FOR INFRARED REMOTE CONTROL TRANSMISSION

### DESCRIPTION

The μPD6P4 is a microcontroller for infrared remote control transmitters which is provided with a one-time PROM as the program memory.

Because users can write programs for the μPD6P4, it is ideal for program evaluation and small-scale production of the application systems using the μPD63, 63A, or 64.

**When reading this document, also refer to the μPD63, 63A, 64 Data Sheet (U11371E).**

### FEATURES

- Program memory (one-time PROM): 2016 × 10 bits
- Data memory (RAM): 32 × 4 bits
- Built-in carrier generation circuit for infrared remote control
- 9-bit programmable timer: 1 channel
- Command execution time: 16 μs (when operating at $f_X$ = 4 MHz: ceramic oscillation)
- Stack level: 1 level (Stack RAM is for data memory RF as well.)
- I/O pins ($K_{I/O}$): 8 units
- Input pins ($K_I$): 4 units
- Sense input pin ($S_0$): 1 unit
- $S_1/\overline{LED}$ pin (I/O): 1 unit (In output mode, this is the remote control transmission display pin.)
- Power supply voltage: $V_{DD}$ = 2.2 to 3.6 V (at $f_X$ = 4 MHz)
  $V_{DD}$ = 2.7 to 3.6 V (at $f_X$ = 8 MHz)
- Operating ambient temperature: $T_A$ = –20 to +70°C
- Oscillator frequency: $f_X$ = 2.4 to 8 MHz
- POC circuit

### APPLICATION

Infrared remote control transmitter (for AV and household electric appliances)



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## ORDERING INFORMATION

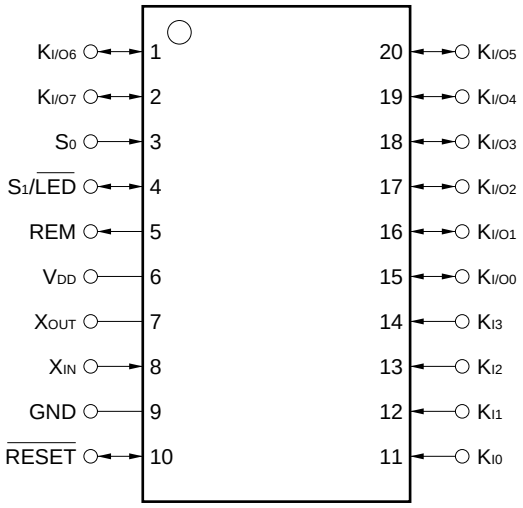
| Part Number | Package |
|---|---|
| μPD6P4GS | 20-pin plastic SOP (300 mil) |

## PIN CONFIGURATION (TOP VIEW)

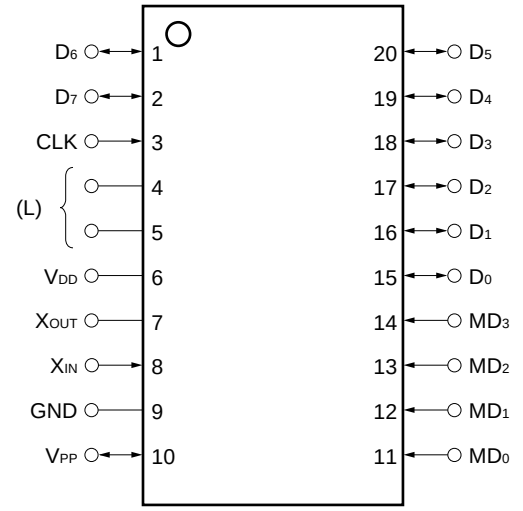
**20-pin Plastic SOP (300 mil)**

- **μPD6P4GS**

**(1) Normal operating mode**

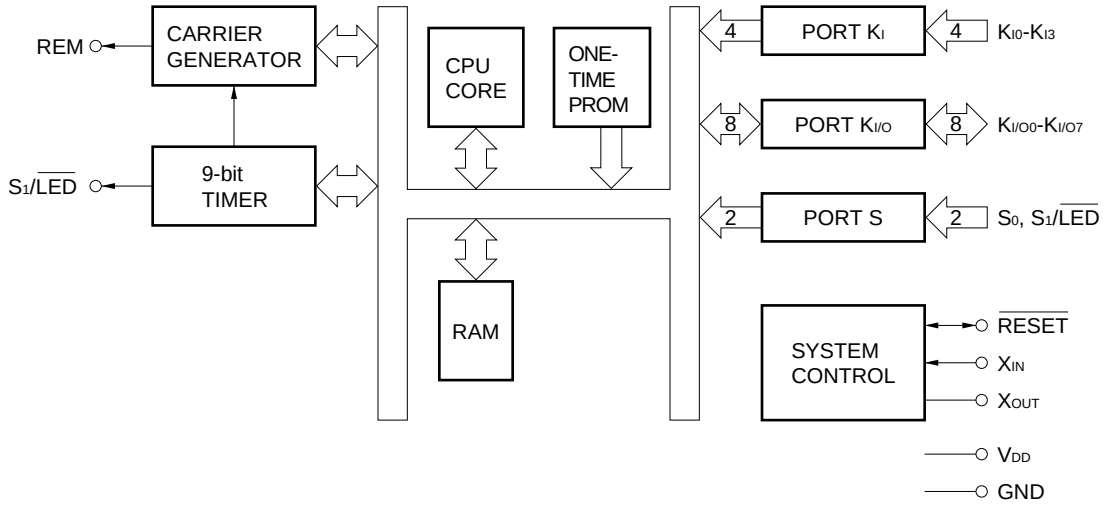



**(2) PROM programming mode**




**Caution Round brackets ( ) indicate the pins not used in the PROM programming mode.**
**L : Connect each of these pins to GND via a pull-down resistor.**

## BLOCK DIAGRAM




## LIST OF FUNCTIONS

| Item | μPD6P4 |
|---|---|
| ROM capacity | 2016 × 10 bits<br>One-time PROM |
| RAM capacity | 32 × 4 bits |
| Stack | 1 level (shared with RF of RAM) |
| I/O pin | Key input ($K_I$) : 4 pins<br>Key I/O ($K_{I/O}$) : 8 pins<br>Key expansion input ($S_0$, $S_1$) : 2 pins<br>Remote control transmitter display output ($\overline{LED}$) : 1 pin (shared with $S_1$ pin) |
| Number of keys | 32 keys<br>48 keys (when expanded by key expansion input)<br>96 keys (when expanded by key expansion input and diode) |
| Clock frequency | Ceramic oscillation<br>$f_X$ = 2.4 to 4 MHz<br>$f_X$ = 4 to 8 MHz**Note** |
| Instruction execution time | 16 μs (at $f_X$ = 4 MHz) |
| Carrier frequency | $f_X/8$, $f_X/16$, $f_X/64$, $f_X/96$, $f_X/128$, $f_X/192$, no carrier (high level) |
| Timer | 9-bit programmable timer : 1 channel |
| POC circuit | Provided |
| Supply voltage | $V_{DD}$ = 2.2 to 3.6 V ($f_X$ = 2.4 to 4 MHz), $V_{DD}$ = 2.7 to 3.6 V ($f_X$ = 4 to 8 MHz) |
| Operating ambient temperature | $T_A$ = –20 to +70°C |
| Package | 20-pin plastic SOP (300 mil) |

**Note** It is necessary to design the application circuit so that the $\overline{RESET}$ pin goes low at a supply voltage of less than 2.7 V.

## TABLE OF CONTENTS

## 1. PIN FUNCTIONS

### 1.1 Normal Operating Mode

| Pin No. | Symbol | Function | Output Format | When Reset |
|---|---|---|---|---|
| 1<br>2<br>15-20 | $K_{I/O0}$-$K_{I/O7}$ | These pins refer to the 8-bit I/O ports. I/O switching can be made in 8-bit units.<br>In INPUT mode, a pull-down resistor is added. In OUTPUT mode, they can be used as the key scan output of the key matrix. | CMOS push-pull[Note 1] | High-level output |
| 3 | $S_0$ | Refers to the input port.<br>Can also be used as the key return input of the key matrix.<br>In INPUT mode, the availability of the pull-down resistor of the $S_0$ and $S_1$ ports can be specified by software in terms in 2-bit units.<br>If INPUT mode is canceled by software, this pin is placed in OFF mode and enters the high-impedance state. | — | High-impedance (OFF mode) |
| 4 | $S_1/\overline{LED}$ | Refers to the I/O port.<br>In INPUT mode ($S_1$), this pin can also be used as the key return input of the key matrix.<br>The availability of the pull-down resistor of the $S_0$ and $S_1$ ports can be specified by software in 2-bit units. In OUTPUT mode ($\overline{LED}$), it becomes the remote control transmission display output (active low). When the remote control carrier is output from the REM output, this pin outputs the low level from the $\overline{LED}$ output synchronously with the REM signal. | CMOS push-pull | High-level output ($\overline{LED}$) |
| 5 | REM | Refers to the infrared remote control transmission output. The output is active high.<br>Carrier frequency: $f_X/8$, $f_X/64$, $f_X/96$, high-level,<br>$f_X/16$, $f_X/128$, $f_X/192$ (usable on software) | CMOS push-pull | Low-level output |
| 6 | $V_{DD}$ | Refers to the power supply. | — | — |
| 7<br>8 | $X_{OUT}$<br>$X_{IN}$ | These pins are connected to system clock ceramic resonators. | — | Low level (oscillation stopped) |
| 9 | GND | Refers to the ground. | — | — |
| 10 | $\overline{RESET}$ | Normally, this pin is a system reset input. By inputting a low level, the CPU can be reset. When resetting with the POC circuit a low level is output. A pull-up resistor is incorporated. | — | — |
| 11-14 | $K_{I0}$-$K_{I3}$[Note 2] | These pins refer to the 4-bit input ports.<br>They can be used as the key return input of the key matrix.<br>The use of the pull-down resistor can be specified by software in 4-bit units. | — | Input (low-level) |

**Notes 1.** Be careful about this because the drive capability of the low-level output side is held low.

**2.** In order to prevent malfunction, be sure to input a low level to more than one of pins $K_{I0}$ to $K_{I3}$ when reset is released (when $\overline{RESET}$ pin changes from low level to high level, or POC is released due to supply voltage startup).

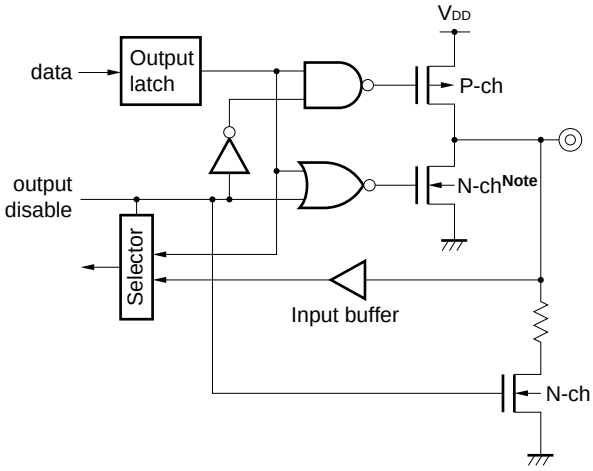
## 1.2 PROM Programming Mode

| Pin No. | Symbol | Function | I/O |
|---|---|---|---|
| 1, 2<br>15-20 | $D_0$-$D_7$ | 8-bit data input/output when writing/verifying program memory | I/O |
| 3 | CLK | Clock input for updating address when writing/verifying program memory | Input |
| 6 | $V_{DD}$ | Power Supply.<br>Supply +6 V to this pin when writing/verifying program memory. | – |
| 7 | $X_{OUT}$ | Clock necessary for writing program memory. Connect 4 MHz ceramic resonator to these pins. | – |
| 8 | $X_{IN}$ | | Input |
| 9 | GND | GND | – |
| 10 | $V_{PP}$ | Supplies voltage for writing/verifying program memory.<br>Apply +10 V to this pin. | – |
| 11-14 | $MD_0$-$MD_3$ | Input for selecting operation mode when writing/verifying program memory. | Input |

### 1.3 INPUT/OUTPUT Circuits of Pins

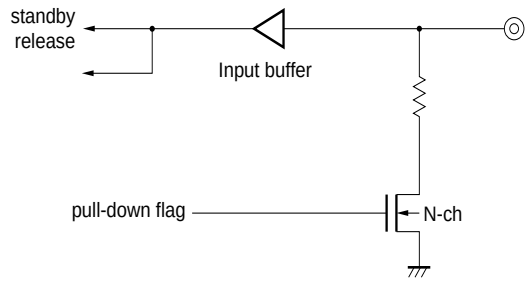
The input/output circuits of the μPD6P4 pins are shown in partially simplified forms below.

**(1) $K_{I/O0}$-$K_{I/O7}$**

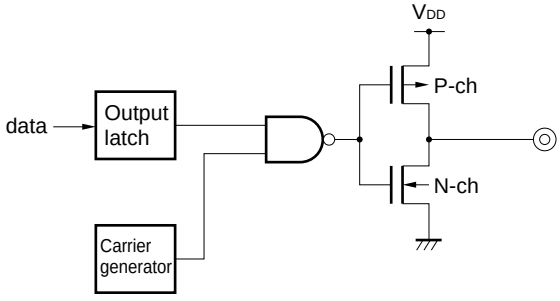



**Note** The drive capability is held low.

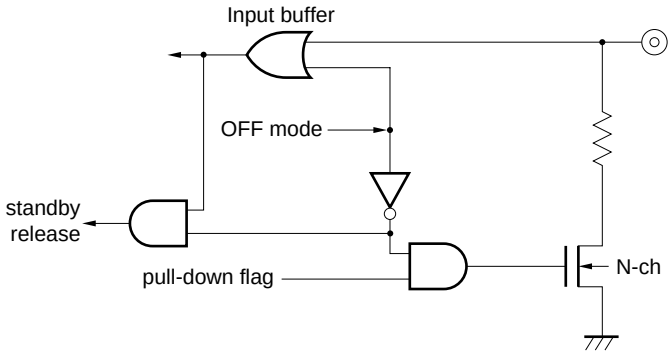
**(2) $K_{I0}$-$K_{I3}$**



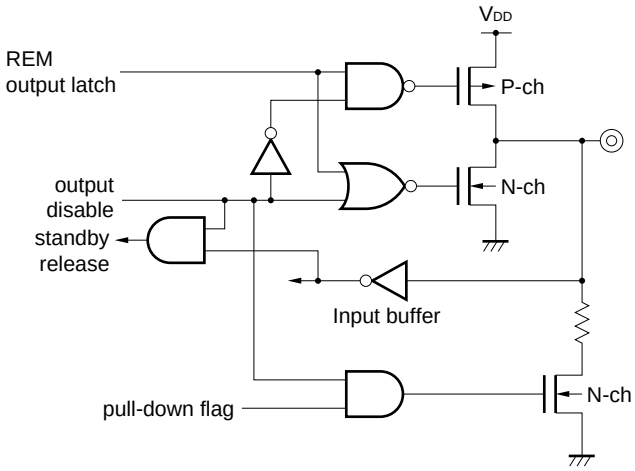

**(3) REM**



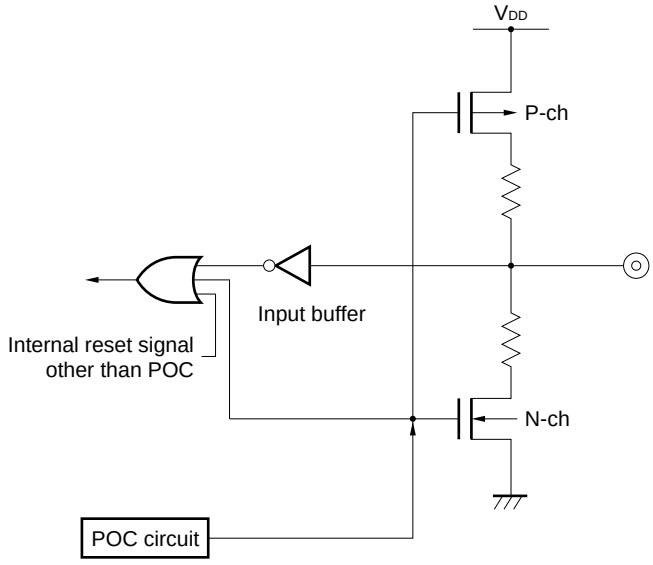

**(4) $S_0$**




**(5) $S_1/\overline{LED}$**




**(6) $\overline{RESET}$**



## 1.4 Dealing with Unused Pins

The following connections are recommended for unused pins in the normal operation mode.

**Table 1-1. Connections for Unused Pins**

| Pin | | Connection | |
|---|---|---|---|
| | | Inside the microcontroller | Outside the microcontroller |
| $K_{I/O}$ | INPUT mode | — | Open |
| | OUTPUT mode | High-level output | |
| REM | | — | |
| $S_1/\overline{LED}$ | | OUTPUT mode ($\overline{LED}$) setting | |
| $S_0$ | | OFF mode setting | Directly connected to GND |
| $K_I$ | | — | |
| $\overline{RESET}$ Note | | Built-in POC circuit | Open |

**Note** If the circuit is an applied one requiring high reliability, be sure to design it in such a manner that the $\overline{RESET}$ signal is entered externally.

**Caution The I/O mode and the terminal output level are recommended to be fixed by setting them repeatedly in each loop of the program.**

## 1.5 Notes on Using $K_I$ Pin at Reset

In order to prevent malfunction, be sure to input a low level to more than one of pins $K_{I0}$ to $K_{I3}$ when reset is released (when $\overline{RESET}$ pin changes from low level to high level, or POC is released due to supply voltage startup).

## 2. DIFFERENCES AMONG μPD63, 63A, 64, AND μPD6P4

Table 2-1 shows the differences among the μPD63, 63A, 64, and μPD6P4.

The only differences among these models are the program memory, supply voltage, system clock frequency, oscillation stabilization wait time, and POC circuit (mask option), and the CPU function and internal peripheral hardware are the same.

The electrical characteristics also differ slightly. For the electrical characteristics, refer to the Data Sheet of each model.

**Table 2-1. Differences among μPD63, 63A, 64, and μPD6P4 (1/2)**

**(1) When POC circuit (mask option) is provided to μPD63, 63A, and 64**

| Item | μPD6P4 | μPD63 | μPD63A | μPD64 |
|---|---|---|---|---|
| ROM | One-time PROM | Mask ROM | | |
| | 2016 × 10 bits (000H to 7DFH) | 512 × 10 bits (000H to 1FFH) | 768 × 10 bits (000H to 2FFH) | 1002 × 10 bits (000H to 3E9H) |
| Program counter (PC) | 11 bits | 10 bits | | |
| Address stack register (ASR) | | | | |
| Data pointer (DP) | | | | |
| Oscillation stabilization wait time | | | | |
| • On releasing STOP mode by release condition | 286/$f_X$ | 52/$f_X$ | | |
| • On releasing STOP or HALT mode by $\overline{\text{RESET}}$ input and at reset | 478/$f_X$ to 926/$f_X$ | 246/$f_X$ to 694/$f_X$ | | |
| $V_{PP}$ pin and operating mode select pin | Provided | Not provided | | |
| Electrical characteristics | Some electrical characteristics, such as data retention voltage and current consumption, differ. For details, refer to Data Sheet of each model. | | | |

**Table 2-1. Differences among μPD63, 63A, 64, and μPD6P4 (2/2)**

**(2) When POC circuit (mask option) is not provided to μPD63, 63A, and 64**

| Item | μPD6P4 | μPD63 | μPD63A | μPD64 |
|---|---|---|---|---|
| ROM | One-time PROM | Mask ROM | | |
| | 2016 × 10 bits (000H to 7DFH) | 512 × 10 bits (000H to 1FFH) | 768 × 10 bits (000H to 2FFH) | 1002 × 10 bits (000H to 3E9H) |
| Program counter (PC) | 11 bits | 10 bits | | |
| Address stack register (ASR) | | | | |
| Data pointer (DP) | | | | |
| Oscillation stabilization wait time | | | | |
| • On releasing STOP mode by release condition | 286/$f_X$ | 52/$f_X$ | | |
| • $\overline{\text{On releasing STOP or HALT mode by RESET input and at reset}}$ | 478/$f_X$ to 926/$f_X$ | 246/$f_X$ to 694/$f_X$ | | |
| $V_{PP}$ pin and operating mode select pin | Provided | Not provided | | |
| POC circuit | Incorporated | Not provided | | |
| Supply voltage | $V_{DD}$ = 2.2 to 3.6 V ($T_A$ = –20 to +70°C) | $V_{DD}$ = 1.8 to 3.6 V ($T_A$ = –40 to +85°C) | | |
| System clock frequency | • $f_X$ = 2.4 to 4 MHz<br>• $f_X$ = 4 to 8 MHz[Note] | • $f_X$ = 2.4 to 4 MHz<br>• $f_X$ = 2.4 to 8 MHz ($V_{DD}$ = 2.2 to 3.6 V) | | |
| Electrical characteristics | Some electrical characteristics, such as data retention voltage and current consumption, differ. For details, refer to Data Sheet of each model. | | | |

**Note** It is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.7 V.

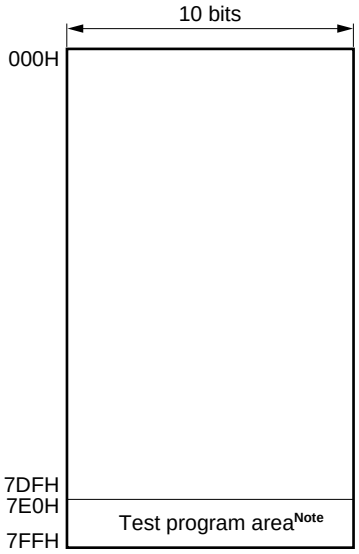
## 2.1 Program Memory (One-time PROM) ... 2016 steps × 10 bits

This one-time PROM is configured with 10 bits per step and is addressed by the program counter.

The program memory stores programs and table data.

The 32 steps from addresses 7E0H through 7FFH constitute a test program area and must not be used.

**Figure 2-1. Program Memory Map**




**Note** Even if execution jumps to the test program area by mistake, it returns to address 000H.

## 2.2 Program Counter (PC) ... 11 bits

The program counter is a binary counter that holds the address information of the program memory.

**Figure 2-2. Program Counter Configuration**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PC | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |

The program counter stores the address of the instruction to be executed next. Usually, each time an instruction has been executed, the contents of the PC are automatically incremented according to the length of the instruction (number of bytes).

If a jump instruction (JMP, JC, JNC, JF, or JNF) is executed, however, the jump destination address written as the operand is stored to the PC.

When a subroutine call instruction (CALL) is executed, the contents of the PC at that time are saved to the address stack register (ASR), and the call destination address written as the instruction operand is stored to the PC. If a return instruction (RET) is executed after the CALL instruction has been executed, the address saved to the ASR is restored to the PC.

At reset, the value of the PC is reset to “000H”.

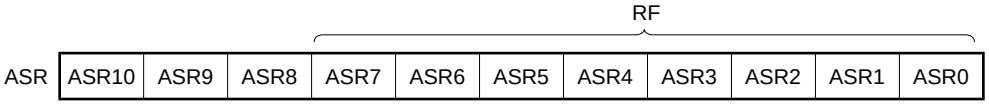
## 2.3 Address Stack Register (ASR (RF)) ... 11 bits

The address stack register saves an address to which program execution is to return after a subroutine call instruction has been executed. The low-order 8 bits of this register are located in the RF area of the data memory as a multiplexed RAM area. The value of ASR is retained even after the RET instruction has been executed.

At reset, the ASR holds the previous data (the value of the ASR is undefined on power application).

**Caution The high-order 3 bits of the ASR are undefined if the RF is accessed as a data memory area.**

**Figure 2-3. Address Stack Register Configuration**



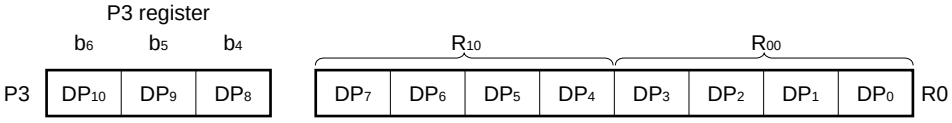
## 2.4 Data Pointer (DP) ... 11 Bits

The ROM data table can be referenced by setting the ROM address in the data pointer to call the ROM contents.

The low-order 8 bits of the ROM address are specified by R0 of the data memory, and the high-order 3 bits by bits 4, 5, and 6 of the P3 register.

When reset, the pointer contents become “000H”.

**Figure 2-4. Data Pointer Configuration**



## 2.5 Control Register 0 (P3)

Control register 0 consists of 8 bits. This following bits of this register can be controlled.

At reset, the value of this register is set to 0000 0011B.

**Table 2-2. Control Register 0 (P3)**

| Bit | | $b_7$ | $b_6$ | $b_5$ | $b_4$ | $b_3$ | $b_2$ | $b_1$ | $b_0$ |
|---|---|---|---|---|---|---|---|---|---|
| Name | | – | DP (data pointer) | | | TCTL | CARY | $MOD_1$ | $MOD_0$ |
| | | | $DP_{10}$ | $DP_9$ | $DP_8$ | | | | |
| Set value | 0 | Fixed to | 0 | 0 | 0 | 1/1 | ON | Refer to **Table 2-3**. | |
| | 1 | "0" | 1 | 1 | 1 | 1/2 | OFF | | |
| At reset | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

$b_0$, $b_1$ ..... Specify the carrier frequency and duty factor of REM output.

$b_2$ ..... Specifies whether a carrier whose frequency is specified by $b_0$ and $b_1$ is used.
"0" = ON (carrier), "1" = OFF (no carrier, high level)

$b_3$ ..... Changes the carrier frequency and division ratio of the timer clock.
"0" = 1/1 (carrier frequency: value specified by $b_0$ and $b_1$, timer clock: $f_X$/64)
"1" = 1/2 (carrier frequency: 1/2 of value specified by $b_0$ and $b_1$, timer clock: $f_X$/128)

**Table 2-3. Setting of Timer Clock and Carrier Frequency**

| $b_3$ | $b_2$ | $b_1$ | $b_0$ | Timer Clock | Carrier Frequency (duty factor) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $f_X$/64 | $f_X$/8 (Duty 1/2) |
| | | 0 | 1 | | $f_X$/64 (Duty 1/2) |
| | | 1 | 0 | | $f_X$/96 (Duty 1/2) |
| | | 1 | 1 | | $f_X$/96 (Duty 1/3) |
| | 1 | × | × | | No carrier (high level) |
| 1 | 0 | 0 | 0 | $f_X$/128 | $f_X$/16 (Duty 1/2) |
| | | 0 | 1 | | $f_X$/128 (Duty 1/2) |
| | | 1 | 0 | | $f_X$/192 (duty 1/2) |
| | | 1 | 1 | | $f_X$/192 (Duty 1/3) |
| | 1 | × | × | | No carrier (high level) |

$b_4$, $b_5$, $b_6$ .... Specify the high-order 3 bits ($DP_8$, $DP_9$, and $DP_{10}$) of the data pointer of ROM.

**Remark** ×: don't care

## 3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD6P4 is a one-time PROM of 2016 × 10 bits.

To write or verify this program memory, the pins shown in Table 3-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

**Table 3-1. Pins Used to Write/Verify Program Memory**

| Pin Name | Function |
|---|---|
| $V_{PP}$ | Supplies voltage when writing/verifying program memory.<br>Apply +10 V to this pin. |
| $V_{DD}$ | Power supply.<br>Supply +6 V to this pin when writing/verifying program memory. |
| CLK | Inputs clock to update address when writing/verifying program memory.<br>By inputting pulse four times to CLK pin, address of program memory is updated. |
| $MD_0$-$MD_3$ | Input to select operation mode when writing/verifying program memory. |
| $D_0$-$D_7$ | Inputs/outputs 8-bit data when writing/verifying program memory. |
| $X_{IN}$, $X_{OUT}$ | Clock necessary for writing program memory. Connect 4 MHz ceramic resonator to this pin. |

### 3.1 Operating Mode When Writing/Verifying Program Memory

The μPD6P4 is set in the program memory write/verify mode when +6 V is applied to the $V_{DD}$ pin and +10 V is applied to the $V_{PP}$ pin after the μPD6P4 has been in the reset status ($V_{DD}$ = 5 V, $V_{PP}$ = 0 V) for a specific time. In this mode, the operating modes shown in Table 3-2 can be set by setting the $MD_0$ through $MD_3$ pins. Connect all the pins other than those shown in Table 3-1 to GND via pull-down resistor.

**Table 3-2. Setting Operation Mode**

| Setting of Operating Mode | | | | | | Operation Mode |
|---|---|---|---|---|---|---|
| $V_{PP}$ | $V_{DD}$ | $MD_0$ | $MD_1$ | $MD_2$ | $MD_3$ | |
| +10V | +6V | H | L | H | L | Clear program address to 0 |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | × | H | H | Program inhibit mode |

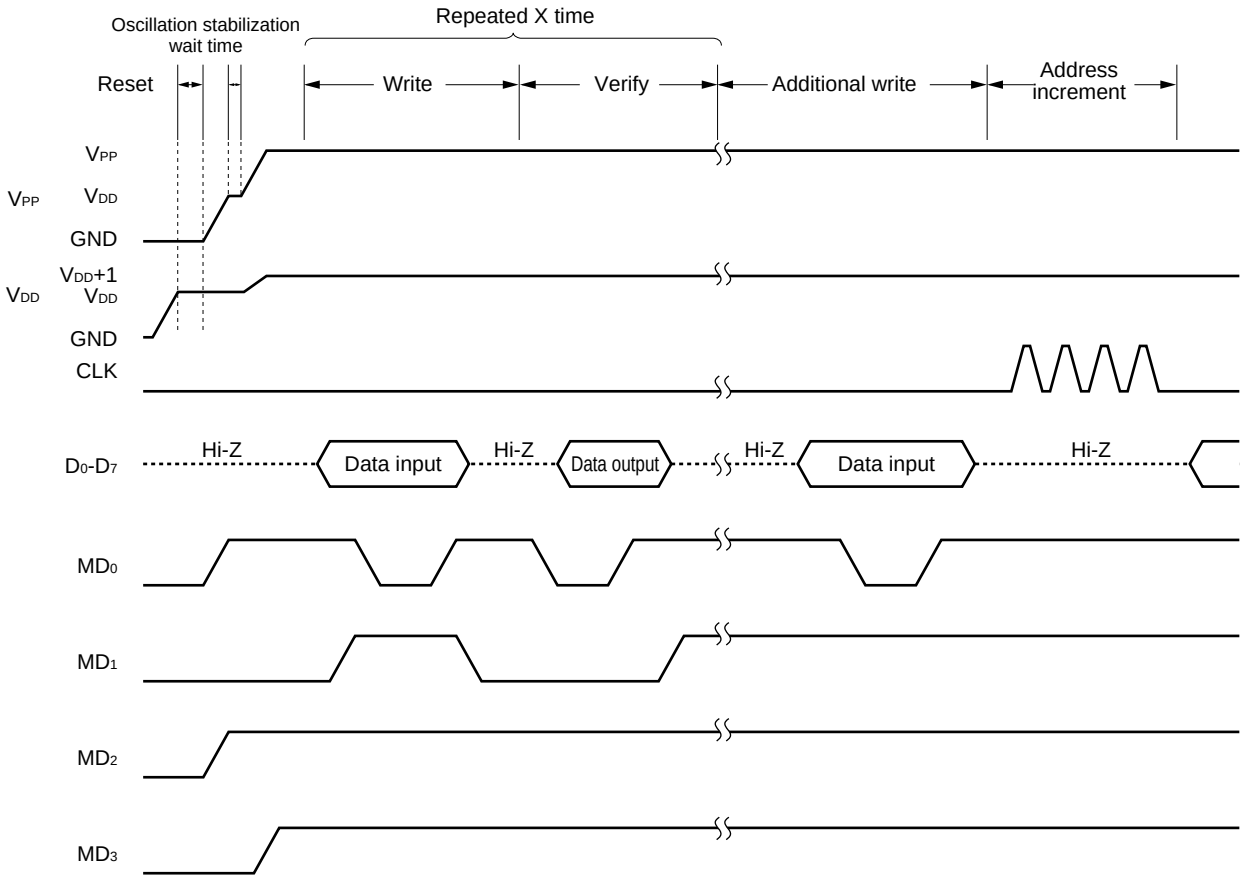
×: don't care (L or H)

### 3.2 Program Memory Writing Procedure

The program memory is written at high speed in the following procedure.

(1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
(2) Supply 5 V to the $V_{DD}$ pin. Keep the $V_{PP}$ pin low.
(3) Supply 5 V to the $V_{PP}$ pin after waiting for 10 μs.
(4) Wait for 2 ms until oscillation of the ceramic resonator connected across the $X_{IN}$ and $X_{OUT}$ pins stabilizes.
(5) Set the program memory address 0 clear mode by using the mode setting pins.
(6) Supply 6 V to $V_{DD}$ and 10 V to $V_{PP}$.
(7) Set the program inhibit mode.
(8) Write data to the program memory in the 1-ms write mode.
(9) Set the program inhibit mode.
(10) Set the verify mode. If the data have been written to the program memory, proceed to (11). If not, repeat steps (8) through (10).
(11) Additional writing of (number of times of writing in (8) through (10): X) × 1 ms.
(12) Set the program inhibit mode.
(13) Input a pulse to the CLK pin four times to update the program memory address (+1).
(14) Repeat steps (8) through (13) up to the last address.
(15) Set the 0 clear mode of the program memory address.
(16) Change the voltages on the $V_{DD}$ and $V_{PP}$ pins to 5 V.
(17) Turn off power.

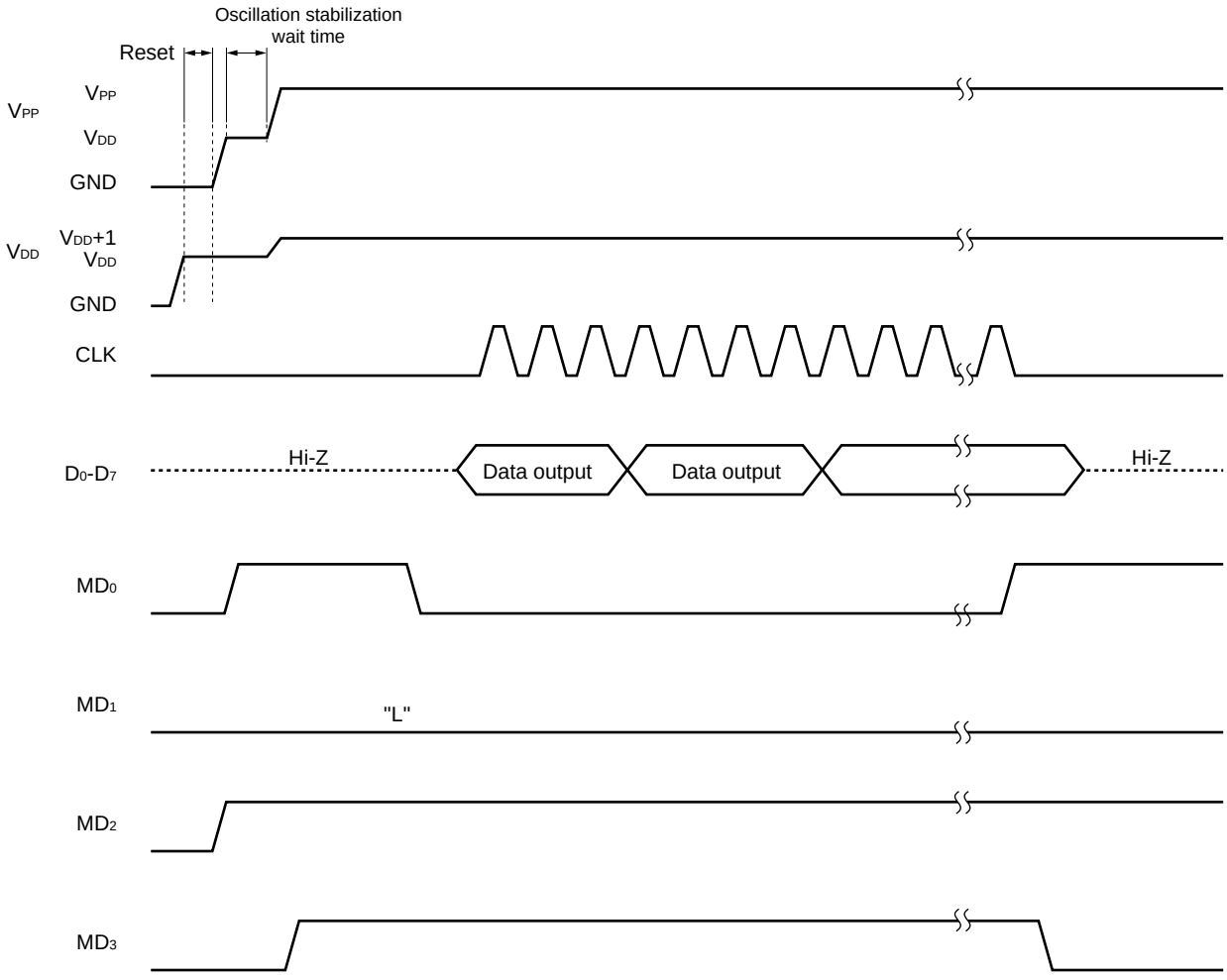
The following figure illustrates steps (2) through (13) above.



### 3.3 Program Memory Reading Procedure

(1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
(2) Supply 5 V to the $V_{DD}$ pin. Keep the $V_{PP}$ pin low.
(3) Supply 5 V to the $V_{PP}$ pin after waiting for 10 μs.
(4) Wait for 2 ms until oscillation of the ceramic resonator connected across the $X_{IN}$ and $X_{OUT}$ pins stabilizes.
(5) Set the program memory address 0 clear mode by using the mode setting pins.
(6) Supply 6 V to $V_{DD}$ and 10 V to $V_{PP}$.
(7) Set the program inhibit mode.
(8) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
(9) Set the program inhibit mode.
(10) Set the program memory address 0 clear mode.
(11) Change the voltage on the $V_{DD}$ and $V_{PP}$ pins to 5 V.
(12) Turn off power.

The following figure illustrates steps (2) through (10) above.



## 4. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings ($T_A$ = +25 °C)

| Parameter | Symbol | Test Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| | $V_{PP}$ | | | –0.3 to +11 | V |
| Input voltage | $V_I$ | $K_{I/O}$, $K_I$, $S_0$, $S_1$, $\overline{RESET}$ | | –0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| High-level output current | $I_{OH}$**Note** | REM | Peak value | –30 | mA |
| | | | rms | –20 | mA |
| | | $\overline{LED}$ | Peak value | –7.5 | mA |
| | | | rms | –5 | mA |
| | | One $K_{I/O}$ pin | Peak value | –13.5 | mA |
| | | | rms | –9 | mA |
| | | Total of $\overline{LED}$ and $K_{I/O}$ pins | Peak value | –18 | mA |
| | | | rms | –12 | mA |
| Low-level output current | $I_{OL}$**Note** | REM | Peak value | 7.5 | mA |
| | | | rms | 5 | mA |
| | | $\overline{LED}$ | Peak value | 7.5 | mA |
| | | | rms | 5 | mA |
| Operating ambient temperature | $T_A$ | | | –20 to +70 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Note** Work out the rms with: [rms] = [Peak value] $\times\sqrt{Duty}$.

**Caution Product quality may suffer if the absolute rating is exceeded for any parameter, even momentarily. In other words, an absolute maxumum rating is a value at which the possibility of psysical damage to the product cannnot be ruled out. Care must therefore be taken to ensure that the these ratings are not exceeded during use of the product.**

### Recommended Power Supply Voltage Range ($T_A$ = –20 to +70°C)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | $f_X$ = 2.4 to 4 MHz | 2.2 | 3.0 | 3.6 | V |
| | | $f_X$ = 4 to 8 MHz**Note** | 2.7 | 3.0 | 3.6 | V |

**Note** It is necessary to design the application circuit so that the $\overline{RESET}$ pin goes low when the supply voltage is less than 2.7 V.

**DC Characteristics ($T_A$ = –20 to +70°C, $V_{DD}$ = 2.2 to 3.6 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH1}$ | $\overline{RESET}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | $K_{I/O}$ | | 0.65 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | $K_I$, $S_0$, $S_1$ | | 0.65 $V_{DD}$ | | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL1}$ | $\overline{RESET}$ | | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL2}$ | $K_{I/O}$ | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL3}$ | $K_I$, $S_0$, $S_1$ | | 0 | | 0.15 $V_{DD}$ | V |
| High-level input leakage current | $I_{LH1}$ | $K_I$<br>$V_I$ = $V_{DD}$, pull-down resistor not incorporated | | | | 3 | μA |
| | $I_{LH2}$ | $S_0$, $S_1$<br>$V_I$ = $V_{DD}$, pull-down resistor not incorporated | | | | 3 | μA |
| Low-level input leakage current | $I_{UL1}$ | $K_I$ $V_I$ = 0 V | | | | –3 | μA |
| | $I_{UL2}$ | $K_{I/O}$ $V_I$ = 0 V | | | | –3 | μA |
| | $I_{UL3}$ | $S_0$, $S_1$ $V_I$ = 0 V | | | | –3 | μA |
| High-level output voltage | $V_{OH1}$ | REM, $\overline{LED}$, $K_{I/O}$ | $I_{OH}$ = –0.3 mA | 0.8 $V_{DD}$ | | | V |
| Low-level output voltage | $V_{OL1}$ | REM, $\overline{LED}$ | $I_{OL}$ = 0.3 mA | | | 0.3 | V |
| | $V_{OL2}$ | $K_{I/O}$ | $I_{OL}$ = 15 μA | | | 0.4 | V |
| High-level output current | $I_{OH1}$ | REM | $V_{DD}$ = 3.0 V, $V_{OH}$ = 1.0 V | –5 | –9 | | mA |
| | $I_{OH2}$ | $K_{I/O}$ | $V_{DD}$ = 3.0 V, $V_{OH}$ = 2.2 V | –2.5 | –5 | | mA |
| Low-level output current | $I_{OL1}$ | $K_{I/O}$ | $V_{DD}$ = 3.0 V, $V_{OL}$ = 0.4 V | 30 | 70 | | μA |
| | | | $V_{DD}$ = 3.0 V, $V_{OL}$ = 2.2 V | 100 | 220 | | μA |
| Built-in pull-up resistor | $R_1$ | $\overline{RESET}$ | | 25 | 50 | 100 | kΩ |
| Built-in pull-down resistor | $R_2$ | $\overline{RESET}$ | | 2.5 | 5 | 15 | kΩ |
| | $R_3$ | $K_I$, $S_0$, $S_1$ | | 75 | 150 | 300 | kΩ |
| | $R_4$ | $K_{I/O}$ | | 130 | 250 | 500 | kΩ |
| Data hold power supply voltage | $V_{DDOR}$ | In STOP mode | | 1.2 | | 3.6 | V |
| Supply current[Note] | $I_{DD1}$ | Operating mode | $f_X$ = 8 MHz, $V_{DD}$ = 3 V ± 10 % | | 1.4 | 2.8 | mA |
| | | | $f_X$ = 4 MHz, $V_{DD}$ = 3 V ± 10 % | | 1.1 | 2.2 | mA |
| | $I_{DD2}$ | HALT mode | $f_X$ = 8 MHz, $V_{DD}$ = 3 V ± 10 % | | 1.3 | 2.6 | mA |
| | | | $f_X$ = 4 MHz, $V_{DD}$ = 3 V ± 10 % | | 1.0 | 2.0 | mA |
| | $I_{DD3}$ | STOP mode | $V_{DD}$ = 3 V ± 10 % | | 1.0 | 8.0 | μA |
| | | | $V_{DD}$ = 3 V ± 10 %, $T_A$ = 25 °C | | 1.0 | 2.0 | μA |

**Note** The POC circuit current and the current flowing in the built-in pull-up resistor are not included.

**AC Characteristics ($T_A$ = –20 to +70°C, $V_{DD}$ = 2.2 to 3.6 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Instruction execution time | $t_{CY}$ | | | 15.9 | | 27 | μs |
| | | $V_{DD}$ = 2.7 to 3.6 V[Note 1] | | 7.9 | | 27 | μs |
| $K_I$, $S_0$, $S_1$ high-level width | $t_H$ | | | 10 | | | μs |
| | | When canceling Standby mode | HALT mode | 10 | | | μs |
| | | | STOP mode | **Note 2** | | | μs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | μs |

**Notes 1.** When using at $f_X$ = 4 MHz or higher, it is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.7 V.

**2.** 10 + 286/$f_X$ + oscillation growth time

**Remark** $t_{CY}$ = 64/$f_X$ ($f_X$: System clock oscillator frequency)

**POC Circuit[Note 1] ($T_A$ = –20 to +70°C)**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| POC-detected voltage[Note 2] | $V_{POC}$ | | 1.8 | 2.0 | 2.2 | V |
| POC circuit current | $I_{POC}$ | | | 1.2 | 1.5 | μA |

**Notes 1.** Operates effectively under the conditions of $V_{DD}$ = 2.2 to 3.6 V and $f_X$ = 2.4 to 4 MHz.

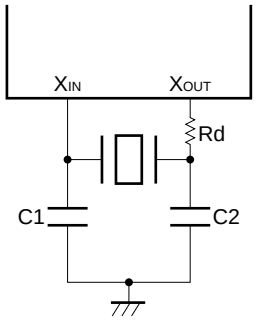
**2.** Refers to the voltage with which the POC circuit cancels an internal reset. If $V_{POC} < V_{DD}$, the internal reset is canceled.
From the time of $V_{POC} \geq V_{DD}$ until the internal reset takes effect, lag of up to 1 ms occurs. When the period of $V_{POC} \geq V_{DD}$ lasts less than 1 ms, the internal reset may not take effect.

**System Clock Oscillation Circuit Characteristics ($T_A$ = –20 to +70°C, $V_{DD}$ = 2.2 to 3.6 V)**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Oscillator frequency | $f_X$ | | 2.4 | 3.64 | 4.0 | MHz |
| (ceramic resonator) | | **Note** | 2.4 | 3.64 | 8.0 | MHz |

**Note** When using at $f_X$ = 4 MHz or higher, it is necessary to design the application circuit so that the $\overline{\text{RESET}}$ pin goes low when the supply voltage is less than 2.7 V.

**An external circuit example**



**PROM Programming Mode**

**DC Programming Characteristics ($T_A$ = 25°C, $V_{DD}$ = 6.0±0.25 V, $V_{PP}$ = 10.0±0.3 V)**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH1}$ | Other than CLK | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | CLK | $V_{DD}$–0.5 | | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL1}$ | Other than CLK | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL2}$ | CLK | 0 | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | | | 10 | μA |
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = –1 mA | $V_{DD}$–1.0 | | | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $V_{DD}$ supply current | $I_{DD}$ | | | | 30 | mA |
| $V_{PP}$ supply current | $I_{PP}$ | MD0 = $V_{IL}$, MD1 = $V_{IH}$ | | | 30 | mA |

**Cautions 1. Keep $V_{PP}$ to within +11 V including overshoot.**

**2. Apply $V_{DD}$ before $V_{PP}$ and turns it off after $V_{PP}$.**

**AC Programming Characteristics ($T_A$ = 25°C, $V_{DD}$ = 6.0±0.25 V, $V_{PP}$ = 10.0±0.3 V)**

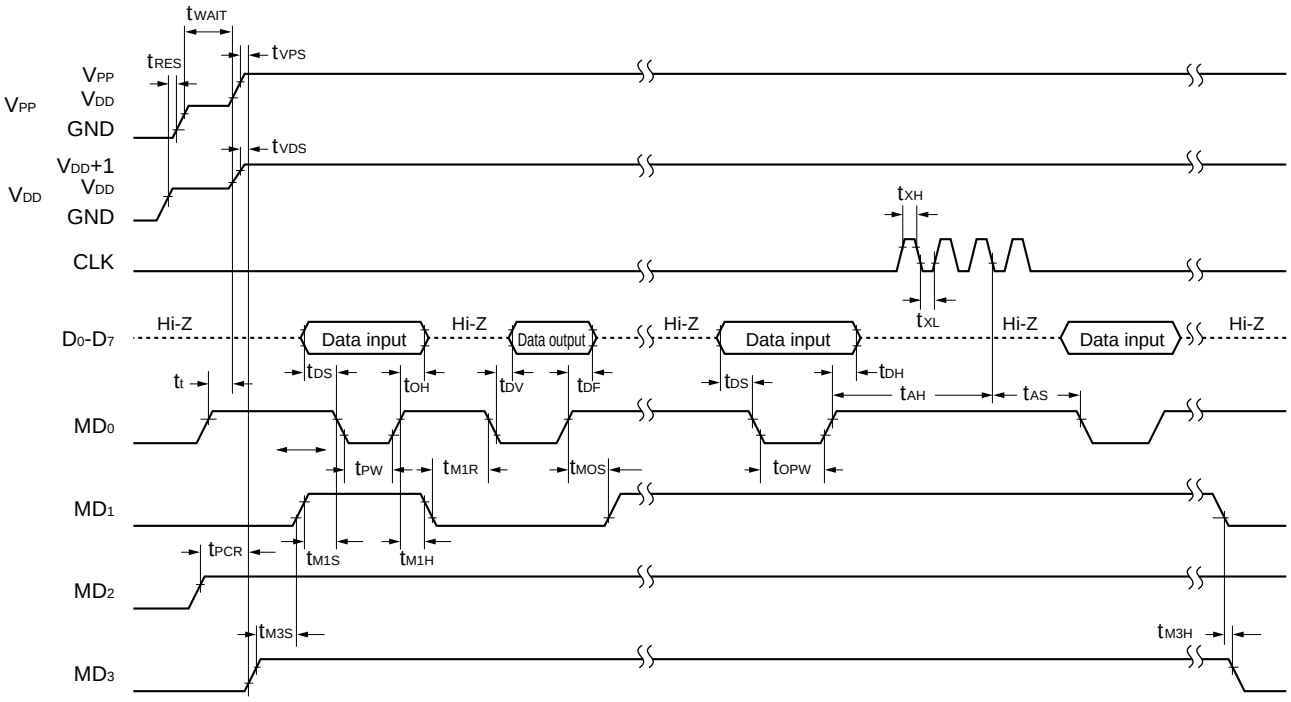
| Parameter | Symbol | **Note1** | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Address setup time[Note 2] (vs. $MD_0$↓) | $t_{AS}$ | $t_{AS}$ | | 2 | | | μs |
| $MD_1$ setup time (vs. $MD_0$↓) | $t_{M1S}$ | $t_{OES}$ | | 2 | | | μs |
| Data setup time (vs. $MD_0$↓) | $t_{DS}$ | $t_{DS}$ | | 2 | | | μs |
| Address hold time[Note 2] (vs. $MD_0$↑) | $t_{AH}$ | $t_{AH}$ | | 2 | | | μs |
| Data hold time (vs. $MD_0$↑) | $t_{DH}$ | $t_{DH}$ | | 2 | | | μs |
| $MD_0$↑→ data output float delay time | $t_{DF}$ | $t_{DF}$ | | 0 | | 130 | ns |
| $V_{PP}$ setup time (vs. $MD_3$↑) | $t_{VPS}$ | $t_{VPS}$ | | 2 | | | μs |
| $V_{DD}$ setup time (vs. $MD_3$↑) | $t_{VDS}$ | $t_{VCS}$ | | 2 | | | μs |
| Initial program pulse width | $t_{PW}$ | $t_{PW}$ | | 0.95 | 1.0 | 1.05 | ms |
| Additional program pulse width | $t_{OPW}$ | $t_{OPW}$ | | 0.95 | | 21.0 | ms |
| $MD_0$ setup time (vs. $MD_1$↑) | $t_{MOS}$ | $t_{CES}$ | | 2 | | | μs |
| $MD_0$↓→ data output delay time | $t_{DV}$ | $t_{DV}$ | MD0 = MD1 = $V_{IL}$ | | | 1 | μs |
| $MD_1$ hold time (vs. $MD_0$↑) | $t_{M1H}$ | $t_{OEH}$ | $t_{M1H}+t_{M1R} \geq 50$ μs | 2 | | | μs |
| $MD_1$ recovery time (vs. $MD_0$↓) | $t_{M1R}$ | $t_{OR}$ | | 2 | | | μs |
| Program counter reset time | $t_{PCR}$ | – | | 10 | | | μs |
| CLK input high-, low-level width | $t_{XH}$, $t_{XL}$ | – | | 0.125 | | | μs |
| CLK input frequency | $f_X$ | – | | | | 8 | MHz |
| Initial mode set time | $t_I$ | – | | 2 | | | μs |
| $MD_3$ setup time (vs. $MD_1$↑) | $t_{M3S}$ | – | | 2 | | | μs |
| $MD_3$ hold time (vs. $MD_1$↓) | $t_{M3H}$ | – | | 2 | | | μs |
| $MD_3$ setup time (vs. $MD_0$↓) | $t_{M3SR}$ | – | When program memory is read | 2 | | | μs |
| Address[Note 2] → data output delay time | $t_{OAD}$ | $t_{ACC}$ | When program memory is read | | | 2 | μs |
| Address[Note 2] → data output hold time | $t_{HAD}$ | $t_{OH}$ | When program memory is read | 0 | | 130 | ns |
| $MD_3$ hold time (vs. $MD_0$↑) | $t_{M3HR}$ | – | When program memory is read | 2 | | | μs |
| $MD_3$↓→ data output float delay time | $t_{DFR}$ | – | When program memory is read | | | 2 | μs |
| Reset setup time | $t_{RES}$ | – | | 10 | | | μs |
| Oscillation stabilization wait time[Note 3] | $t_{WAIT}$ | – | | 2 | | | ms |

**Notes 1.** Equivalent symbol of the corresponding μPD27C256A (The μPD27C256A is a maintenance product.)

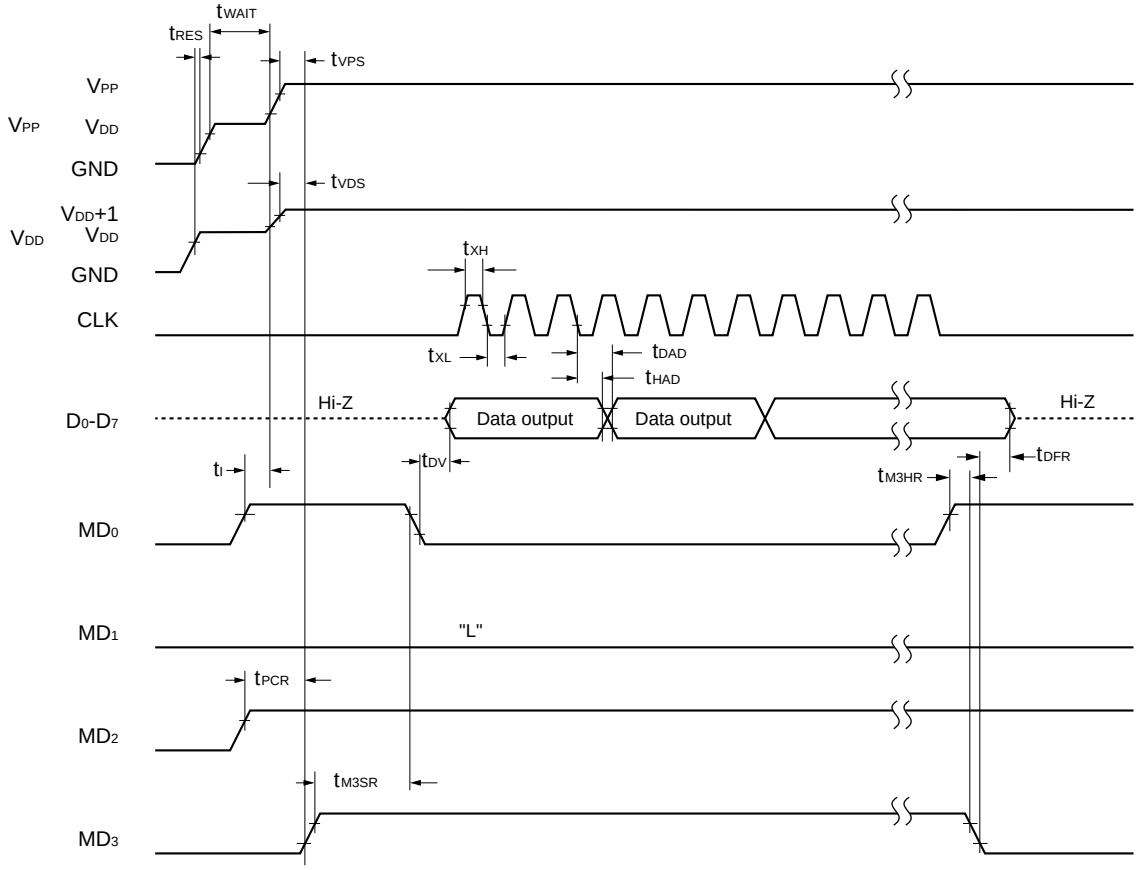
**2.** The internal address signal is incremented at the falling edge of the third clock of CLK.

**3.** Connect a 4 MHz ceramic resonator between the $X_{IN}$ and $X_{OUT}$ pins.

### Program Memory Write Timing

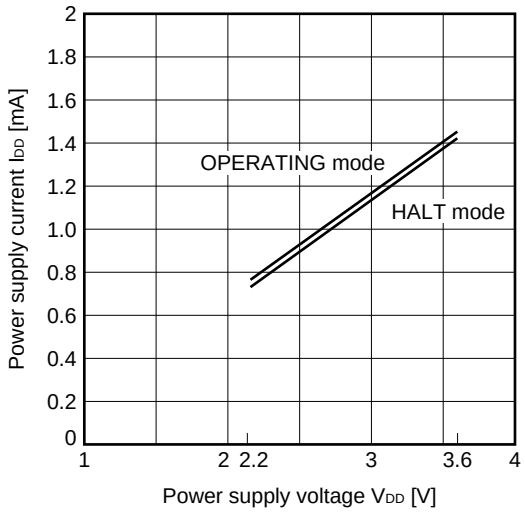



### Program Memory Read Timing

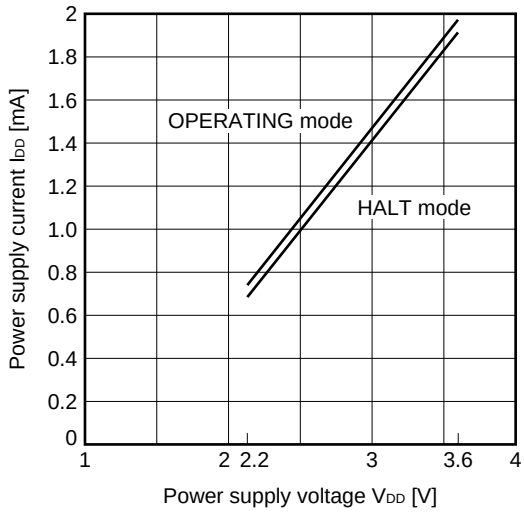


## 5. CHARACTERISTIC CURVE (REFERENCE VALUES)

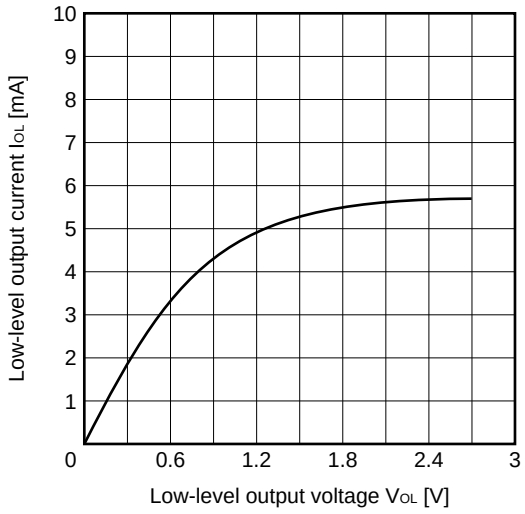
**$I_{DD}$ vs $V_{DD}$ ($f_X$ = 4 MHz)**
**($T_A$ = 25 °C )**



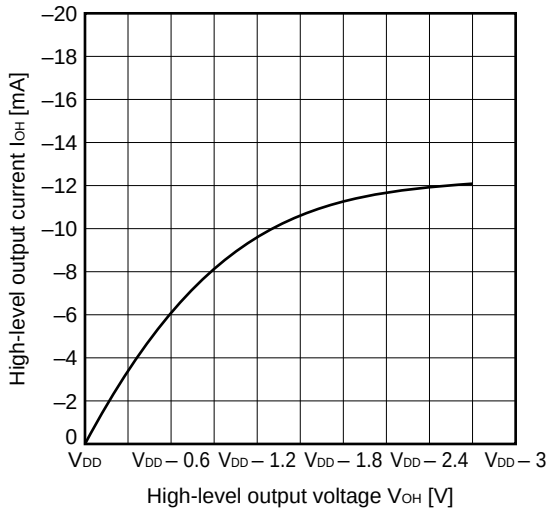

**$I_{DD}$ vs $V_{DD}$ ($f_X$ = 8 MHz)**
**($T_A$ = 25 °C)**



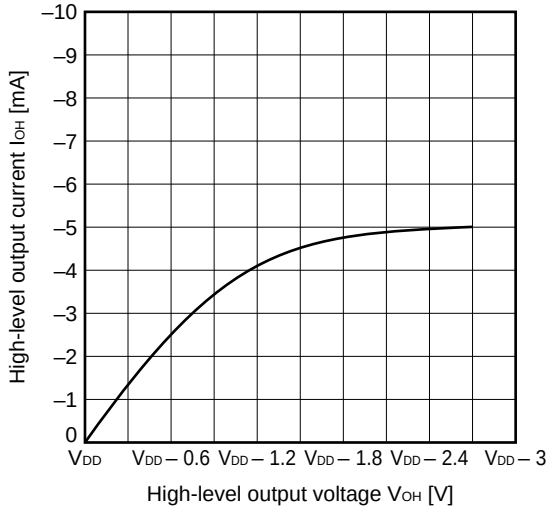

**$I_{OL}$ vs $V_{OL}$ (REM, $\overline{LED}$)**
**($T_A$ = 25 °C, $V_{DD}$ = 3.0 V)**



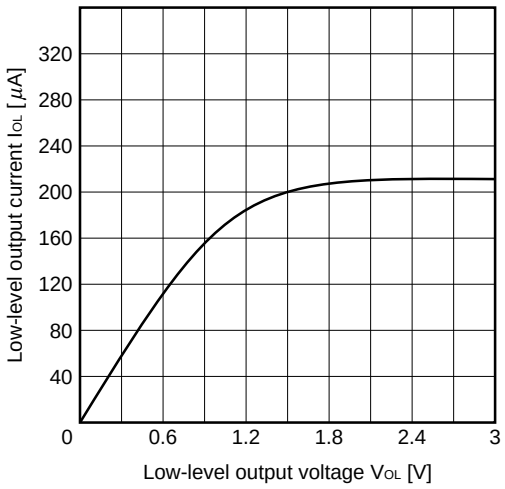

**$I_{OH}$ vs $V_{OH}$ (REM)**
**($T_A$ = 25 °C , $V_{DD}$ = 3.0 V)**



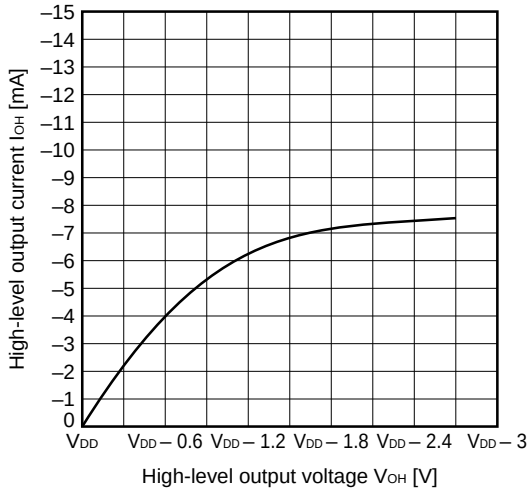

**$I_{OH}$ vs $V_{OH}$ ($\overline{LED}$)**
**($T_A$ = 25 °C , $V_{DD}$ = 3.0 V)**



**$I_{OL}$ vs $V_{OL}$ ($K_{I/O}$)**
**($T_A$ = 25 °C, $V_{DD}$ = 3.0 V)**



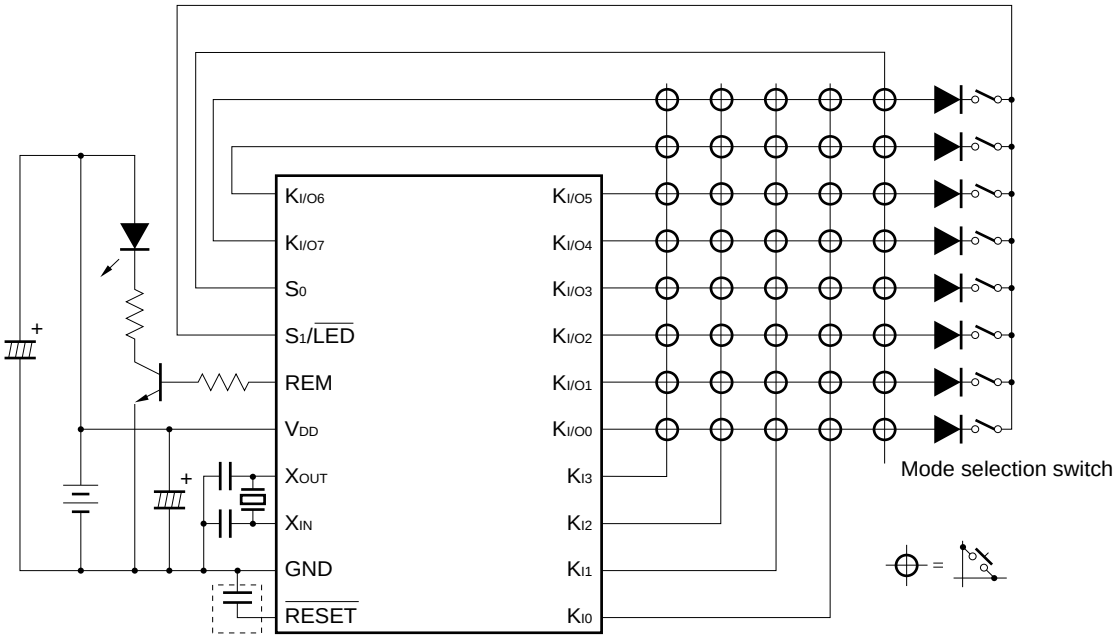

**$I_{OH}$ vs $V_{OH}$ ($K_{I/O}$)**
**($T_A$ = 25 °C, $V_{DD}$ = 3.0 V)**



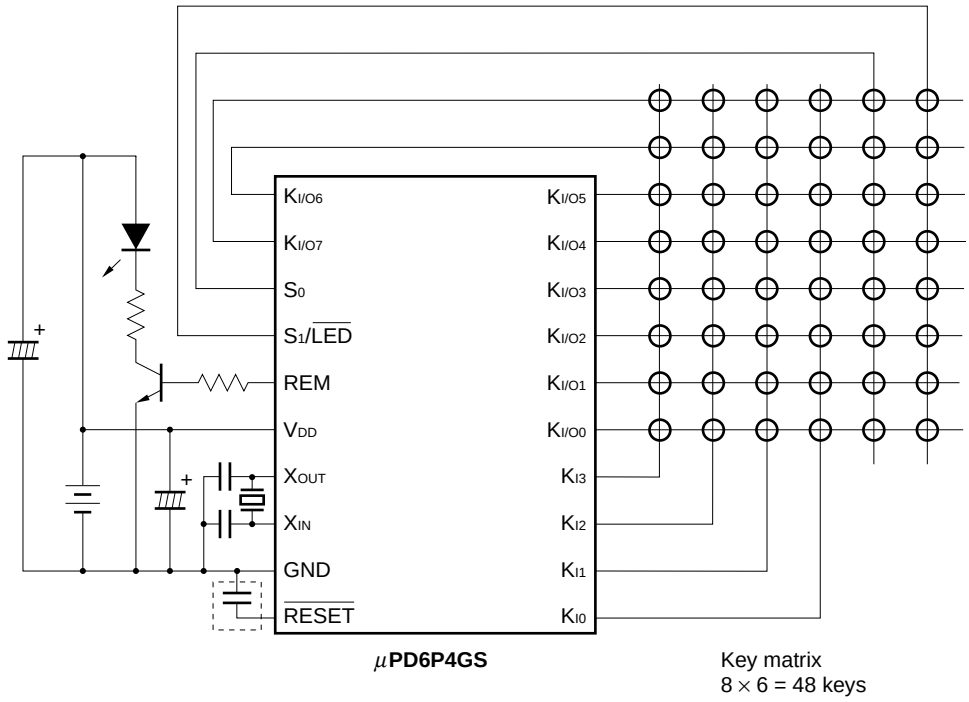
## 6. APPLIED CIRCUIT EXAMPLE

**Example of Application to System**

**· Remote-control transmitter (40 keys; mode selection switch accommodated)**



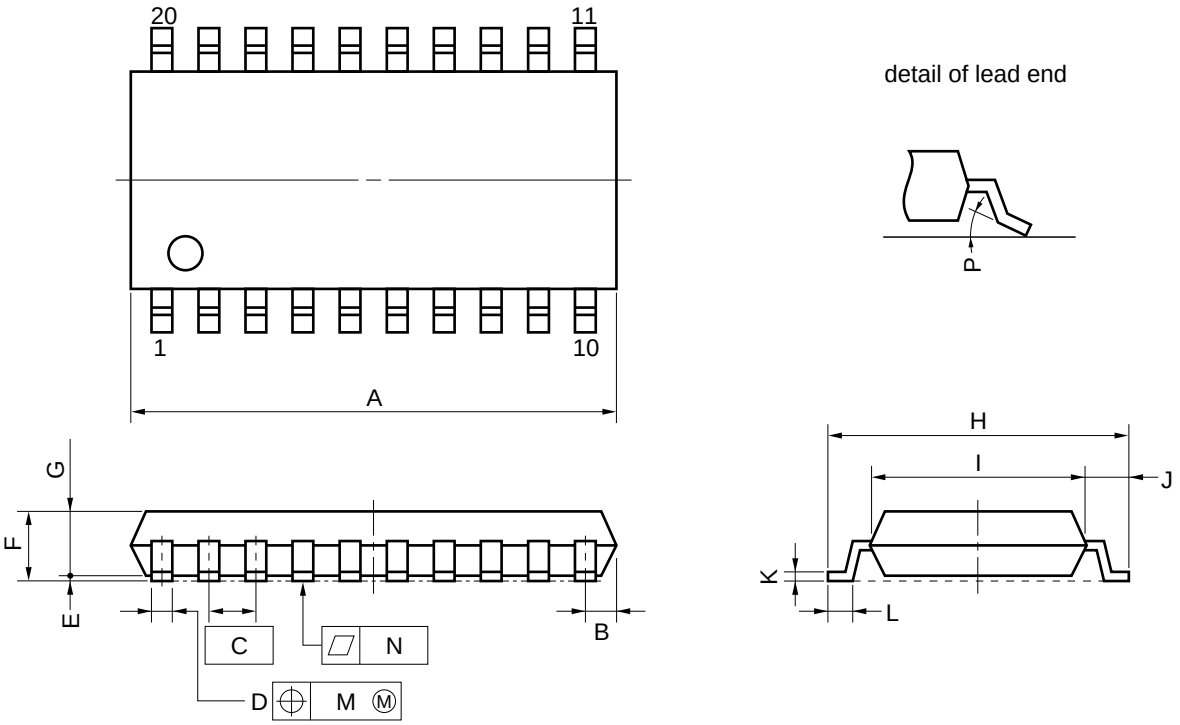

**· Remote-control transmitter (48 keys accommodated)**




**Remark** When the POC circuit is used effectively, it is not necessary to connect the capacitor enclosed in the dotted lines.

## 7. PACKAGE DRAWINGS

## 20 PIN PLASTIC SOP (300 mil)




**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 13.00 MAX. | 0.512 MAX. |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | $0.40^{+0.10}_{-0.05}$ | $0.016^{+0.004}_{-0.003}$ |
| E | 0.1±0.1 | 0.004±0.004 |
| F | 1.8 MAX. | 0.071 MAX. |
| G | 1.55 | 0.061 |
| H | 7.7±0.3 | 0.303±0.012 |
| I | 5.6 | 0.220 |
| J | 1.1 | 0.043 |
| K | $0.20^{+0.10}_{-0.05}$ | $0.008^{+0.004}_{-0.002}$ |
| L | 0.6±0.2 | $0.024^{+0.008}_{-0.009}$ |
| M | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

**P20GM-50-300B, C-4**

## 8. RECOMMENDED SOLDERING CONDITIONS

Carry out the soldered packaging of this product under the following recommended conditions.

For details of the soldering conditions, refer to information material **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than the recommended conditions, please consult one of our NEC sales representatives.

**Table 8-1. Soldering Conditions for Surface-Mount Type**

**μPD6P4GS-×××: 20-pin plastic SOP (300 mil)**

| Soldering Method | Soldering Condition | Recommended Condition Symbol |
|---|---|---|
| Partial heating | Pin temperature: 300 °C or less ; time: 3 secs or less (for each side of the device) | — |

## APPENDIX A. DEVELOPMENT TOOLS

This product uses no hardware in-circuit emulator, etc. Instead, the software simulator is used from designing to development and evaluation.

As a writing tools for the μPD6P4, a PROM programmer and program adapter are provided.

**Hardware**

- **PROM programmer (AF-9704[Note], AF-9705[Note], AF-9706[Note])**
  This PROM programmer supports the μPD6P4.
  By connecting a program adapter to this PROM programmer, the μPD6P4 can be programmed.

**Note** These are products of Ando Electric Co., Ltd. For details, consult Ando Electric Co., Ltd (03-3733-1163).

- **Program adapter (PA-61F34)**
  It is used to program the μPD6P4 in combination with AF-9704, AF-9705, or AF-9706.

## Software

- **Software simulator (SM6133)**
  - Refers to the software development tool of the remote-control transmitter.
  - An assembler (AS6133) is added.

**Caution The assembler alone cannot be purchased.**

**List of SM6133 Ordering Codes**

| Host Machine | OS | | Supply Medium | Ordering Code |
|---|---|---|---|---|
| PC-9800 series (CPU: 80386 and up) | MS-DOS™ | Windows™ | 3.5-inch 2HD | μSAA13SM6133 |
| IBM PC/AT™ and compatible | PC DOS™ | | 3.5-inch 2HC | μSBB13SM6133 |

**Remark** The matching OS versions are as follows.

| OS | Version |
|---|---|
| MS-DOS | Ver. 3.30 to Ver. 5.00 |
| PC DOS | Ver. 3.1 to Ver. 5.0 |
| Windows | Ver. 3.0 to Ver. 3.1 |

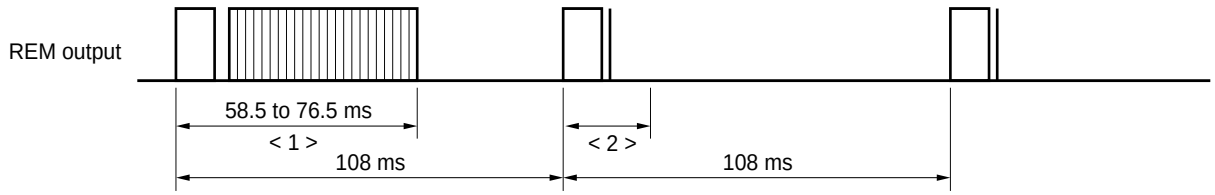
- CPU: 80386 and up (80486DX2 at 66 MHz or high recommended); Windows environment (PC-9800 series; IBM PC/AT)
- Simulation run time: About 500 times of the actual device (when using CPU of 80486 at 16 MHz)
- Key matrix (KEY MAT) function : Capable of applications ranging from single pressing to continuous/multiple pressing, etc. (automatic patch)
  : Direct input possible (serial communications mode available)
- Remote-control waveform data translation function: Translates data values to numeric values “0” and “1”.

  <Example> In the case of the NEC format:
  Header + customer code + data code + STOP bit + frame space
  (P + 5A6C + 18E7 + H500μ + L2000μ)
- WAVE function: Edits and displays the I/O waveform and the key press waveform.
- MEMORY function: Displays all the memory values in real time.
- LISTING function: Capable of Run, Break, Continuous Exec/Step Exec operations.
- Editing function: Can correct and change the program on the simulator.
- TRIGGER function: Break conditions <program counter, memory register, stack level, run time>
  <single, AND, OR, sequential>
- TRACE function: Can trace the program counter, the memory, and the register and measure their times.

## APPENDIX B. EXAMPLE OF REMOTE-CONTROL TRANSMISSION FORMAT (in the case of NEC transmission format in command one-shot transmission mode)

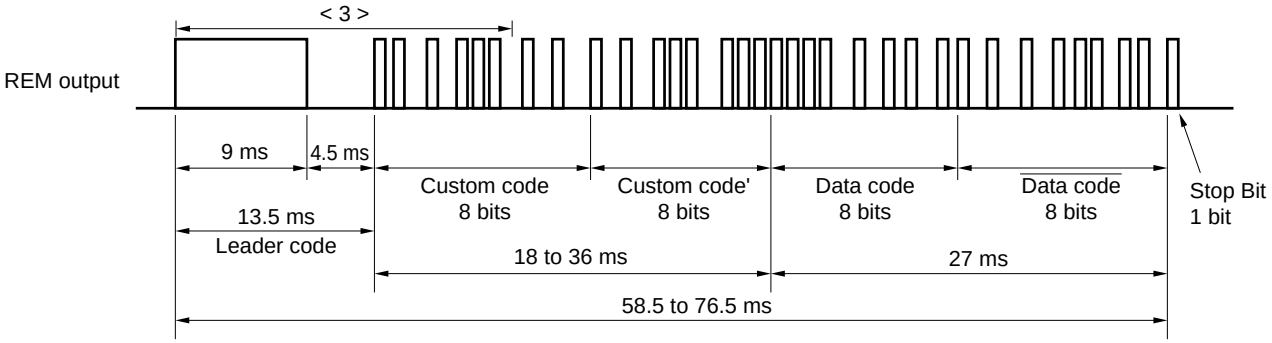
**Caution When using the NEC transmission format, please apply for a custom code at NEC.**

**(1) REM output waveform (From <2> on, the output is made only when the key is kept pressed.)**

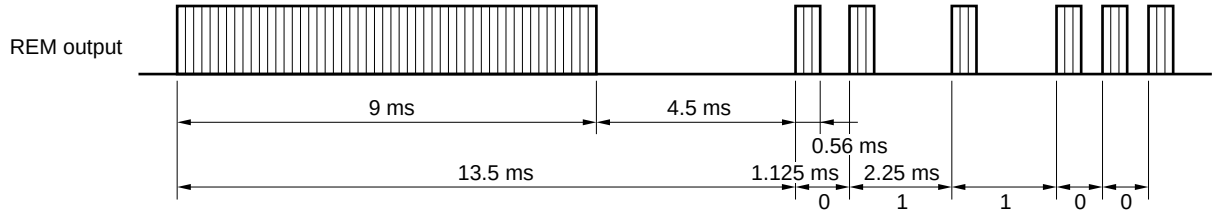



**Remark** If the key is repeatedly pressed, the power consumption of the infrared light-emitting diode (LED) can be reduced by sending the reader code and the stop bit from the second time.

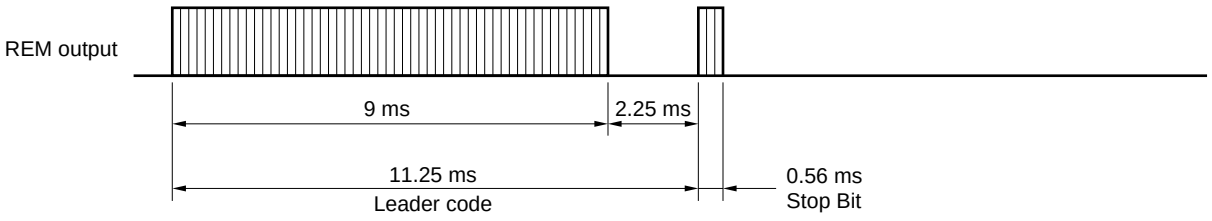
**(2) Enlarged waveform of <1>**



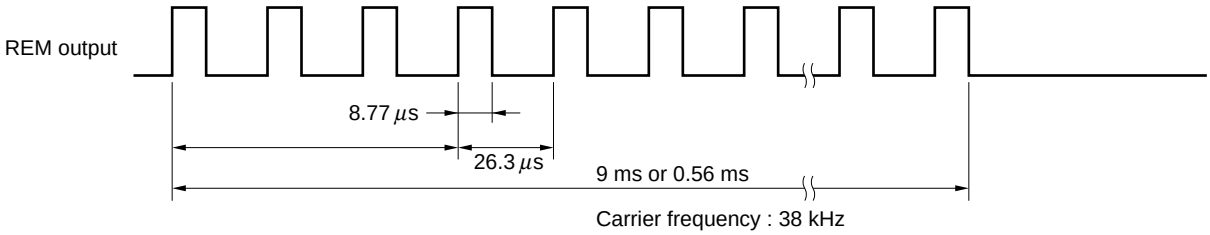

**(3) Enlarged waveform of <3>**



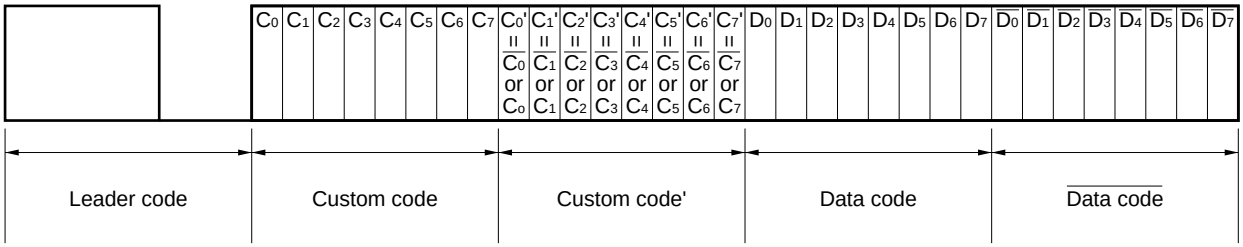

**(4) Enlarged waveform of <2>**



**(5) Carrier waveform (Enlarged waveform of each code's high period)**




**(6) Bit array of each code**




**Caution To prevent malfunction with other systems when receiving data in the NEC transmission format, not only fully decode (make sure to check $\overline{\text{Data Code}}$ as well) the total 32 bits of the 16-bit custom codes (Custom Code, Custom Code') and the 16-bit data codes (Data Code, $\overline{\text{Data Code}}$) but also check to make sure that no signals are present.**

[MEMO]

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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