NEC

MOS INTEGRATED CIRCUIT

μPD753304

4-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD753304 is one of the 75XL series 4-bit single-chip microcontroller chips and has a data processing capability comparable to that of an 8-bit microcontroller.

Since it inherits the 75X series CPU, it has upward compatibility.

While the conventional 75X series products with an on-chip LCD controller/driver use an 80-pin package, the μPD753304 is sold as a pellet/wafer to make it possible to be built into portable devices with an LCD display function, etc.

For detailed function descriptions, refer to the following user's manual.
μPD753304 User's Manual: U12020E

FEATURES

- RC oscillation circuit on chip
- ★ · Main system clock: f_{CC} = 3.6 MHz (typical value with 6.8-kΩ external resistor connected. An internal 10-pF (typ.) capacitor is provided.)
- ★ · Subsystem clock : f_{CT} = 47 kHz (typ.) (Both a resistor and a capacitor are provided internally.)
- Processing can be started immediately after standby mode is released.
- Oscillation of the subsystem clock can be stopped in STOP mode.
- Supply voltage: V_{DD} = 2.5 to 5.5 V
- On-chip memory
  - · Program memory (ROM): 4096 × 8 bits
  - · Data memory (RAM) : 256 × 4 bits
- Variable instruction execution time function useful for power saving
  - · 1.1, 2.2, 4.4, 17.8 μs (in f_{CC} = 3.6 MHz operation)
  - · 85.1 μs (in f_{CT} = 47 kHz operation)
- Programmable LCD controller/driver on chip
- Sold as a pellet/wafer to make it possible to be built into portable devices with an LCD display function

APPLICATION

Small LCD display device, etc.

★ ORDERING INFORMATION

Part Number	Package
μPD753304P-XXX	Pellet
μPD753304W-XXX	Wafer

Caution The μPD753304 is sold as a pellet/wafer. However, an ES product in 42-pin ceramic shrink DIP is also available.

Remark XXX is a ROM code suffix.

★ For the pellet/wafer, consult NEC because an agreement concerning quality must be made.

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The mark ★ shows major revised points.

FUNCTIONAL OUTLINE

	Parameter		Function
★	Instruction execution time		• 1.1, 2.2, 4.4, 17.8 μs (@ 3.6 MHz with main system clock) • 85.1 μs (@ 47 kHz with subsystem clock)
	On-chip memory	ROM	4096 × 8 bits
		RAM	256 × 4 bits
	General-purpose register		• 4-bit operation: 8 × 4 banks • 8-bit operation: 4 × 4 banks
	Input/output port	CMOS input/output	12 — On-chip pull-up resistors which can be specified by software: 4 Also used for segment pins: 4
	LCD controller/driver		• Segment selection: 20/24 segments (can be changed to CMOS input/output port in 4 time-unit; max. 4) • Display mode selection: Static 1/2 duty (1/2 bias) 1/3 duty (1/2 bias) 1/3 duty (1/3 bias) 1/4 duty (1/3 bias)
★			• LCD display modes can be selected by mask option
	Timer		3 channels • 8-bit timer counter: 1 channel (with subclock source input function) • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel
★	Clock output (PCL)		• Φ, 3.6 MHz, 450 kHz, 225 kHz (@ 3.6 MHz with main system clock)
★	Buzzer output (BUZ)		• 2.94, 5.88, 47 kHz (@ 47 kHz with subsystem clock) • 1.76, 3.52, 28.13 kHz (@ 3.6 MHz with main system clock)
	Vectored interrupts		External: 1, Internal: 2
	Test input		Internal: 1
★	System clock oscillation circuit		• Main system clock oscillation RC oscillation circuit (with external resistor and 10 pF (typ.) on-chip capacitor) • Subsystem clock oscillation RC oscillation circuit (with on-chip resistor and capacitor)
	Standby function		STOP mode/HALT mode
	Supply voltage		V_{DD} = 2.5 to 5.5 V
★	Operating ambient temperature		T_A = –10 to +60 °C
★	Package		• Volume production product: Pellet/wafer • ES product (for evaluation): 42-pin ceramic shrink DIP (600 mil)

TABLE OF CONTENTS

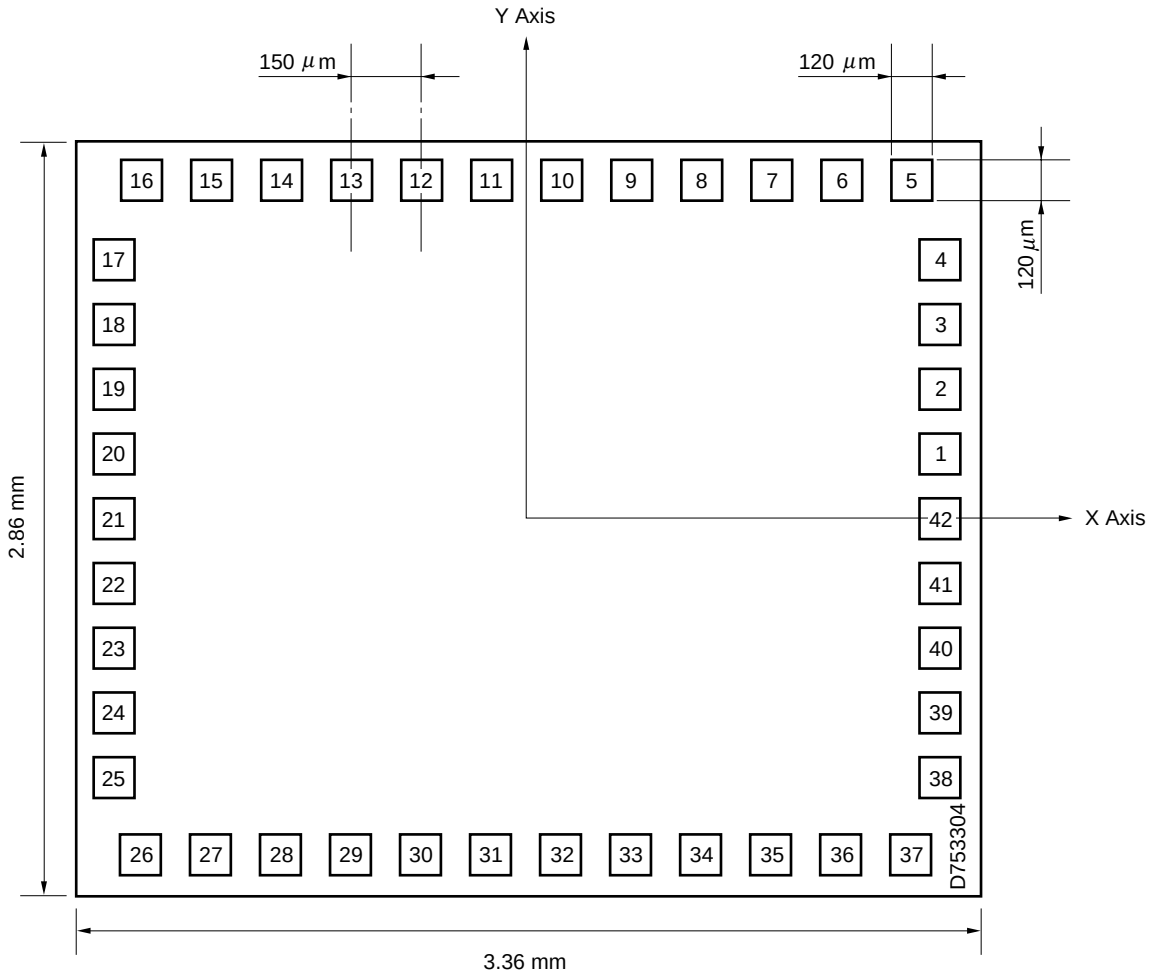
1. PIN CONFIGURATION

★ • **Pin configuration of volume production product (Pad configuration)**

· Pellet

μPD753304P-XXX

Chip size : 3.36 × 2.86 mm²
Pad intervals : 150 μm
Pad size : 120 × 120 μm



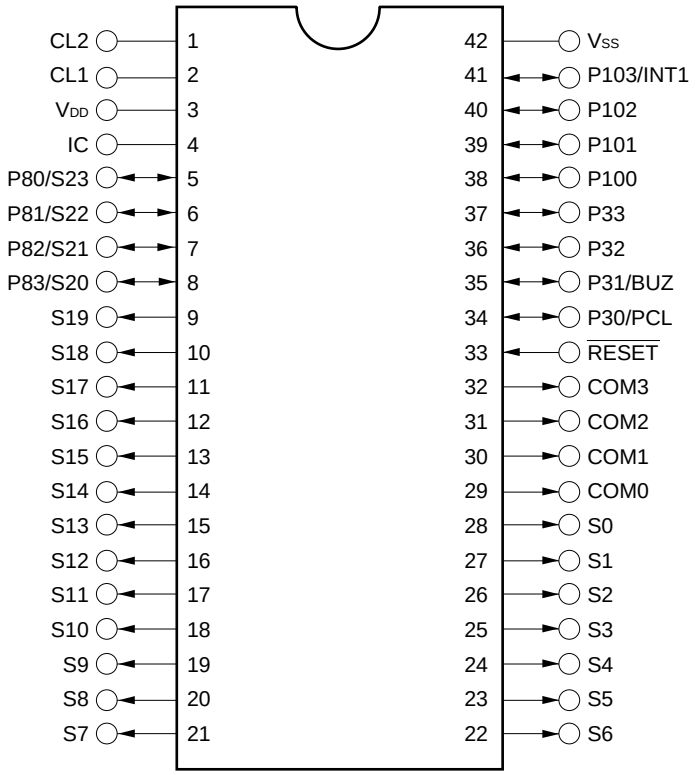
Pad Coordinates (unit: μm: pad center coordinates)

No.	Pin Name	X Axis	Y Axis
1	CL2	1549	311
2	CL1	1549	540
3	V_{DD}	1549	769
4	IC	1549	998
5	P80/S23	1422.5	1299
6	P81/S22	1169.5	1299
7	P82/S21	916.5	1299
8	P83/S20	663.5	1299
9	S19	410.5	1299
10	S18	157.5	1299
11	S17	–216.5	1299
12	S16	–469.5	1299
13	S15	–715.5	1299
14	514	–961.5	1299
15	S13	–1207.5	1299
16	S12	–1453.5	1299
17	S11	–1549	992.5
18	S10	–1549	746.5
19	S9	–1549	500.5
20	S8	–1549	254.5
21	S7	–1549	–105.5

No.	Pin Name	X Axis	Y Axis
22	S6	–1549	–351.5
23	S5	–1549	–597.5
24	S4	–1549	–843.5
25	S3	–1549	–1089.5
26	S2	–1301	–1299
27	S1	–1055	–1299
28	S0	–809	–1299
29	COM0	–563	–1299
30	COM1	–317	–1299
31	COM2	–71	–1299
32	COM3	289	–1299
33	$\overline{\text{RESET}}$	518	–1299
34	P30/PCL	747	–1299
35	P31/BUZ	976	–1299
36	P32	1205	–1209
37	P33	1434	–1299
38	P100	1549	–997
39	P101	1549	–768
40	P102	1549	–539
41	P103/INT1	1549	–310
42	V_{SS}	1549	0.5

Caution Connect the rear side of the pellet to GND.

- **Pin configuration of ES product (Top View)**
  - 42-pin ceramic shrink DIP (600 mil)



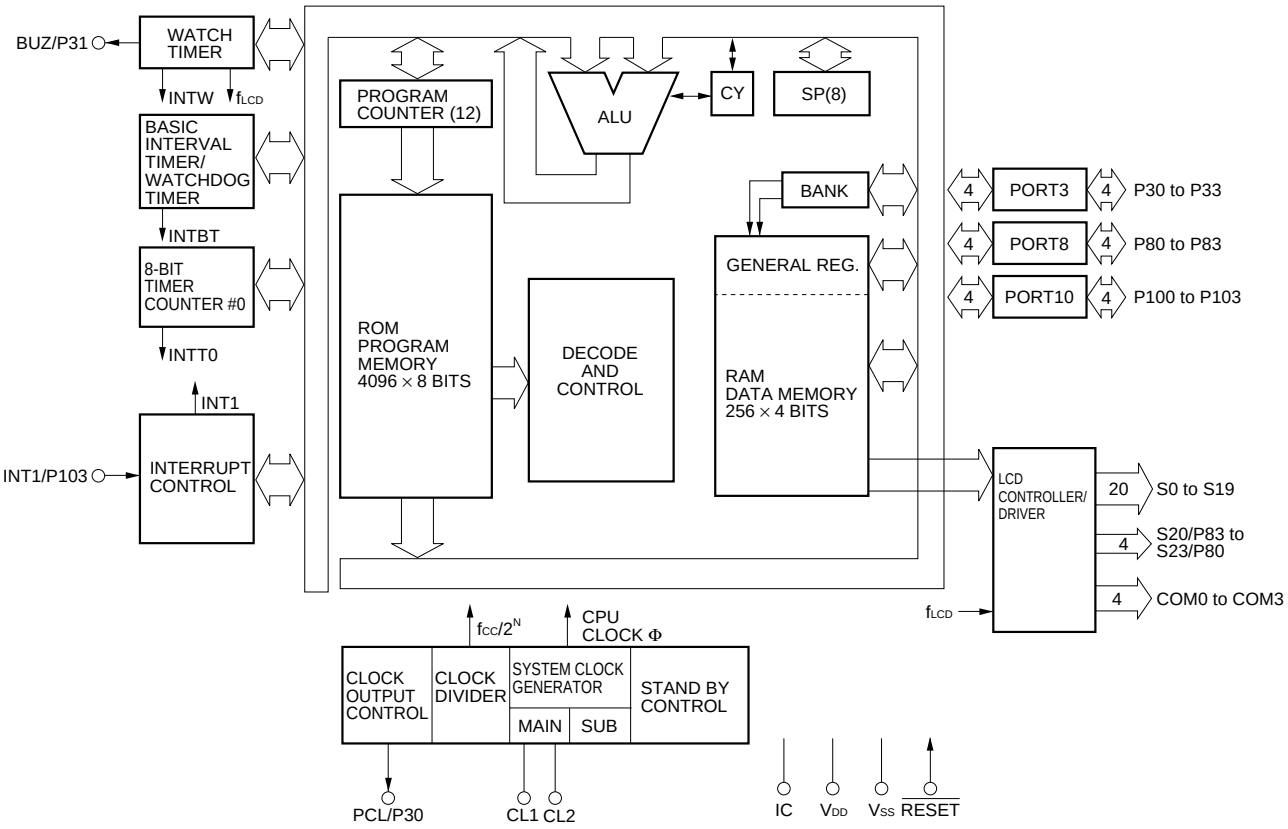
IC: Internally Connected (Connect directly to V_{DD}.)

Caution The μPD753304 is sold as pellet/wafer. The above pin configuration applies to an ES product.

Pin Name

BUZ	:	Buzzer Clock	P100-P103	:	Port10
CL1, CL2	:	RC Oscillator	PCL	:	Programmable Clock
COM0-COM3	:	Common Output0-3	$\overline{\text{RESET}}$	:	Reset
IC	:	Internally Connected	S0-S23	:	Segment Output0-23
INT1	:	External Vectored Interrupt1	V_{DD}	:	Positive Power Supply
P30-P33	:	Port3	V_{SS}	:	Ground
P80-P83	:	Port8			

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

	Pin Name	Input/output	Dual-Function Pin	Function	8-Bit I/O	After Reset	I/O Circuit Type Note 1
★	P30	Input/output	PCL	Programmable 4-bit input/output port (PORT3) Input/output specifiable bit-wise Input/output mode after reset specifiable (mask option) Note 2	X	Input Note 2	E
	P31		BUZ				
	P32		—				
	P33		—				
	P80	Input/output	S23	4-bit input/output port (PORT8)	X	Input	H
	P81		S22				
	P82		S21				
	P83		S20				
★	P100	Input/output	—	Programmable 4-bit input/output port (PORT10) Input/output specifiable bit-wise Connection of on-chip pull-up resistor specifiable in 4-bit units by software	X	Input with pull-up resistor	E-B
	P101		—				
	P102		—				
	P103		INT1				Ⓕ-A

Notes 1. ○ denotes Schmitt trigger input.

★ **2.** Input/output mode after reset can be specified by mask option. For details, refer to **Table 3-1**.

★ **Table 3-1. State after Reset by Mask Option of Port 3**

Pin Names	State after Reset		
	Mask Option <1>	Mask Option <2>	Mask Option <3>
P30/PCL	Input	Low-level output	Low-level output
P31/BUZ			
P32			
P33			High-level output

3.2 Non-Port Pins

Pin Name	Input/output	Dual-Function Pin	Function		After Reset	I/O Circuit Type Note 1
★ PCL	Output	P30	Clock output		Input Note 2	E
BUZ		P31	Arbitrary frequency output (for buzzers or system clock trimming)			
★ INT1	Input	P103	Edge detected vectored interrupt input (detected edge is selectable)	Asynchro-nous	Input with pull-up resistor	Ⓕ-A
★ S0-S19	Output	—	Segment signal output		High-impedance	G-B
S20-S23	Output	P83-P80	Segment signal output		Input	H
★ COM0-COM3	Output	—	Common signal output		High-impedance	G-B
CL1	—	—	Main system clock oscillation resistor (R) connection pin. No external clock can be input.		—	—
CL2	—					
$\overline{\text{RESET}}$	Input	—	System reset input (low level active). On-chip pull-up resistor specifiable (mask option)		—	Ⓑ-A
IC	—	—	Internally connected. Connect directly to V_{DD}.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	Ground potential		—	—

Notes 1. ◯ denotes Schmitt trigger input.

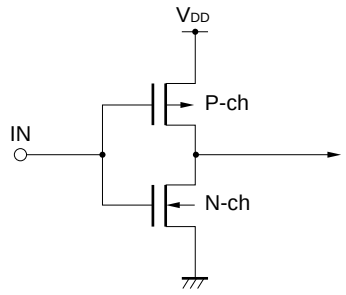
★ **2.** Input/output mode after reset can be specified by mask option. For details, refer to **Table 3-1**.

3.3 Pin Input/Output Circuits

The μPD753304 pin input/output circuits are shown schematically.

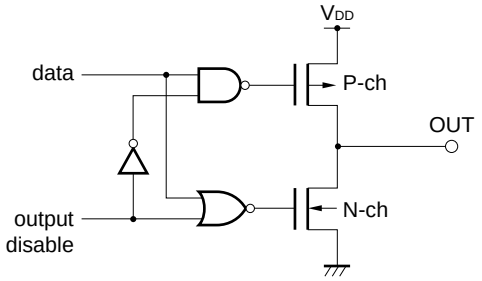
(1/2)

TYPE A



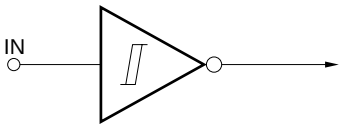
CMOS specification input buffer.

TYPE D



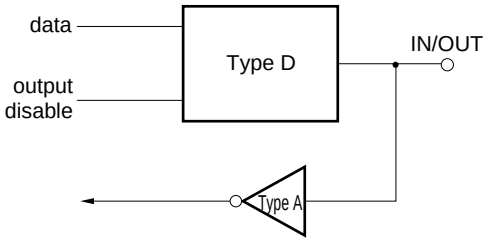
Push-pull output that can be placed in output high-impedance (both P-ch, N-ch off).

TYPE B

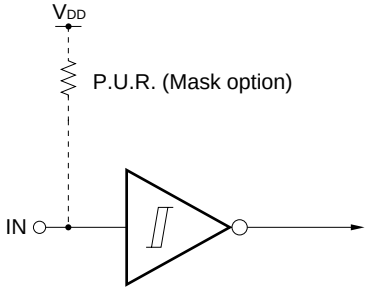


Schmitt triggered input with hysteresis characteristic.

TYPE E



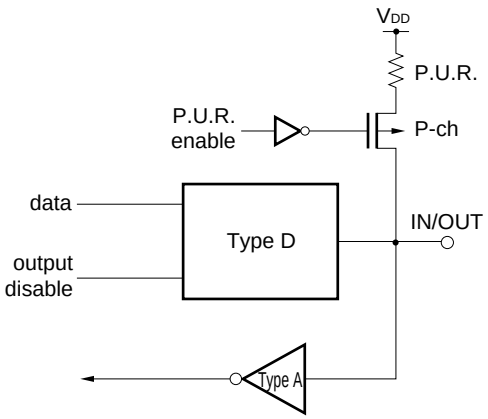
TYPE B-A



P.U.R. : Pull-Up Resistor

Schmitt triggered input with hysteresis characteristic.

TYPE E-B

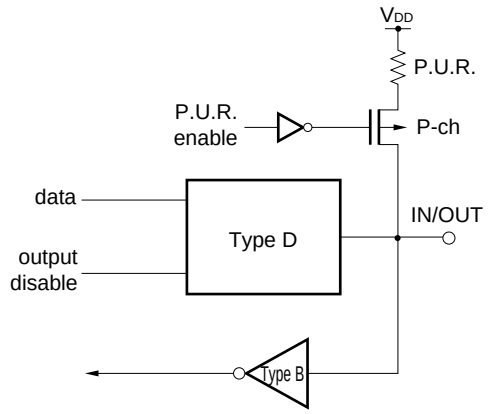


P.U.R. : Pull-Up Resistor

(At $\overline{\text{RESET}}$ active: Enable)

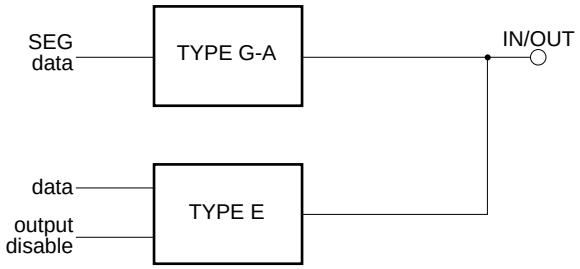
(2/2)

TYPE F-A

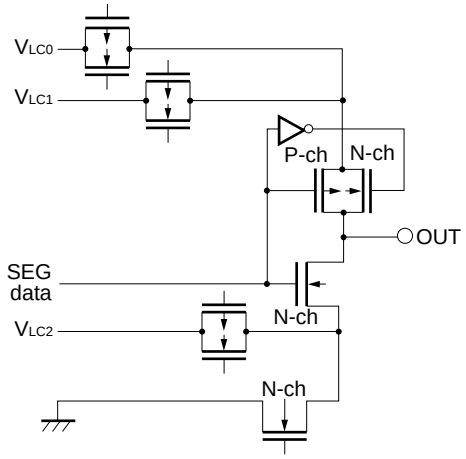


P.U.R. : Pull-Up Resistor

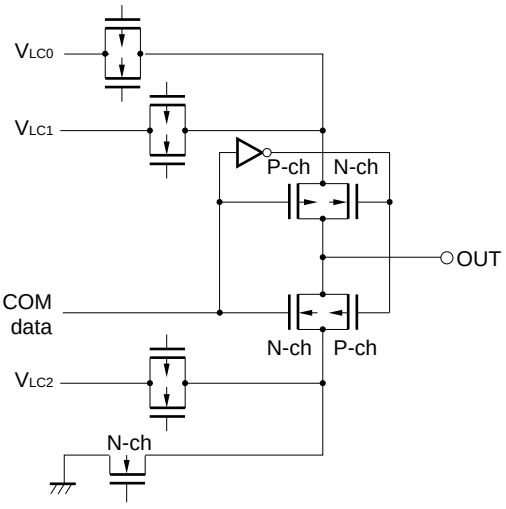
TYPE H



TYPE G-A



TYPE G-B



3.4 Recommended Connections for Unused Pins

Table 3-2. List of Recommended Connections for Unused Pins

Pin	Recommended Connection
P30/PCL	Input state: Connect independently to V_{SS} or V_{DD} via resistor Output state: Leave open
P31/BUZ	
P32	
P33	
P100	
P101	
P102	
P103/INT1	
S0-S19	Leave open
COM0-COM3	
S20/P83-S23/P80	Input state: Connect independently to V_{SS} or V_{DD} via resistor Output state: Leave open
IC	Connect directly to V_{DD}

4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

4.1 Difference between Mk I and Mk II Modes

The CPU of the μPD753304 has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by bit 3 of the Stack Bank Select register (SBS).

- Mk I mode: Can be used in the 75XL CPU with a ROM capacity of up to 16K bytes.
- Mk II mode: Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16K bytes.

Table 4-1. Differences between Mk I Mode and Mk II Mode

	Mk I mode	Mk II mode
Number of stack bytes for subroutine instructions	2 bytes	3 bytes
BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
CALL !addr instruction	3 machine cycles	4 machine cycles
CALLF !faddr instruction	2 machine cycles	3 machine cycles

Caution The Mk II mode supports a program area which exceeds 16K bytes in the 75X and 75XL series. This mode enhances the software compatibility with products which have more than 16K bytes.

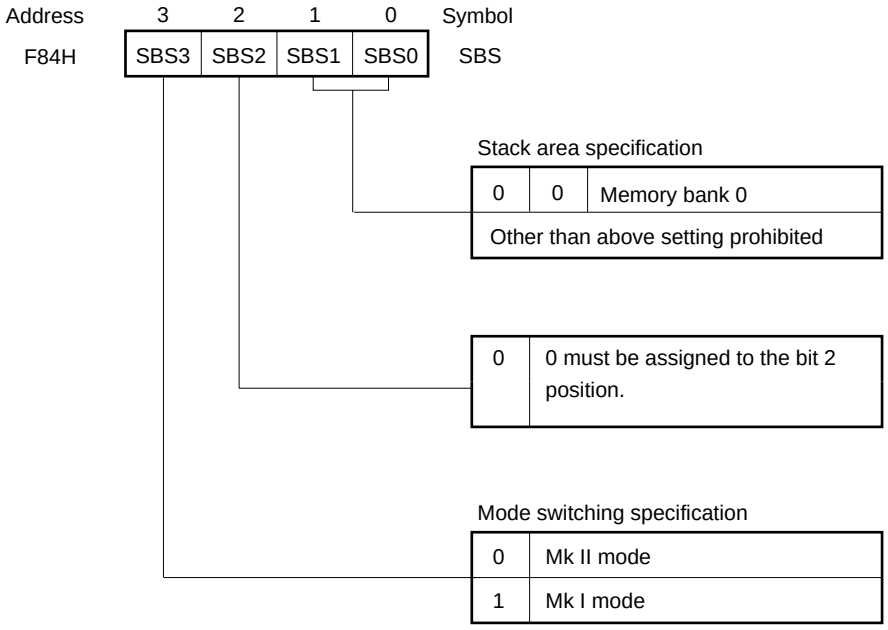
When Mk II mode is selected, the number of stack bytes (usable area) in the execution of a subroutine call instruction increases by 1 per stack compared to Mk I mode. Furthermore, when a CALL !addr, or CALLF !faddr instruction is used, each instruction takes another machine cycle. Therefore, when more importance is attached to RAM utilization or throughput than software compatibility, use the Mk I mode.

4.2 Setting Method of Stack Bank Select Register (SBS)

Switching between the Mk I mode and Mk II mode can be done by the SBS. Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction. When using the Mk I mode, the SBS must be initialized to 1000B at the beginning of a program. When using the Mk II mode, it must be initialized to 0000B.

Figure 4-1. Stack Bank Select Register Format



Caution Since SBS. 3 is set to "1" after a $\overline{\text{RESET}}$ signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to "0" to select the Mk II mode.

5. MEMORY CONFIGURATION

- Program Memory (ROM) .... 4096 × 8 bits
  - Addresses 0000H and 0001H
    Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset and start are possible at an any address.

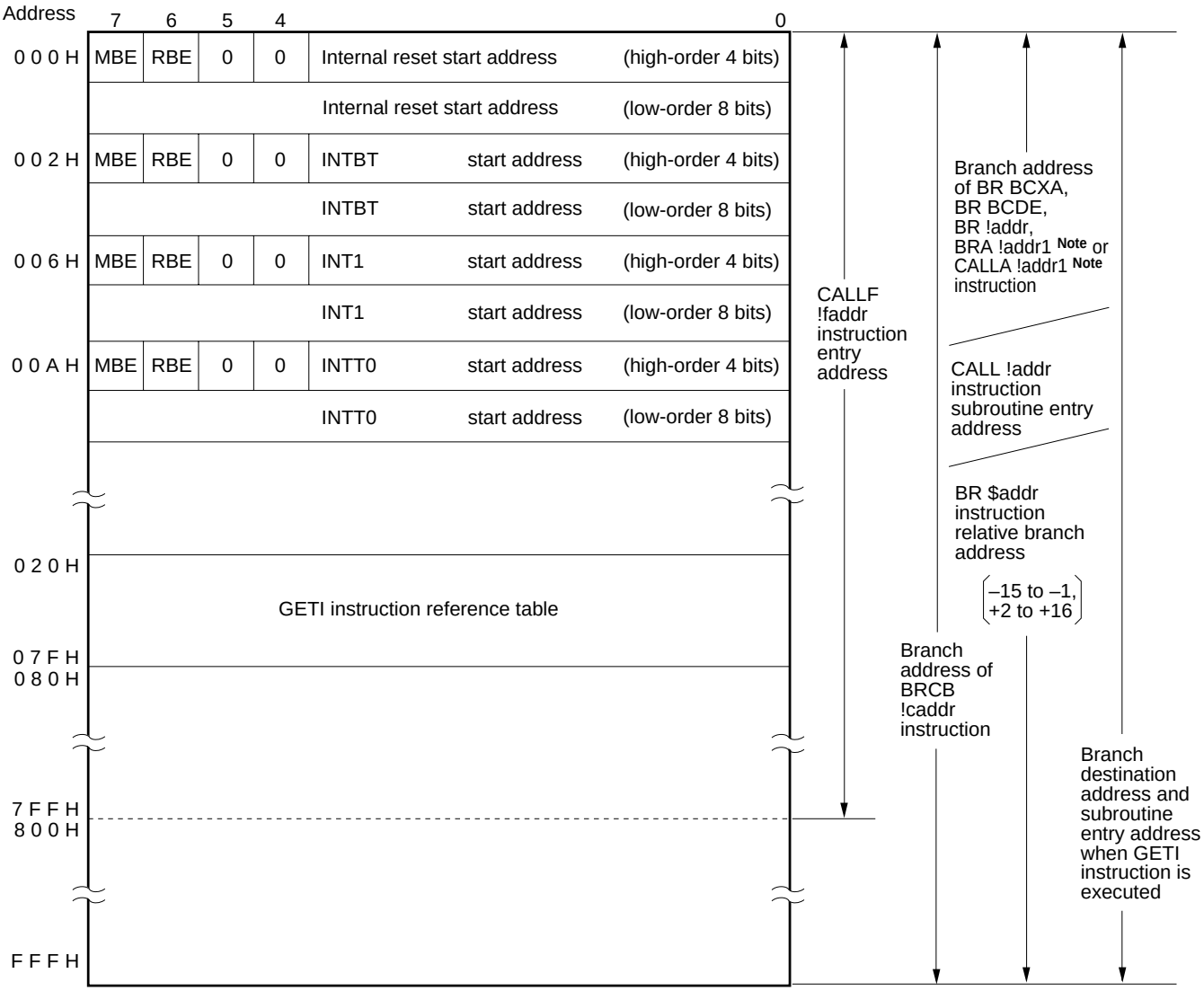
  - Addresses 0002H to 000DH
    Vector table wherein the program start address and values set for the RBE and MBE by the vectored interrupts are written. Interrupt execution can be started at an any address.

  - Addresses 0020H to 007FH
    Table area referenced by the GETI instruction [Note].

    Note The GETI instruction realizes a 1-byte instruction on behalf of an any 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the program steps.

- Data Memory (RAM)
  - Data area ... 256 words × 4 bits (000H to 0FFH)
  - Peripheral hardware area ... 128 words × 4 bits (F80H to FFFH)

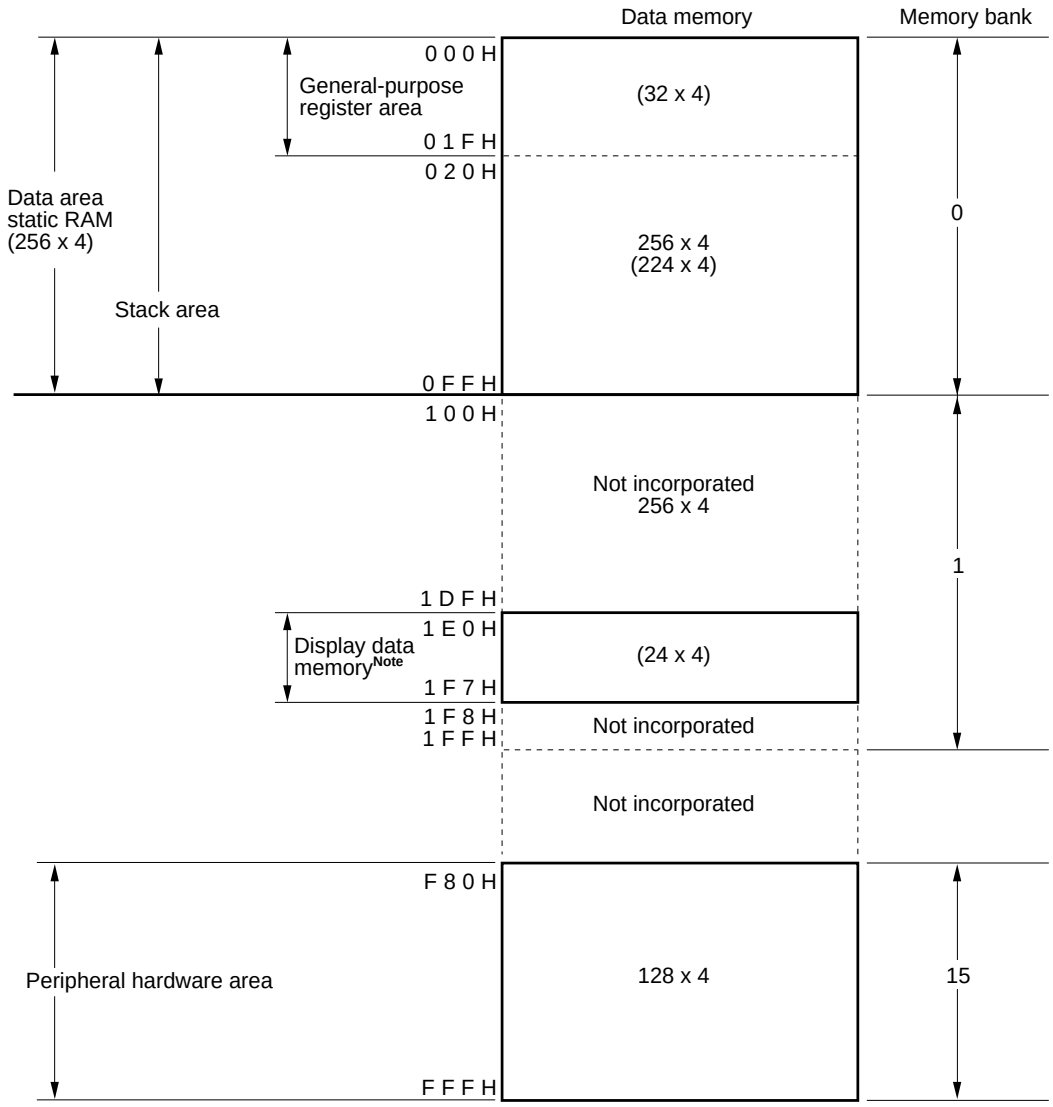
Figure 5-1. Program Memory Map



Note Can be used in Mk II mode only.

Remark In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

Figure 5-2. Data Memory Map



Note Write only.

6. PERIPHERAL HARDWARE FUNCTION

6.1 Digital I/O Port

There are three kinds of I/O port.

- CMOS input/output ports (PORT 3, 8, 10): 12

Table 6-1. Types and Features of Digital Ports

Port	Function	Operation & features	Remarks
PORT3	4-bit I/O	Can be set to input mode or output mode in 1-bit unit.	Also used for the PCL and BUZ pins.
PORT8		Can be set to input mode or output mode in 4-bit units.	Also used for the S20 to S23 pins.
PORT10		Can be set to input mode or output mode in 1-bit unit.	Also used for the INT1 pin.

6.2 Clock Generator

The clock generator is a device that generates the clock fed to peripheral hardware on the CPU and is configured as shown in Figure 6-1.

The clock generator operates according to how the processor clock control register (PCC) and system clock control register (SCC) are set.

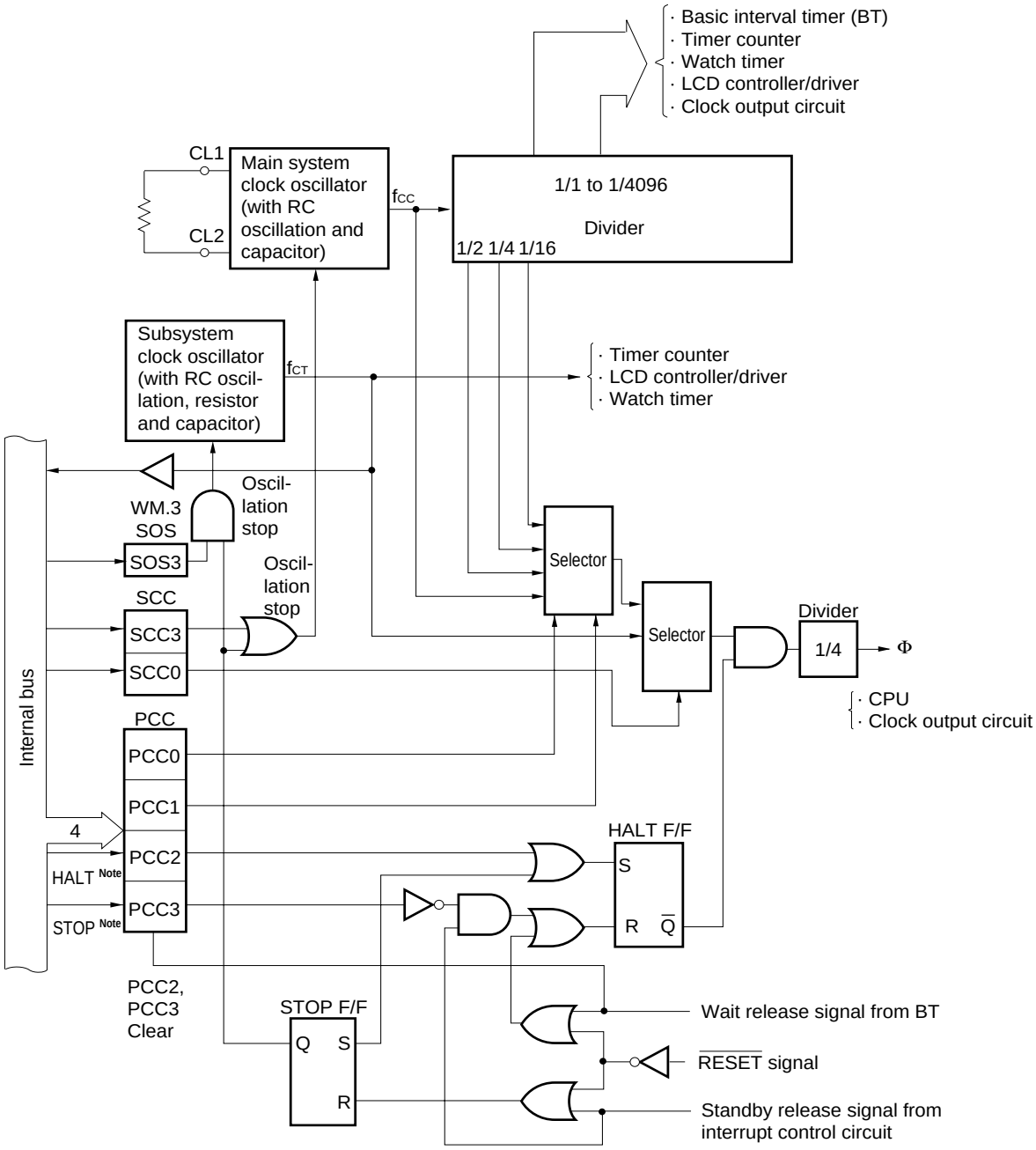
There are two kinds of clocks, main system clock and subsystem clock.

The instruction execution time can also be changed.

★ • 1.1, 2.2, 4.4, 17.8 μs (main system clock: in 3.6-MHz operation)

★ • 85.1 μs (subsystem clock: in 47-kHz operation)

Figure 6-1. Clock Generator Block Diagram



Note Instruction execution

Remarks 1. f_{CC} = Main system clock frequency

2. f_{XT} = Subsystem clock frequency

3. Φ = CPU clock

4. PCC: Processor Clock Control Register

5. SCC: System Clock Control Register

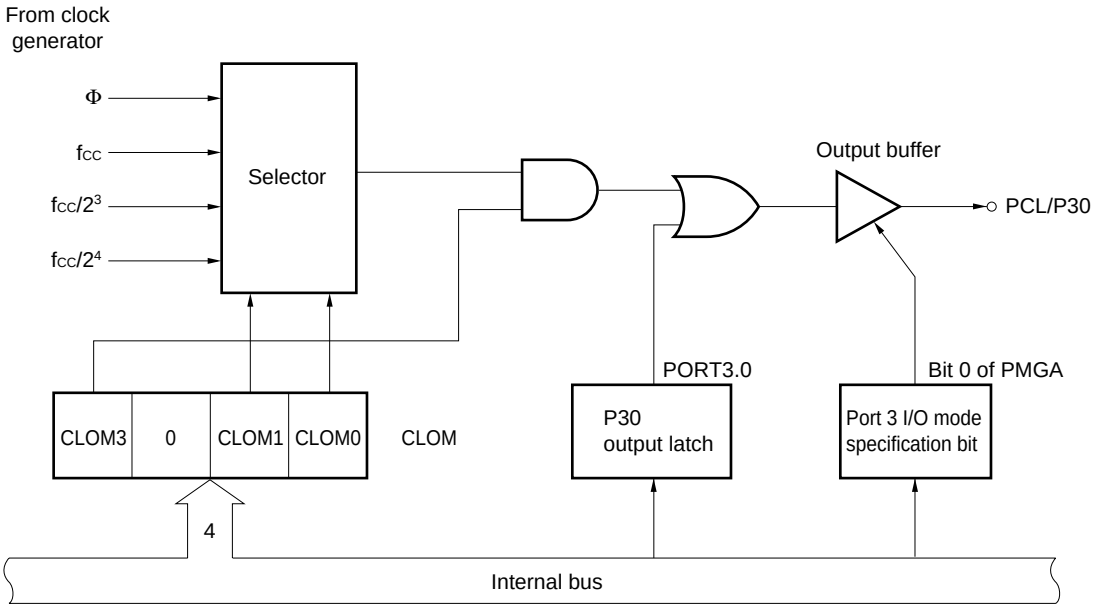
6. One clock cycle (t_{CY}) of the CPU clock is equal to one machine cycle of the instruction.

6.3 Clock Output Circuit

The clock output circuit is provided to output the clock pulses from the PCL/P30 pin to the remote control waveform outputs and peripheral LSI's.

★ • Clock Output (PCL): Φ, 3.6 MHz, 450 kHz, 225 kHz (in 3.6-MHz operation)

Figure 6-2. Clock Output Circuit Block Diagram



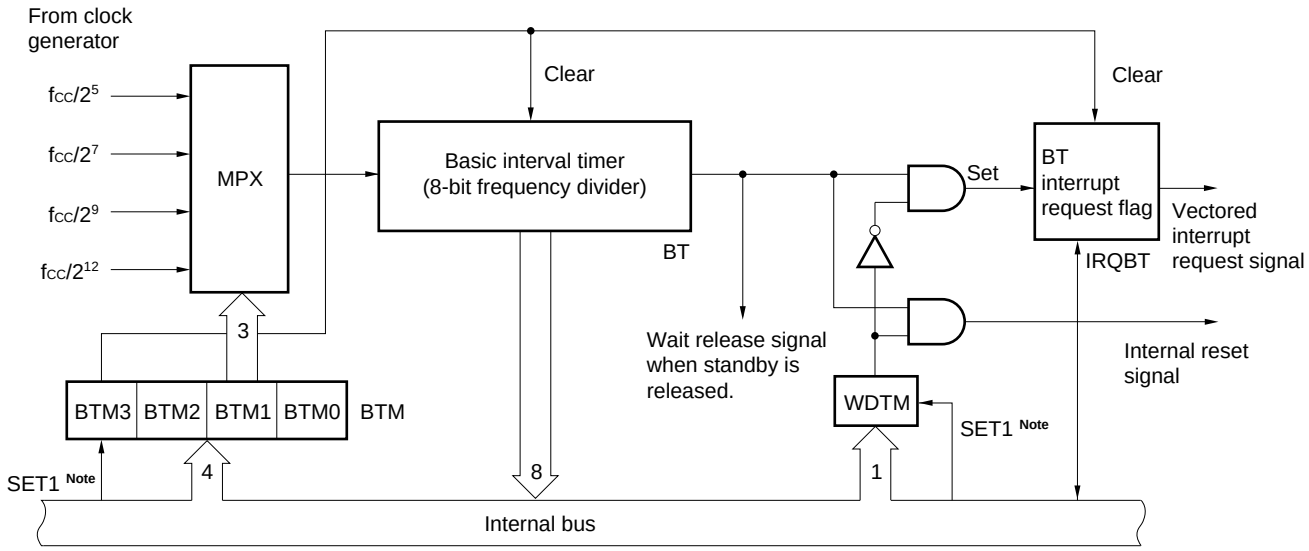
Remark Special care has been taken in designing the chip so that small-width pulses may not be output when switching clock output enable/disable.

6.4 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- Interval timer operation to generate a reference time interrupt
- Watchdog timer operation to detect an inadvertent program loop and reset the CPU
- Reads the contents of counting

Figure 6-3. Basic Interval Timer/Watchdog Timer Block Diagram



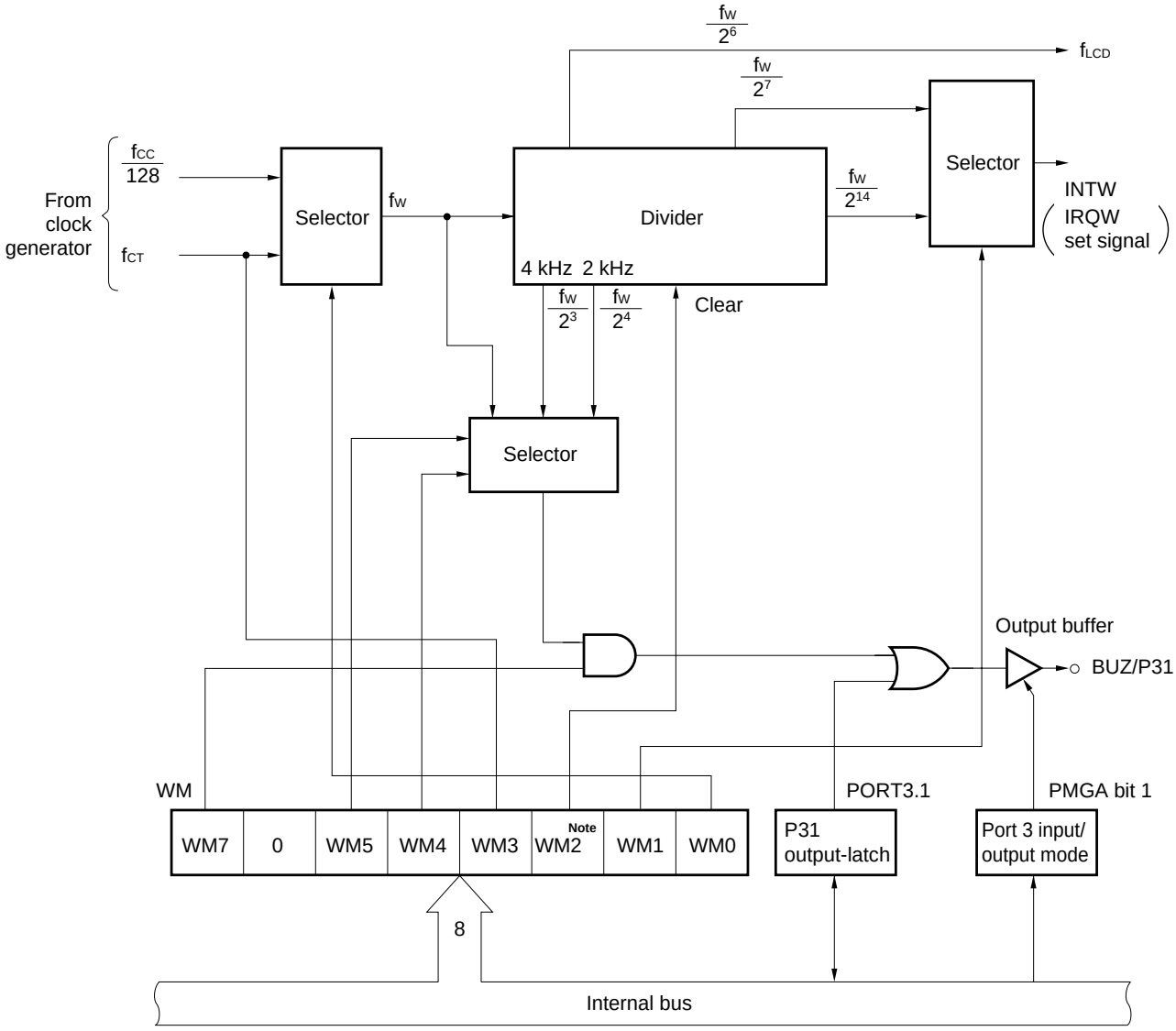
Note Instruction execution

6.5 Watch Timer

The μPD753304 has one watch timer channel which has the following functions.

- Sets the test flag (IRQW) at $f_W/2^{14}$ intervals. The standby mode can be released by the IRQW.
- Convenient for program debugging and checking as interval becomes 128 times longer ($f_W/2^7$) with the fast feed mode.
- Outputs the frequencies (f_W, $f_W/2^3$, $f_W/2^4$) to the BUZ/P31 pin, usable for buzzer and trimming of system clock frequencies.
- Clears the frequency divider to make the watch start with zero seconds.

Figure 6-4. Watch Timer Block Diagram



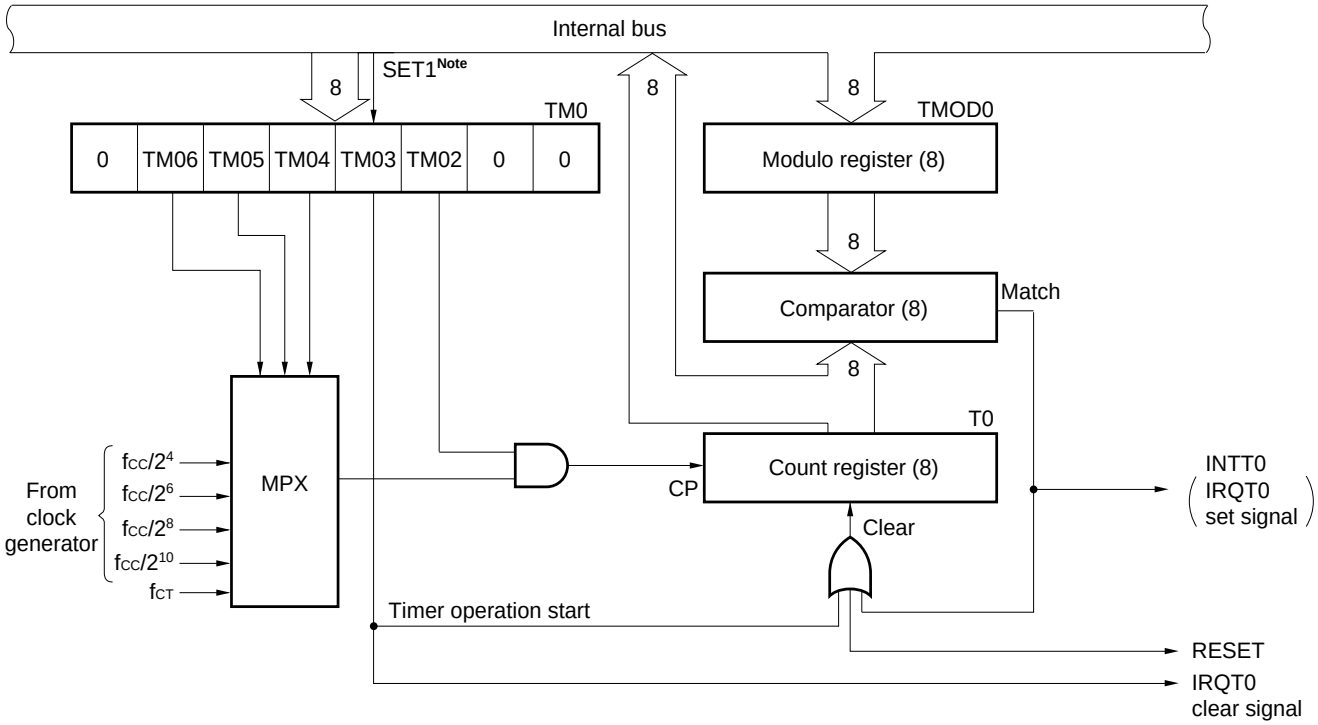
Note Set WM2 to 1 when using the LCD controller/driver.

6.6 Timer Counter

The μPD753304 has one channel of timer counter. Its configuration is shown in Figure 6-5. The timer counter has the following functions.

- Programmable interval timer operation
- Read the count value.

Figure 6-5. Timer Counter Block Diagram



Note Instruction execution

Caution When setting data to the TM0, be sure to set bits 0, 1, 7 to 0.

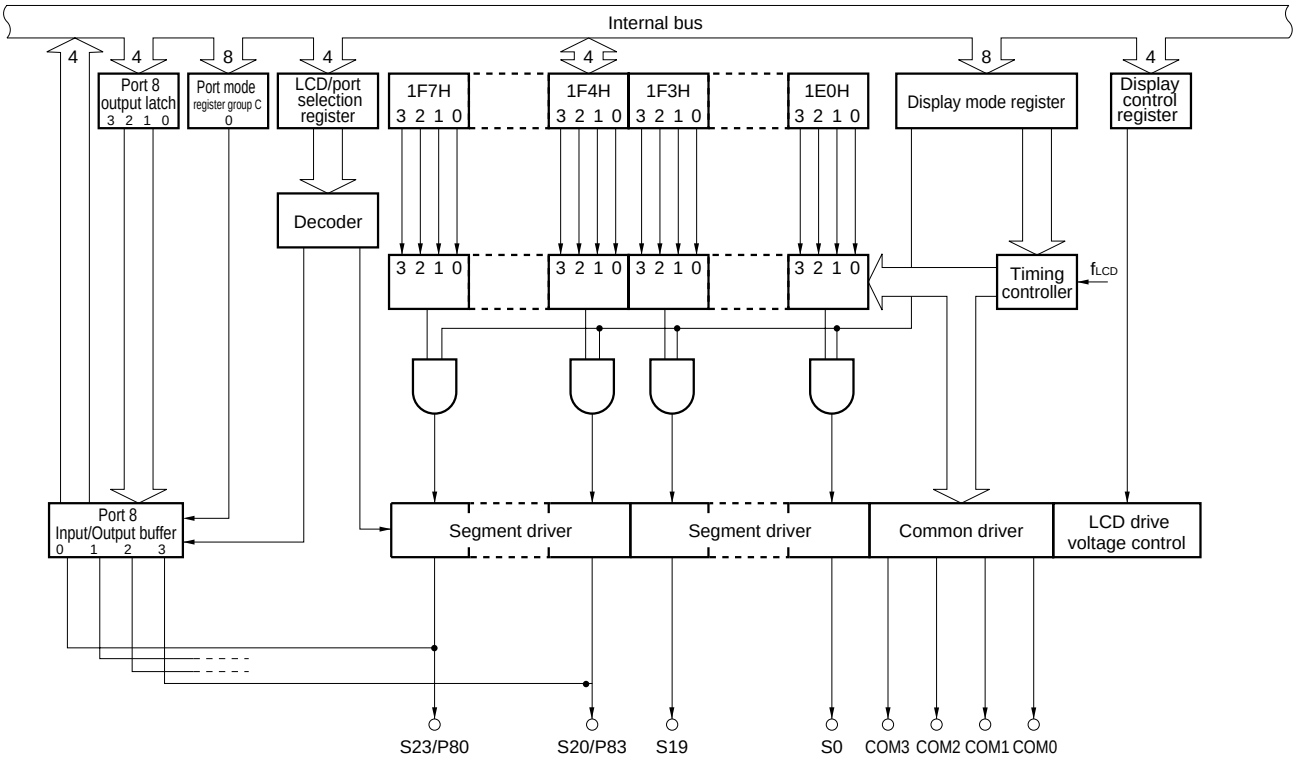
6.7 LCD Controller/Driver

The μPD753304 incorporates a display controller which generates segment and common signals according to the display data memory contents and incorporates segment and common drivers which can drive the LCD panel directly.

The μPD753304 LCD controller/driver has the following functions:

- Display data memory is read automatically by DMA operation and segment and common signals are generated.
- Display mode can be selected from among the following five:
  - <1> Static
  - <2> 1/2 duty (time multiplexing by 2), 1/2 bias
  - <3> 1/3 duty (time multiplexing by 3), 1/2 bias
  - <4> 1/3 duty (time multiplexing by 3), 1/3 bias
  - <5> 1/4 duty (time multiplexing by 4), 1/3 bias
- A frame frequency can be selected from among four in each display mode.
- A maximum of 24 segment signal output pins (S0 to S23) and four common signal output pins (COM0 to COM3).
- The segment signal output pins (S20 to S23) can be changed to the I/O ports (PORT8).
- LCD display modes can be selected (mask option).
- It can also operate by using the subsystem clock.

Figure 6-6. LCD Controller/Driver Block Diagram



7. INTERRUPT FUNCTION AND TEST FUNCTION

The μPD753304 has three different interrupt sources and one types of test source.
The interrupt control circuit of the μPD753304 has the following functions.

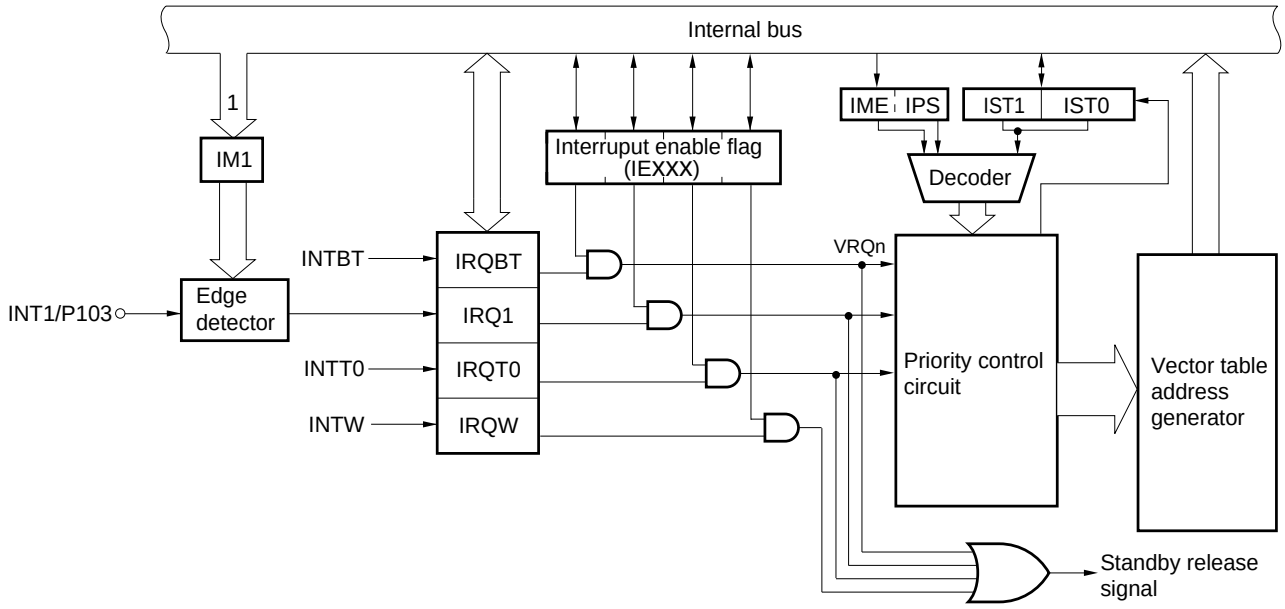
(1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acceptance by the interrupt enable flag (IExxx) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQxxx). An interrupt generation can be checked by software.
- Release the standby mode. An interrupt to be released can be selected by the interrupt enable flag.

(2) Test function

- Test request flag (IRQxxx) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

Figure 7-1. Interrupt Control Circuit Block Diagram



8. STANDBY FUNCTION

In order to reduce power dissipation while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD753304.

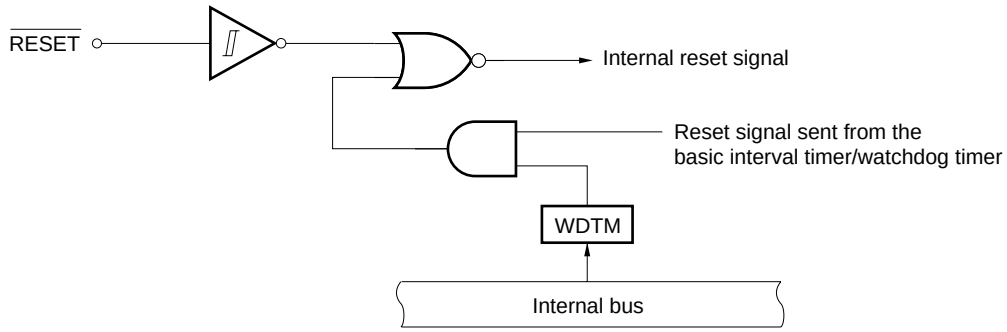
Table 8-1. Operation Status in Standby Mode

Item \ Mode		STOP mode	HALT mode
Set instruction		STOP instruction	HALT instruction
System clock for setting		Can be set by either main system clock or subsystem clock.	
Operating status	Clock generator	Oscillation of main system clock is stopped. Setting the sub oscillation circuit stop enable flag (SOS.3) to 1 also stops oscillation of the subsystem clock.	Only CPU clock Φ is stopped (oscillation continues.)
	Basic interval timer/ watchdog timer	Operation stopped	Operates only when main system clock is oscillating BT mode : Sets IRQBT at reference time intervals WT mode: Generates reset signal when BT overflows
	Timer counter	Operation possible only when SOS.3 is set to 0 and f_{CT} is selected as count clock.	Operation impossible only when a divided main system clock is selected as count clock when the main system clock is stopped.
	LCD control/driver	Operation possible only when SOS.3 is set to 0 and f_{CT} is selected as LCDCL.	Operation possible
	Watch timer	Operation possible only when SOS.3 is set to 0 and f_{CT} is selected as count clock.	Operation possible
	External interrupt	Operation possible only when SOS.3 is set to 0.	
	CPU	Operation stopped	
Release signal		Generation of an interrupt request signal from hardware whose operation is enabled by an interrupt enable flag or $\overline{\text{RESET}}$ signal.	

9. RESET FUNCTION

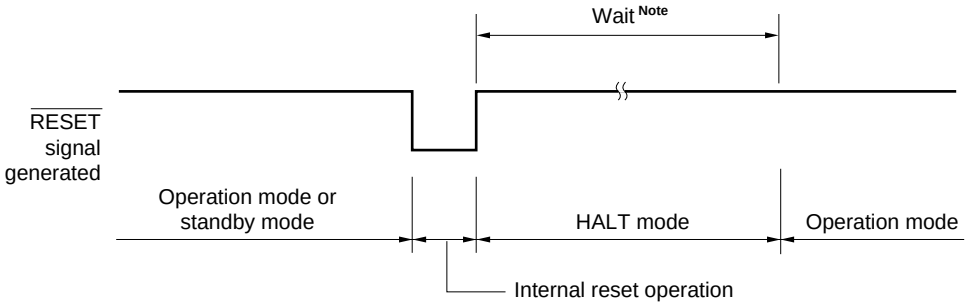
There are two reset inputs: external $\overline{\text{RESET}}$ signal and reset signal sent from the basic interval timer/watchdog timer. When either one of the reset signals are input, an internal reset signal is generated. Figure 9-1 shows the circuit diagram of the above two inputs.

Figure 9-1. Configuration of Reset Function



Generation of the $\overline{\text{RESET}}$ signal initializes each device as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

Figure 9-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation



★ **Note** 56/fcc (15.6 μs: @ 3.6-MHz operation)

Table 9-1. Status of Each Device After Reset (1/2)

Hardware		$\overline{\text{RESET}}$ signal generation in the standby mode	$\overline{\text{RESET}}$ signal generation in operation
Program counter (PC)		Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.	Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0)	0	0
	Bank enable flag (MBE, RBE)	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.
Stack pointer (SP)		Undefined	Undefined
Stack bank select register (SBS)		1000B	1000B
Data memory (RAM)		Held	Undefined
General-purpose register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank select register (MBS, RBS)		0, 0	0, 0
Basic interval timer/watchdog timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
	Watchdog timer enable flag (WDTM)	0	0
Timer counter (T0)	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0

Table 9-1. Status of Each Device After Reset (2/2)

Hardware		$\overline{\text{RESET}}$ signal generation in the standby mode	$\overline{\text{RESET}}$ signal generation in operation
Watch timer	Mode register (WM)	0	0
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Subsystem clock oscillator control register (SOS)		0	0
LCD controller/ driver	Display mode register (LCDM)	0	0
	Display control register (LCDC)	0	0
	LCD/port selection register (LPS)	0	0
Interrupt function	Interrupt request flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt enable flag (IExxx)	0	0
	Interrupt priority select register (IPS)	0	0
	INT1 mode registers (IM1)	0	0
Digital port	Output buffer (P30-P33)	On	On
	Output buffer (P80-P83, P100-P103)	Off	Off
	Output latch (P30-P32, P80-P83, P100-P103)	Cleared (0)	Cleared (0)
	Output latch (P33)	Set (1)	Set (1)
	I/O mode registers (PMGA)	0FH	0FH
	I/O mode registers (PMGC, D)	00H	00H
	Pull-up resistor setting register (POGB)	01H	01H

10. MASK OPTION

The μPD753304 has the following mask options.

- $\overline{\text{RESET}}$ pin mask option
  An on-chip pull-up resistor can be selected.
  <1> Specifies an on-chip pull-up resistor.
  <2> Specifies no on-chip pull-up resistor.

★ • LCD display mode mask option
  LCD display modes can be selected.
  <1> Static display mode (BIAS-V_{LC0} shorted, V_{LC0} – V_{LC1} opened)
  <2> 1/2 bias mode (BIAS-V_{LC0} shorted, V_{LC1} – V_{LC2} shorted)
  <3> 1/3 bias mode (BIAS-V_{LC0} shorted)

- Standby function mask option
  Wait time can be selected after STOP mode is released.
  <1> 512/f_{CC} (142 μs: in 3.6 MHz operation)
  <2> No waits

★ • Port 3 mask option
  Input/output mode after reset can be specified

Pin Names	Status after Reset		
	Mask Option <1>	Mask Option <2>	Mask Option <3>
P30/PCL	Input	Low-level output	Low-level output
P31/BUZ			
P32			
P33			High-level output

11. INSTRUCTION SET

(1) Expression formats and description methods of operands

The operand is written in the operand column of each instruction in accordance with the method of use of the instruction operand identifier. For details, refer to "**RA75X ASSEMBLER PACKAGE USER'S MANUAL—LANGUAGE (U12385E)**". If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are written as they are.

For immediate data, appropriate numbers and labels are written.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the registers can be written. However, there are restrictions in the labels that can be written for fmem and pmem. For details, refer to **User's Manual (U12020E)**.

Identifier	Format
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label [Note] 2-bit immediate data or label
fmem pmem	FB0H-FBFH, FF0H-FFFH immediate data or label FC0H-FFFH immediate data or label
addr, addr1 caddr faddr	0000H-0FFFH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H-7FH immediate data (where bit 0 = 0) or label
PORTn IExxx RBn MBn	PORT3, PORT8, PORT10 IEBT, IET0, IE1, IEW RB0-RB3 MB0, MB1, MB15

Note mem can be only used for even address in 8-bit data processing.

(2) Legend in explanation of operation

A	: A register, 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: XA register pair; 8-bit accumulator
BC	: BC register pair
DE	: DE register pair
HL	: HL register pair
XA'	: XA' expanded register pair
BC'	: BC' expanded register pair
DE'	: DE' expanded register pair
HL'	: HL' expanded register pair
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag, bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 3, 8, 10)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IExxx	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Separation between address and bit
(xx)	: The contents addressed by xx
xxH	: Hexadecimal data

(3) Explanation of symbols under addressing area column

*1	MB = MBE·MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 000H to FFFH	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
	addr1 = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 000H to FFFH	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 000H to FFFH	

Remarks 1. MB indicates memory bank that can be accessed.

2. In *2, MB = 0 independently of how MBE and MBS are set.

3. In *4 and *5, MB = 15 independently of how MBE and MBS are set.

4. *6 to *11 indicate the areas that can be addressed.

(4) Explanation of number of machine cycles column

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction Note: S = 2

Note 3-byte instruction: BR !addr, BRA !addr1, CALL !addr or CALLA !addr1 instruction

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of CPU clock (= t_{CY}); time can be selected from among four types by setting PCC.

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycles	Operation	Addressing area	Skip condition
Transfer instruction	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2+S	A ← (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ← (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2+S	A ↔ (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ↔ (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{11-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{11-8}+XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ Note	*6	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ Note	*6	

Note Be sure to assign “0” to register B.

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycles	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← (H+mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit, CY	2	2	(H+mem_{3-0}.bit) ← CY	*1	
Operation	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		XA, #n8	2	2+S	XA ← XA+n8		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
		XA, rp'	2	2+S	XA ← XA+rp'		carry
		rp'1, XA	2	2+S	rp'1 ← rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY ← XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1+XA+CY		
	SUBS	A, @HL	1	1+S	A ← A–(HL)	*1	borrow
		XA, rp'	2	2+S	XA ← XA–rp'		borrow
		rp'1, XA	2	2+S	rp'1 ← rp'1–XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A–(HL)–CY	*1	
		XA, rp'	2	2	XA, CY ← XA–rp'–CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1–XA–CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∀ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∀ XA		
Accumulator manipulation instructions	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		
Increment and Decrement instructions	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		rp1	1	1+S	rp1 ← rp1+1		rp1 = 00H
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0
	DECS	reg	1	1+S	reg ← reg–1		reg = FH
		rp'	2	2+S	rp' ← rp'–1		rp' = FFH

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycles	Operation	Addressing area	Skip condition
Comparison instruction	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
		XA, rp'	2	2+S	Skip if XA = rp'		XA = rp'
Carry flag manipulation instruction	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory bit manipulation instructions	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ←1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ←1	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ←1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ←0	*3	
		fmem.bit	2	2	(fmem.bit) ←0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ←0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ←0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY∧ (H+mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H+mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∀ (H+mem$_{3-0}$.bit)	*1	

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycles	Operation	Addressing area	Skip condition
Branch instructions	BR Note 1	addr	–	–	PC_{11-0} ← addr (Select appropriate instruction from among BR !addr, BRCB !caddr and BR $addr according to the assembler being used.)	*6	
		addr1	–	–	PC_{11-0} ← addr1 (Select appropriate instruction from among BR !addr BRA !addr1, BRCB !caddr and BR $addr1 according to the assembler being used.)	*11	
		!addr	3	3	PC_{11-0} ← addr	*6	
		$addr	1	2	PC_{11-0} ← addr	*7	
	BR	$addr1	1	2	PC_{11-0} ← addr1	*7	
		PCDE	2	3	PC_{11-0} ← PC_{11-8}+DE		
		PCXA	2	3	PC_{11-0} ← PC_{11-8}+XA		
		BCDE	2	3	PC_{11-0} ← BCDE Note 2	*6	
		BCXA	2	3	PC_{11-0} ← BCXA Note 2	*6	
	BRA Note 1	!addr1	3	3	PC_{11-0} ← addr1	*11	
	BRCB	!caddr	2	2	PC_{11-0} ← $caddr_{11-0}$	*8	
Subroutine stack control instructions	CALLA Note 1	!addr1	3	3	(SP–2) ← x, x, MBE, RBE (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 PC_{11-0} ← addr1, SP ← SP–6	*11	
	CALL Note 1	!addr	3	3	(SP–3) ←MBE, RBE, 0, 0 (SP–4) (SP–1) (SP–2) ← PC_{11-0} PC_{11-0} ← addr, SP ← SP–4	*6	
				4	(SP–2) ←x, x, MBE, RBE (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 PC_{11-0} ← addr, SP ← SP–6		
	CALLF Note 1	!faddr	2	2	(SP–3) ←MBE, RBE, 0, 0 (SP–4) (SP–1) (SP–2) ← PC_{11-0} PC_{11-0} ← 0+faddr, SP ← SP–4	*9	
				3	(SP–2) ← x, x, MBE, RBE (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 PC_{11-0} ← 0+faddr, SP ← SP–6		

Notes 1. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

2. "0" must be assigned to B register.

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycles	Operation	Addressing area	Skip condition
Subroutine stack control instructions	RET Note 1		1	3	PC_{11-0} ← (SP) (SP+3) (SP+2) MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4		
					x, x, MBE, RBE ← (SP+4) 0, 0, 0, 0, ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2), SP ← SP+6		
	RETS Note 1		1	3+S	MBE, RBE, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) SP ← SP+4 then skip unconditionally		Unconditional
					0, 0, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) x, x, MBE, RBE ← (SP+4) SP ← SP+6 then skip unconditionally		
	RETI Note 1		1	3	MBE, RBE, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6		
					0, 0, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP–1)(SP–2) ← rp, SP ← SP–2		
		BS	2	2	(SP–1) ← MBS, (SP–2) ← RBS, SP ← SP–2		
	POP	rp	1	1	rp ← (SP+1) (SP), SP ← SP+2		
		BS	2	2	MBS ←(SP+1), RBS ←(SP), SP ← SP+2		
Interrupt control instructions	EI		2	2	IME (IPS.3) ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IExxx	2	2	IExxx ← 0		
Input/output instructions	IN Note 2	A, PORTn	2	2	A ← PORTn (n = 3, 8, 10)		
	OUT Note 2	PORTn, A	2	2	PORTn ← A (n = 3, 8, 10)		
CPU control instructions	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special instructions	SEL	RBn	2	2	RBS ← n (n = 0-3)		
		MBn	2	2	MBS ← n (n = 0, 15)		

Notes 1. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

2. While the IN instruction and OUT instruction are being executed, the MBE must be set to 0 or 1 and MBS must be set to 15.

Instruction group	Mnemonic	Operand	Number of bytes	Machine cycles	Operation	Addressing area	Skip condition
Special instructions	GET Note 1, 2	taddr	1	3	• When TBR instruction $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$	*10	
					• When TCALL instruction $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, 0$ $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ $SP \leftarrow SP-4$		
					• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.		Depending on the reference instruction
				3	• When TBR instruction $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$	*10	
				4	• When TCALL instruction $(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$ $(SP-5) \leftarrow 0, 0, 0, 0$ $(SP-2) \leftarrow x, x, MBE, RBE$ $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ $SP \leftarrow SP-6$		
				3	• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.		Depending on the reference instruction

Notes 1. The TBR and TCALL instructions are the table definition assembler directives of the GETI instruction.

2. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

★ 12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

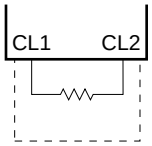
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Low-level output current	I_{OL}	Per pin	30	mA
		Total of all pins	220	mA
Ambient operating temperature	T_A		–10 to +60	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Pins other than tested pins: 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillation Circuit Characteristics (T_A = –10 to +60 °C, V_{DD} = 2.5 to 5.5 V)

Oscillator	Recommended Constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillation		Oscillation frequency (f_{CC}) Note	V_{DD} = 4.5 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 2.5 to 4.5 V	1.0		5.0	MHz

Note The oscillation frequency indicates characteristics of the oscillation circuit only. For the instruction execution time and oscillation frequency characteristics, refer to AC Characteristics.

Caution When using the main system clock frequency circuit, wire the portion enclosed by the dotted line in the above figure as follows to prevent adverse influence from wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Do not route the wiring in the vicinity of line through which a high alternating current flows.**
- **Do not extract any signal from the oscillation circuit.**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –10 to +60 °C, V_{DD} = 2.5 to 5.5 V)

Oscillation	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillation Note 1	Oscillation frequency (f_{CT}) Note 2	V_{DD} = 5.0 V ± 10 %	27	47	74	kHz
		V_{DD} = 3.0 V ± 10 %	27	47	74	kHz

Notes 1. The subsystem clock oscillation circuit incorporates a resistor (R) and a capacitor (C), and does not have external pins.

2. The oscillation frequency indicates characteristics of the oscillation circuit only. For the instruction execution time and oscillation frequency characteristics, refer to **AC Characteristics**.

DC Characteristics (T_A = –10 to +60 °C, V_{DD} = 2.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level output current	I_{OL}	Par pin				15	mA
		Total of all pins				150	mA
High-level input voltage	V_{IH1}	Ports 3, 8, P100-P102		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P103, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 3, 8, P100-P102		0		0.3V_{DD}	V
	V_{IL2}	P103, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
High-level output voltage	V_{OH1}	P31-P33, Ports 8, 10	I_{OH} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P30 (HCLK)		V_{DD} – 0.12			V
Low-level output voltage	V_{OL1}	P31-P33, Ports 8, 10	I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	P30 (HCLK)				0.19	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than CL1			3	μA
	I_{LIH2}		CL1			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Pins other than CL1			–3	μA
	I_{LIL2}		CL1			–20	μA
High-level output leakage current	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Internal pull-up resistor	R_{L1}	Port 10		50	100	200	kΩ
	R_{L2}	$\overline{\text{RESET}}$ (Mask option)		30	60	120	kΩ
LCD drive voltage	V_{LCD}			2.5		5.5	V
LCD divider resistor	R_{LCD}			50	100	200	kΩ
LCD output voltage deviation [Note 1] (common)	V_{ODC}	**Note 2** 2.5 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2	V
LCD output voltage deviation [Note 1] (segment)	V_{ODS}			0		±0.2	V

Notes 1. "Voltage deviation" means a difference between the output voltage and the ideal value of the segment and common outputs (V_{LCDn}: n = 0, 1, or 2).

2. The LCD controller/driver can select the following three display modes using a mask option:

(1) Static : V_{LCD0} = V_{LCD}

(2) 1/2 bias: V_{LCD0} = V_{LCD}
V_{LCD1} = V_{LCD} × 1/2

(3) 1/3 bias: V_{LCD0} = V_{LCD}
V_{LCD1} = V_{LCD} × 2/3
V_{LCD2} = V_{LCD} × 1/3

DC Characteristics (T_A = –10 to +60 °C, V_{DD} = 2.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1} Note 2	Main system clock 3.6 MHz RC oscillation Operation mode	V_{DD} = 5.0 V ± 10 % Note 3		2.1	5.3	mA
			V_{DD} = 5.0 V ± 10 %, T_A = 25 °C Note 3		2.1	4.2	mA
			V_{DD} = 3.0 V ± 10 % Note 4		0.70	1.8	mA
			V_{DD} = 3.0 V ± 10 %, T_A = 25 °C Note 4		0.70	1.5	mA
	I_{DD2} Note 2	Main system clock 3.6 MHz RC oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		1.4	3.5	mA
			V_{DD} = 5.0 V ± 10 %, T_A = 25 °C		1.4	2.8	mA
			V_{DD} = 3.0 V ± 10 %		0.65	1.6	mA
			V_{DD} = 3.0 V ± 10 %, T_A = 25 °C		0.65	1.3	mA
	I_{DD3} Note 5	Subsystem clock RC oscillation Operation mode	V_{DD} = 5.0 V ± 10 % Note 6		65	163	μA
			V_{DD} = 5.0 V ± 10 %, T_A = 25 °C Note 6		65	130	μA
			V_{DD} = 3.0 V ± 10 % Note 7		18	45	μA
			V_{DD} = 3.0 V ± 10 %, T_A = 25 °C Note 7		18	36	μA
	I_{DD4} Note 5	Subsystem clock RC oscillation HALT mode	V_{DD} = 5.0 V ± 10 % Note 6		58	150	μA
			V_{DD} = 5.0 V ± 10 %, T_A = 25 °C Note 6		58	120	μA
			V_{DD} = 3.0 V ± 10 % Note 7		9.5	25	μA
			V_{DD} = 3.0 V ± 10 %, T_A = 25 °C Note 7		9.5	20	μA
	I_{DD4} Note 8	STOP mode	V_{DD} = 5.0 V ± 10 %		0.05	10	μA
			V_{DD} = 5.0 V ± 10 %, T_A = 25 °C		0.05	5	μA
			V_{DD} = 3.0 V ± 10 %		0.02	5	μA
			V_{DD} = 3.0 V ± 10 %, T_A = 25 °C		0.02	3	μA

Notes 1. The current flowing through the internal pull-up resistor and LCD divider resistor is not included.

2. When an external 6.8-kΩ resistor is connected. However, the temperature characteristics of the resistor are not included.

3. When the μPD753304 operates in the high-speed mode with the processor clock control resistor (PCC) set to 0011.

4. When the μPD753304 operates in the low-speed mode with the PCC reset to 0000.

5. When the μPD753304 operates with the subsystem clock by setting the system clock control resistor (SCC) to 1001 and stopping the main system clock oscillation.

6. The subsystem clock oscillation frequency (f_{CT}) is 60 kHz when V_{DD} = 5.0 V ± 10%.

7. The subsystem clock oscillation frequency (f_{CT}) is 55 kHz when V_{DD} = 3.0 V ± 10%.

8. When both the main system clock and subsystem clock are stopped by setting the sub oscillation circuit stop enable flag (SOS.3) to 1.

AC Characteristics (T_A = –10 to +60 °C, V_{DD} = 2.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Main system clock frequency deviation	f_{CC}	V_{DD} = 5.0 V ± 10 %, R = 6.8 kΩ		3.1	3.7	4.3	MHz
			T_A = 25 °C	3.3	3.7	4.0	MHz
		V_{DD} = 3.0 V ± 10 %, R = 6.8 kΩ		2.8	3.6	4.2	MHz
			T_A = 25 °C	3.0	3.6	3.9	MHz
Subsystem clock frequency deviation	f_{CT}	V_{DD} = 5.0 V ± 10 %		27	47	74	kHz
		V_{DD} = 3.0 V ± 10 %		27	47	74	kHz
Main system clock duty factor Note 1	f_{duty}	V_{DD} = 5.0 V ± 10 %		45		55	%
		V_{DD} = 3.0 V ± 10 %		40		60	%
CPU clock cycle time Note 2 (Minimum instruction execution time = 1 machine cycle)	t_{CY}	Operates with main system clock	V_{DD} = 4.5 to 5.5 V	0.67		64	μs
			V_{DD} = 2.5 to 4.5 V	0.80		64	μs
		Operates with subsystem clock		54		148	μs
Interrupt input high-, low-level width	t_{INTH}, t_{INTL}	INT1		10			μs
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

Notes 1. Main system clock duty factor = high-level width of 1 clock/1 cycle of clock

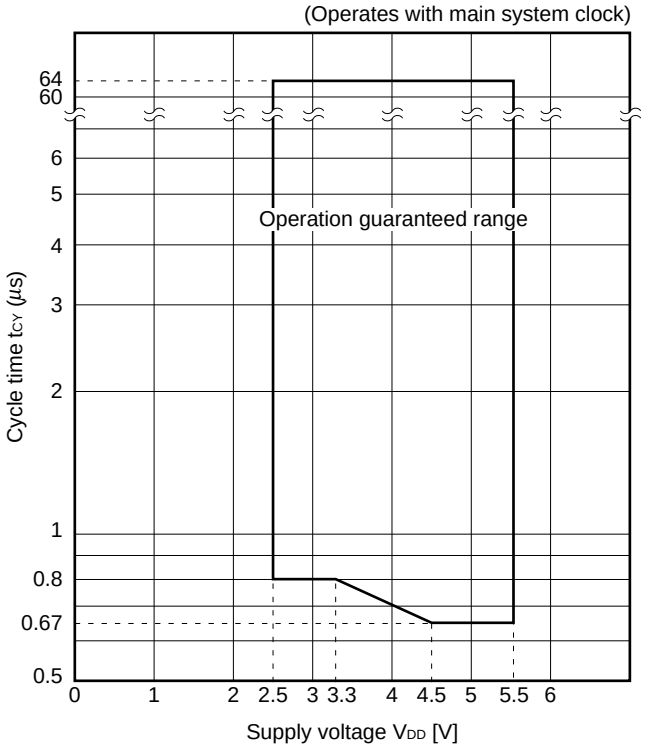
2. The cycle time (minimum instruction execution time) of the CPU clock (Φ) when the device operates with the main system clock is determined by the time constant of the internal capacitor (C: 10-pF typ.) and an externally connected resistor (R), and by the system clock control register (SCC) and processor clock control register (PCC).

The cycle time of the CPU clock (Φ) when the device operates with the subsystem clock is determined by the time constant of the internal capacitor (C) and an internal resistor (R).

The figure on the right shows the dependency of the cycle time t_{CY} on supply voltage V_{DD} when the device operates with the main system clock.

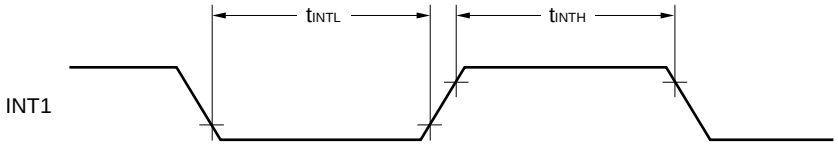
t_{CY} vs V_{DD}

(Operates with main system clock)

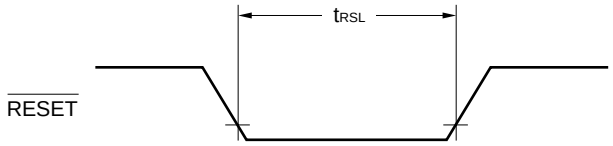


AC timing test points

Interrupt input timing



$\overline{\text{RESET}}$ input timing



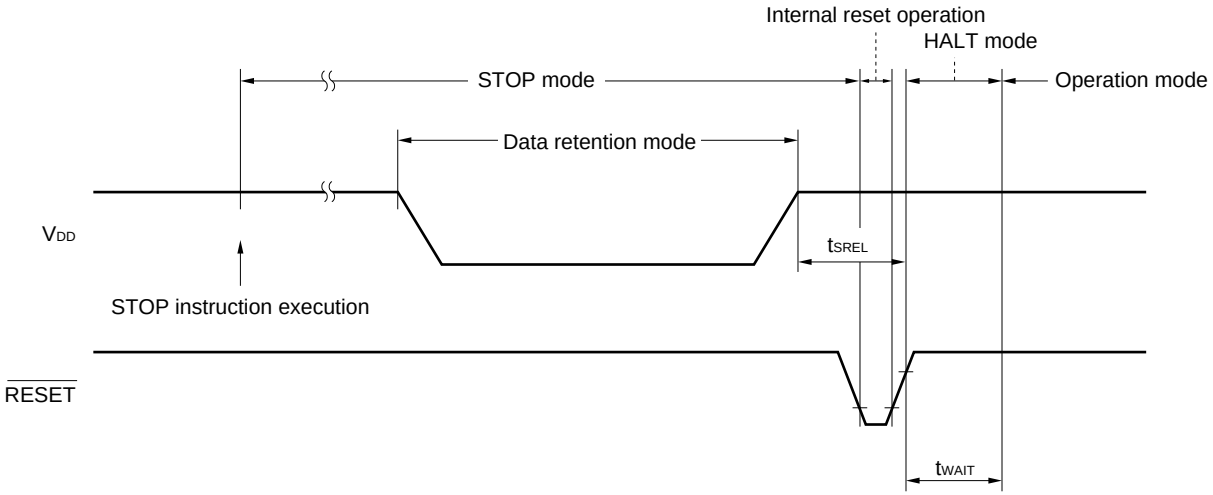
Data retention characteristics of data memory in STOP mode and at low supply voltage (T_A = –10 to +60 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Released by $\overline{RESET}$		56/f_{CC}		μs
		Released by interrupt request		**Note 2**		μs

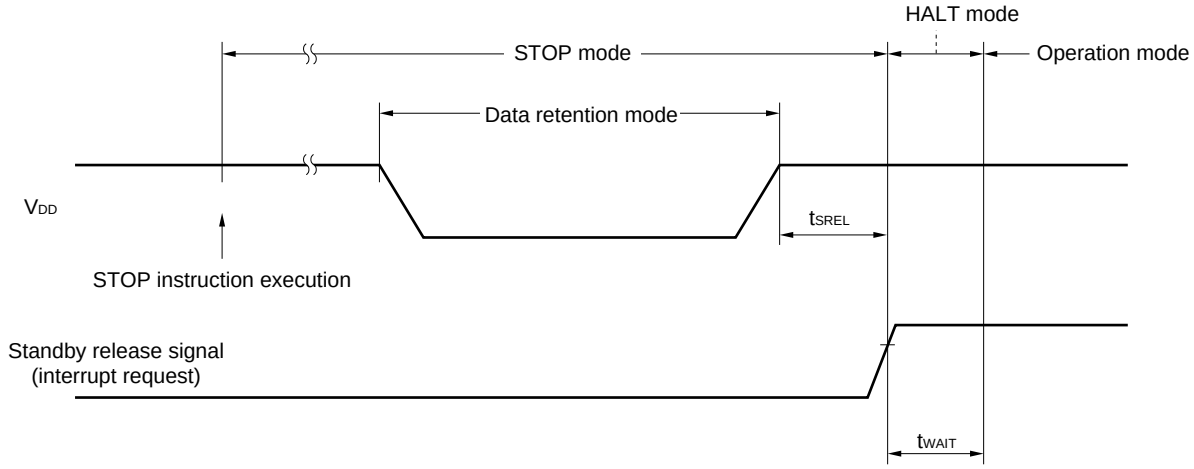
Notes 1. The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.

2. Either $2^9/f_{CC}$ or no wait can be selected by mask option.

Data retention timing (when STOP mode released by $\overline{RESET}$)

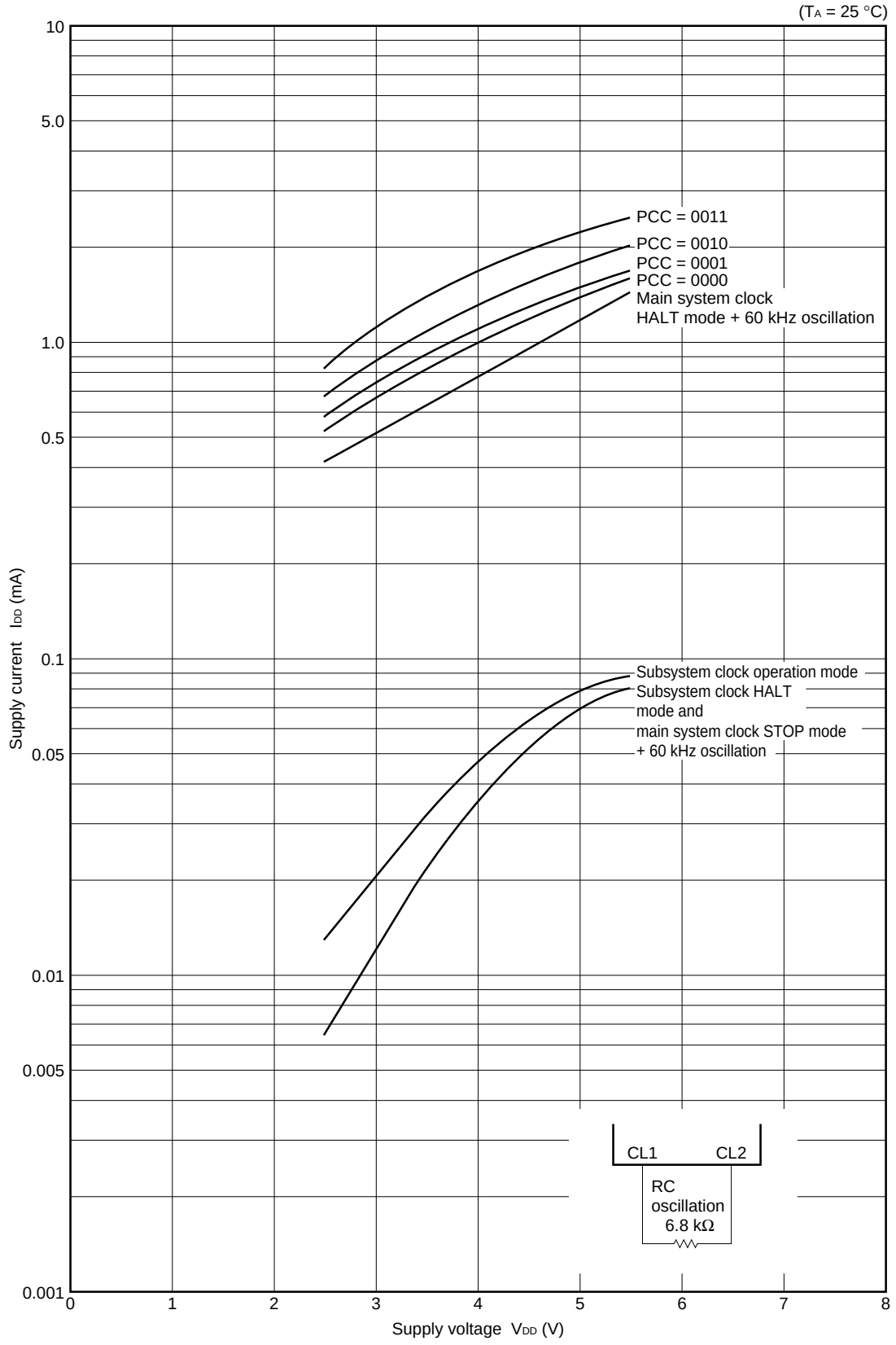


Data retention timing (standby release signal: when STOP mode released by interrupt signal)



★ 13. CHARACTERISTIC CURVE (reference)

I_{DD} vs V_{DD} (main system clock: 3.6 MHz RC oscillation (with 6.8-kΩ external resistor connected), subsystem clock : 60 kHz RC oscillation)



APPENDIX A. μPD75308B, 753108 AND 753304 FUNCTIONAL LIST

Parameter		μPD75308B	μPD753108	μPD753304
Program memory		Mask ROM 0000H to 1F7FH (8064 × 8 bits)	Mask ROM 0000H to 1FFFH (8192 × 8 bits)	Mask ROM 0000H to 0FFFH (4096 × 8 bits)
Data memory		000H to 1FFH (512 × 4 bits)		000H to 0FFH (256 × 4 bits)
CPU		75X Standard	75XL CPU	
Main system clock oscillation circuit		Crystal/ceramic oscillation circuit		RC oscillation circuit
Subsystem clock oscillation circuit		Crystal oscillation circuit		RC oscillation circuit
Wait time when released by $\overline{\text{RESET}}$ signal		2^{17}/fx	2^{17}/fx, 2^{15}/fx (Selected by mask option)	56/fcc
Wait time when STOP mode is released by interrupt occurrence		2^{20}/fx, 2^{17}/fx, 2^{15}/fx, 2^{13}/fx (Selected by setting of BTM)		512/fcc, with no wait (Selected by mask option)
Clock oscillation circuit which can executes STOP instruction		Main system clock oscillation circuit		Main system clock oscillation circuit and subsystem clock oscillation circuit
★ Instruction execution time	When main system clock is selected	0.95, 1.91, 15.3 μs (during 4.19-MHz operation)	• 0.95, 1.91, 3.81, 15.3 μs (during 4.19-MHz operation) • 0.67, 1.33, 2.67, 10.7 μs (during 6.0-MHz operation)	1.1, 2.2, 4.4, 17.8 μs (during 3.6-MHz operation)
★	When subsystem clock is selected	122 μs (during 32.768-kHz operation)		85.1 μs (during 47-kHz operation)
Stack	SBS register	None	SBS.3 = 1: Mk I mode selection SBS.3 = 0: Mk II mode selection	
	Stack area	000H to 0FFH	000H to 1FFH	0000H to 0FFH
	Subroutine call instruction stack operation	2-byte stack	When Mk I mode: 2-byte stack When Mk II mode: 3-byte stack	
Instruction	BRA !addr1 CALLA !addr1	Unavailable	When Mk I mode: unavailable When Mk II mode: available	

	MOVT XA, @BCDE
	MOVT XA, @BCXA
	BR BCDE
	BR BCXA
			Available	

	CALL !addr	3 machine cycles	Mk I mode: 3 machine cycles, Mk II mode: 4 machine cycles	
	CALLF !faddr	2 machine cycles	Mk I mode: 2 machine cycles, Mk II mode: 3 machine cycles	
I/O port	CMOS input	8	8	0
	CMOS input/output	16	20	12
	Bit port output	8	0	0
	N-ch open-drain input/output	8	4	0
	Total	40	32	12

	Parameter		μPD75308B	μPD753108	μPD753304
	LCD controller/driver		Segment selection: 24/28/32 segments (can be changed to CMOS I/O port in 4 time-unit; max. 8)	Segment selection: 16/20/24 segments (can be changed to CMOS I/O port in 4 time-unit; max. 8)	Segment selection: 20/24 segments (can be changed to CMOS I/O port in 4-time unit; max. 4)
			Display mode selection: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)		
★			On-chip split resistor for LCD driver can be specified by using mask option		On-chip split resistor for LCD driver
★			LCD driving voltage can not be selected		
	Timer		3 channels • Basic interval timer: 1 channel • 8-bit timer/event counter: 1 channel • Watch timer: 1 channel	5 channels • Basic interval timer/ watchdog timer: 1 channel • 8-bit timer/event counter: 3 channels (can be used as 16-bit timer/event counter) • Watch timer: 1 channel	3 channels • Basic interval timer/ watchdog timer: 1 channel • 8-bit timer counter: 1 channel (with subclock source input function) • Watchtimer: 1 channel
★	Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation)	• Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation) • Φ, 750, 375, 93.8 kHz (Main system clock: during 6.0-MHz operation)	• Φ, 3.6 MHz, 450 kHz, 225 kHz (Main system clock: during 3.6-MHz operation)
★	BUZ output (BUZ)		2 kHz (Main system clock: during 4.19-MHz operation)	• 2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation) • 2.93, 5.86, 46.9 kHz (Main system clock: 6.0-MHz operation)	• 2.94, 5.88, 47 kHz (Subsystem clock: during 47-kHz operation) • 1.76, 3.52, 28.13-kHz (Main system clock: during 3.6-MHz operation)
	Serial interface		3 modes are available • 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit • 2-wire serial I/O mode • SBI mode		None
	SOS register	Feedback resistor cut flag (SOS.0)	None	Contained	None
		Subsystem clock oscillation circuit current cut flag (SOS.1)	None	Contained	None
		Sub oscillation circuit stop enable flag (SOS.3)	None		Contained
	Register bank selection register (RBS)		None	Yes	
	Vectored interrupt		External: 3, internal: 3	External: 3, internal: 5	External: 1, internal: 2
	Supply voltage		V_{DD} = 2.0 to 6.0 V	V_{DD} = 1.8 to 5.5 V	V_{DD} = 2.5 to 5.5 V
★	Operating ambient temperature		T_A = –40 to +85 °C		T_A = –10 to +60 °C
★	Package		• 80-pin plastic QFP (14 × 20 mm) • 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (Fine pitch) (12 × 12 mm)	• 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic QFP (12 × 12 mm)	• Volume production product: Pellet/wafer • ES product (for evaluation): 42-pin ceramic shrink DIP (600 mil)

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD753304.

In the 75XL series, the relocatable assembler which is common to the series is used in combination with the device file of each product.

Language processor

RA75X relocatable assembler	Host machine	OS	Distribution media	Part number (product name)
	PC-9800 series	MS-DOS™ (Ver. 3.30 to Ver. 6.2 Note)	3.5-inch 2HD	μS5A13RA75X
			5-inch 2HD	μS5A10RA75X
	IBM PC/AT™ and compatible machines	Refer to "**OS for IBM PC**"	3.5-inch 2HC	μS7B13RA75X
			5-inch 2HC	μS7B10RA75X

Device file	Host machine	OS	Distribution media	Part number (product name)
	PC-9800 series	MS-DOS (Ver. 3.30 to Ver. 6.2 Note)	3.5-inch 2HD	μS5A13DF753304
			5-inch 2HD	μS5A10DF753304
	IBM PC/AT and compatible machines	Refer to "**OS for IBM PC**"	3.5-inch 2HC	μS7B13DF753304
			5-inch 2HC	μS7B10DF753304

Note Ver.5.00 and later have the task swap function, but it cannot be used for this software.

Remark Operation of the assembler and the device file are guaranteed only on the above host machine and OSs.

Debugging tool

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD753304.

The system configurations are described as follows.

Hardware	IE-75000-R Note 1	In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD753304, the emulation board IE-75300-R-EM and emulation probe EP-753304DU-R that are sold separately must be used with the IE-75000-R. By connecting with the host machine, efficient debugging can be made. It contains the emulation board IE-75000-R-EM which is connected.			
	IE-75001-R	In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD753304, the emulation board IE-75300-R-EM and emulation probe EP-753304DU-R which are sold separately must be used with the IE-75001-R. It can debug the system efficiently by connecting the host machine.			
	IE-75300-R-EM	Emulation board for evaluating the application systems that use a μPD753304. It must be used with the IE-75000-R or IE-75001-R.			
★	EP-753304DU-R	Emulation probe for ES products. It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM.			
Software	IE control program	Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the above hardware on a host machine.			
		Host machine	OS	Distribution media	Part No. (product name)
		PC-9800 series	MS-DOS (Ver. 3.30 to Ver. 6.2 Note 2)	3.5-inch 2HD	μS5A13IE75X
				5-inch 2HD	μS5A10IE75X
		IBM PC/AT and compatible machines	Refer to "**OS for IBM PC**"	3.5-inch 2HC	μS7B13IE75X
				5-inch 2HC	μS7B10IE75X

Notes 1. Maintenance parts.

2. Ver.5.00 and later have the task swap function, but it cannot be used for this software.

Remark Operation of the IE control program is guaranteed only on the above host machines and OSs.

OS for IBM PC

The following IBM PC OS's are supported.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.3 J6.1/V Note to J6.3/V Note
MS-DOS	Ver. 5.0 to Ver. 6.22 5.0/V Note to 6.2/V Note
IBM DOS™	J5.02/V Note

Note Only the English mode is supported.

Caution Ver. 5.0 and later have the task swap function, but it cannot be used for this software.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device Related Documents

Document Name	Document No.	
	English	Japanese
μPD753304 Data Sheet	This document	U11874J
μPD753304 User's Manual	U12020E	U12020J
75XL Series Selection Guide	U10453E	U10453J

Development Tool Related Documents

Document Name			Document No.	
			English	Japanese
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416	EEU-846
	IE-75300-R-EM User's Manual		U11354E	U11354J
	EP-753304DU-R User's Manual		U12173E	U12173J
Software	RA75X Assembler Package	Operation	EEU-1346	U12622J
	User's Manual	Language	EEU-1363	U12385J

Other Related Documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Electrostatic Discharge (ESD) Test	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	C11893J
Microcomputer related Product Guide - Other Manufacturers	—	U11416J

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Tel: 800-366-9782
Fax: 800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Tel: 01908-691-133
Fax: 01908-670-290

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Tel: 040-2445845
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Tel: 01-30-67 58 00
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Fax: 2886-9022/9044

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Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

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United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

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Sao Paulo-SP, Brasil
Tel: 011-889-1680
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