DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

µPD76F0018

V850E/VANStorm™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER
WITH CAN AND VAN INTERFACES

DESCRIPTION

The V850E/VANStorm single chip microcontroller, is a member of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.
The V850E/VANStorm offers an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI), timers and measurement inputs (A/D converter), with dedicated CAN and VAN network support. To support more than one network, two VAN interfaces and one CAN interface are implemented on chip. The device offers power-saving modes to manage the power consumption effectively under varying conditions. Thus equipped, the V850E/VANStorm is ideally suited for automotive applications.

Functions in detail are described in the following user's manuals. Be sure to read these manuals when you design your systems.

V850E/VANStorm User's Manual - Hardware	**: U14879EE1V0UM00**
V850E Family™ User's Manual - Architecture	**: U14559EJ1**

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- Full-VAN Interface: 2 channels
- Full-CAN Interface: 1 channel
- Serial Interfaces: 4 channels
  - 3-wire mode: 2 channels
  - UART mode: 2 channels
- Timers: 7 channels
  - 16/32-bit multi purpose timer/event counter: 3 channels
  - 16-bit OS timer: 2 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- 10-bit resolution A/D Converter: 12 channels
- I/O lines: 89
- External Bus Interface (16-bit data / 24-bit address bus)
- Power supply voltage range: 4.5 V $\leq V_{DD5} \leq$ 5.5 V
- Frequency range: up to 20 MHz
- Crystal frequency range: 4 MHz $\leq f_{CRYSTAL} \leq$ 5 MHz
- Built-in voltage monitor with low voltage detection (selectable threshold and hysteresis)
- Built-in low power saving mode
- Built-in clock oscillator circuit with internal PLL
- Vectored interrupts: 49
- Temperature range: -40 °C to +85 °C
- Package: 144 QFP, 0.5 mm pin-pitch (20 x 20 mm)

ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	Oper. Freq.
V850E/VANStorm	µPD76F0018	QFP144 20 x 20 mm	256 K Flash	8 K	20 MHz

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

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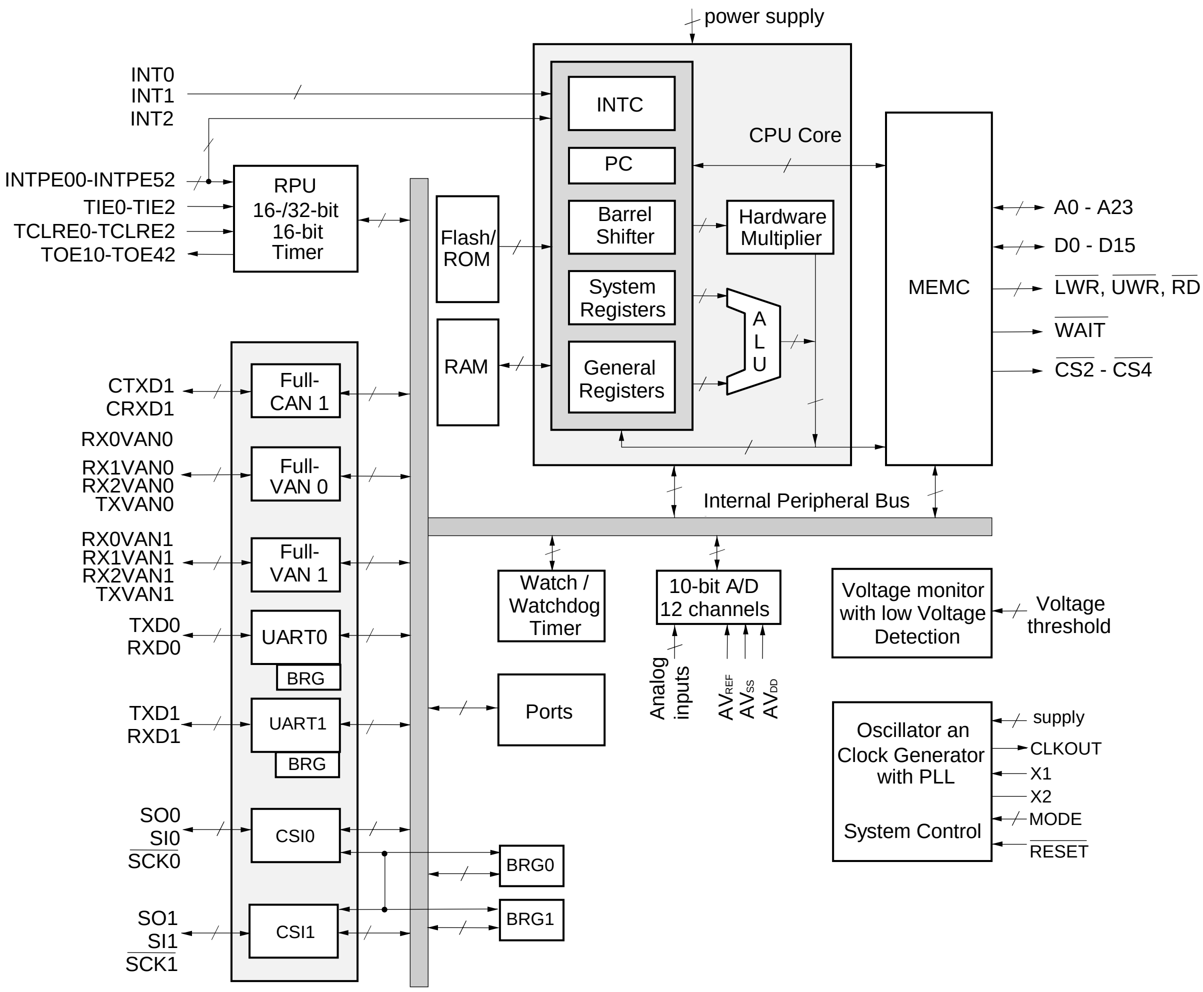
Data Published: January 2002

INTERNAL BLOCK DIAGRAM



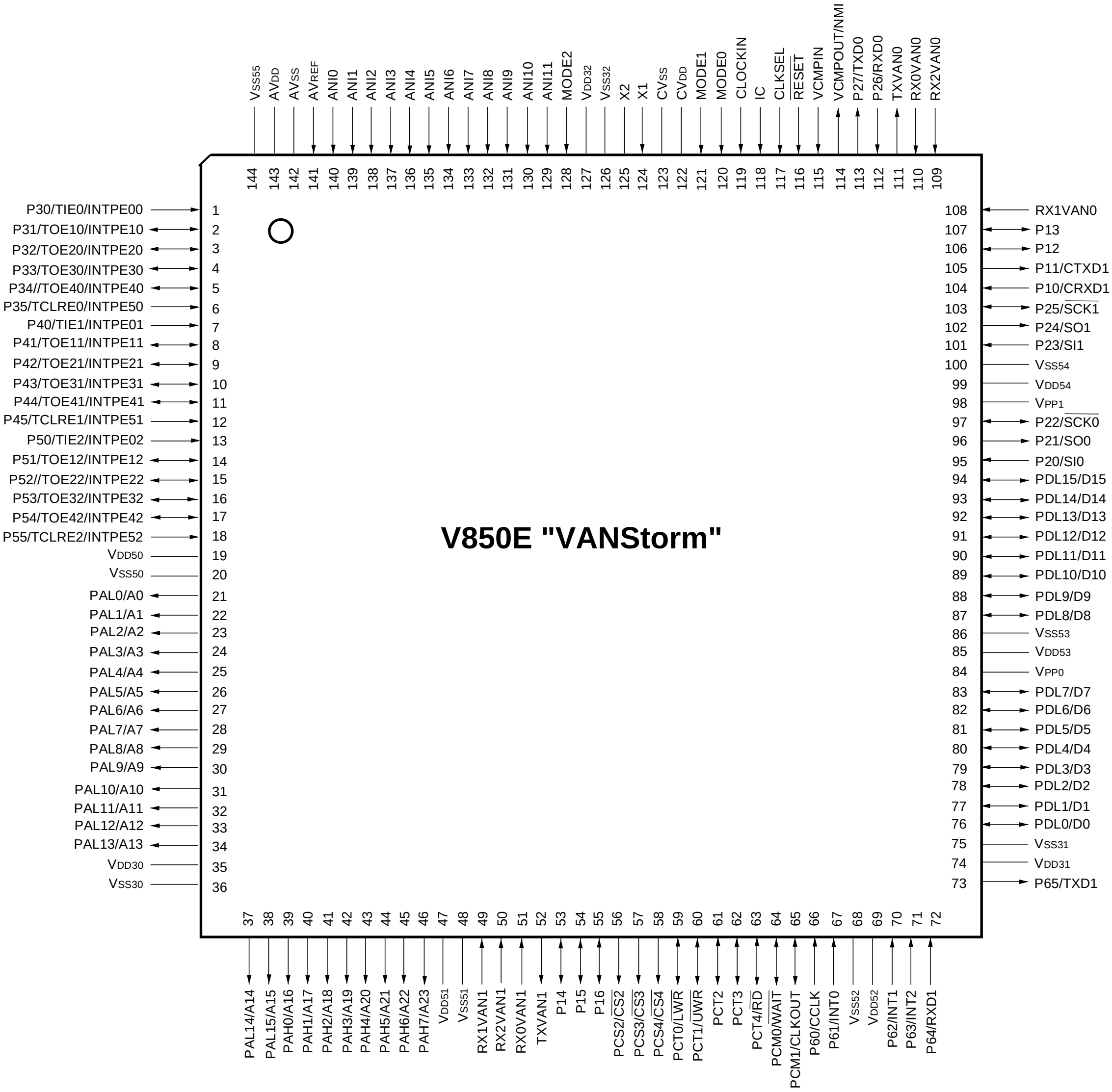
PIN IDENTIFICATION

A0 - A23	Address Bus
ANI0 - ANI11	Analogue Inputs
AV_{DD}	Power Supply +5 V
AV_{REF}	Analogue Reference Voltage
AV_{SS}	Power Supply Ground
CCLK	External CAN Clock Input
CLOCKIN	External System Clock Input
CLKSEL	Clock Selection Configuration Input
CLKOUT	Clock Output
CV_{DD}	Voltage Regulator Capacitor Connection
CV_{SS}	Voltage Regulator Capacitor Connection
CRXD1	CAN Receive Data Inputs
CTXD1	CAN Transmit Data Outputs
$\overline{\text{CS2}}$ - $\overline{\text{CS4}}$	Chip Select Outputs for accessing external devices
D0 - D15	Data Bus
IC	Always connect to V_{SS5x}
INT0 - INT2	External Interrupt Inputs
INTPE00- INTPE52	Shared External Interrupt Inputs
MODE0 - MODE2	Global Operation Mode Selection Inputs
NMI	Non Maskable Interrupt Input
P1x - P6x	Multi-Purpose I/O Ports, shared with other functions
PALx, PAHx	Multi-Purpose I/O Ports, shared with other functions
PCMx	Multi-Purpose I/O Ports, shared with other functions
PCSx	Multi-Purpose I/O Ports, shared with other functions
PCTx	Multi-Purpose I/O Ports, shared with other functions
PDLx	Multi-Purpose I/O Ports, shared with other functions

RX0VAN0 - RX0VAN1	VAN Receive Data Inputs
RX1VAN0 - RX1VAN1	VAN Receive Data Inputs
RX2VAN0 - RX2VAN1	VAN Receive Data Inputs
RXD0 - RXD1	Receive Data Inputs
$\overline{\text{RESET}}$	System Reset Input
$\overline{\text{RD}}$	Read Data Control Signal
$\overline{\text{SCK0}}$ - $\overline{\text{SCK1}}$	Serial Clock
SI0 - SI1	Serial Input
SO0 - SO1	Serial output
TCLRE0 - TCLRE2	External Function Control Inputs
TIE0 - TIE2	External Count Clock Inputs
TOE10 - TOE42	Function Outputs (PWM)
TXD0 - TXD1	Transmit Data Outputs
TXVAN0 - TXVAN1	VAN Transmit Data Outputs
VCMPOUT	Hysteresis Feedback Output
VCMPIN	Voltage Surveillance Sense Input
V_{DD30} - V_{DD32}	Voltage Regulator Capacitor Connection
V_{DD50} - V_{DD54}	Power Supply +5 V
V_{PP0} - V_{PP1}	Programming Voltage Inputs
V_{SS50} - V_{SS55}	Power Supply Ground
V_{SS30} - V_{SS32}	Voltage Regulator Capacitor Connection and Ground
$\overline{\text{WAIT}}$	Waitstate Input for external devices
$\overline{\text{LWR}}$ - $\overline{\text{UWR}}$	Write Data Control Signal
X1	Oscillator quartz connection
X2	Oscillator quartz connection

PIN CONFIGURATION

- 144-Pin Plastic QFP (Top View)



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1. PIN FUNCTIONS

1.1 Port Pins

Table 1-1: Pin Functions: Ports

Port	I/O	Function	Driver Type	Alternate1	Alternate2	Alternate2
P10	I/O	Port 1 7-bit input/output port	5-K	CRXD0		
P11				CTXD0		
P12						
P13						
P14						
P15						
P16						
P20	I/O	Port 2 8-bit input/output port	5	SI0		
P21			5-K	SO0		
P22			5	$\overline{\text{SCK0}}$		
P23			5-K	SI1		
P24				SO1		
P25				$\overline{\text{SCK1}}$		
P26				RXD0		
P27				TXD0		
P30	I/O	Port 3 6-bit input/output port	5-K	TIE00	INTPE00	
P31				TIE10	TOE10	INTPE10
P32				TIE20	TOE20	INTPE20
P33				TIE30	TOE30	INTPE30
P34				TIE40	TOE40	INTPE40
P35				TIE50	TCLRE0	INTPE50
P40	I/O	Port 4 6-bit input/output port	5-K	TIE01	INTPE01	
P41				TIE11	TOE11	INTPE11
P42				TIE21	TOE21	INTPE21
P43				TIE31	TOE31	INTPE31
P44				TIE41	TOE41	INTPE41
P45				TIE51	TCLRE1	INTPE51
P50	I/O	Port 5 6-bit input/output port	5-K	TIE0	INTPE02	
P51				TIE12	TOE12	INTPE12
P52				TIE22	TOE22	INTPE22
P53				TIE32	TOE32	INTPE32
P54				TIE42	TOE42	INTPE42
P55				TIE52	TCLRE2	INTPE52
P60	I/O	Port 6 6-bit input/output port	5-K	CCLK		
P61				INT0		
P62				INT1		
P63				INT2		
P64				RXD1		
P65				TXD1		

Table 1-1: Pin Functions: Ports

Port	I/O	Function	Driver Type	Alternate1	Alternate2	Alternate2
PAL0	I/O	Port AL 16-bit input/output port	5-K	A0		
PAL1				A1		
PAL2				A2		
PAL3				A3		
PAL4				A4		
PAL5				A5		
PAL6				A6		
PAL7				A7		
PAL8				A8		
PAL9				A9		
PAL10				A10		
PAL11				A11		
PAL12				A12		
PAL13				A13		
PAL14				A14		
PAL15				A15		
PAH0	I/O	Port AH 8-bit input/output port	5	A16		
PAH1				A17		
PAH2				A18		
PAH3				A19		
PAH4				A20		
PAH5				A21		
PAH6				A22		
PAH7				A23		
PDL0	I/O	Port DL 16-bit input/output port	5-K	D0		
PDL1				D1		
PDL2				D2		
PDL3				D3		
PDL4				D4		
PDL5				D5		
PDL6				D6		
PDL7				D7		
PDL8				D8		
PDL9				D9		
PDL10				D10		
PDL11				D11		
PDL12				D12		
PDL13				D13		
PDL14				D14		
PDL15				D15		
PCM0	I/O	Port CM 2-bit input/output port	5-K	$\overline{\text{WAIT}}$		
PCM1				CLKOUT		

Table 1-1: Pin Functions: Ports

Port	I/O	Function	Driver Type	Alternate1	Alternate2	Alternate2
PCS2	I/O	Port CS 3-bit input/output port	5-K	$\overline{\text{CS2}}$		
PCS3				$\overline{\text{CS3}}$		
PCS4				$\overline{\text{CS4}}$		
PCT0	I/O	Port CT 5-bit input/output port	5-K	$\overline{\text{WR0}}$		
PCT1				$\overline{\text{WR1}}$		
PCT2						
PCT3						
PCT4				$\overline{\text{RD}}$		

1.2 Other Pins

Table 1-2: Pin Functions: Functions

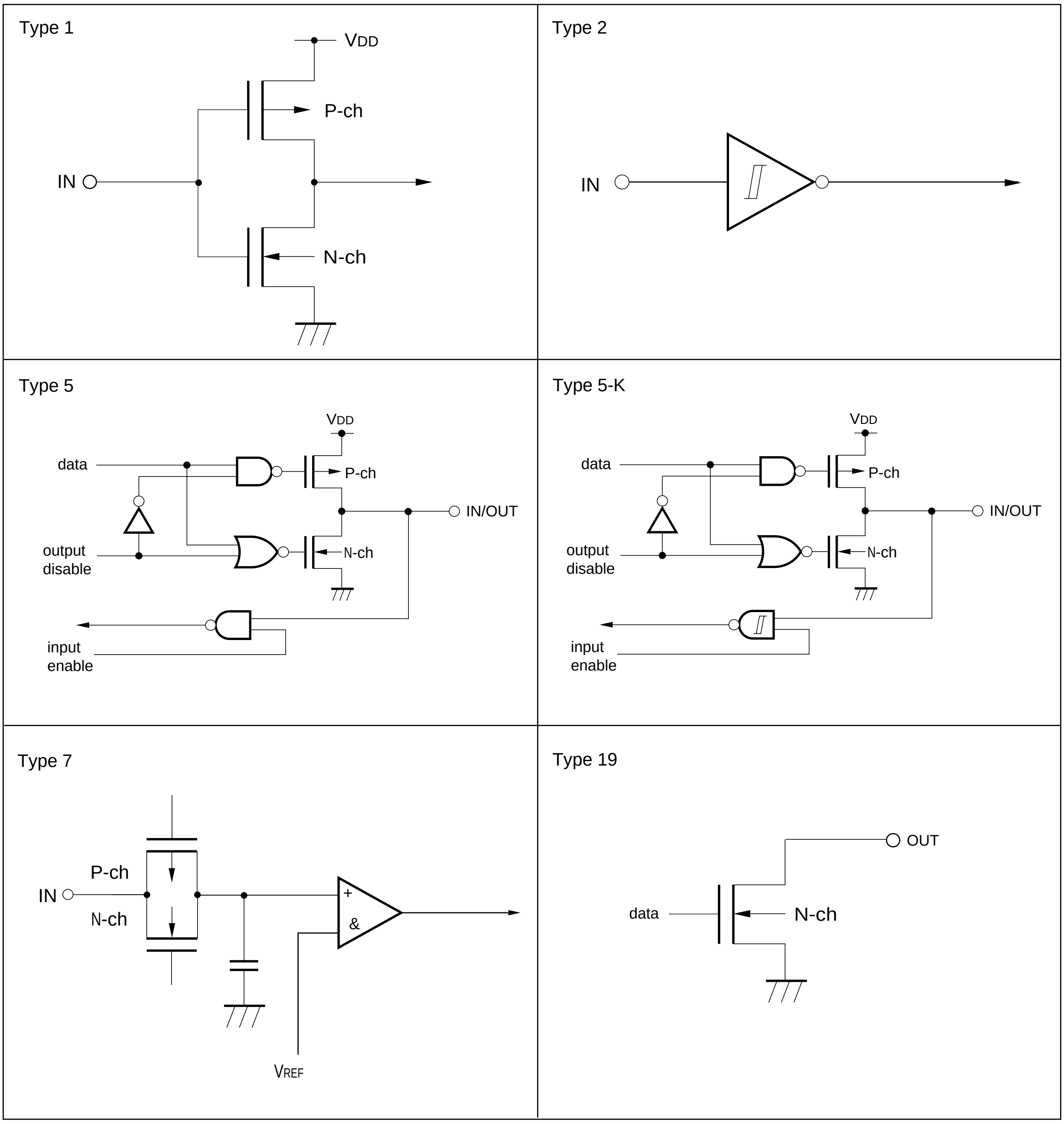
Pin Name	I/O	Function	Termination	Driver Type
V_{DD50} - V_{DD54}	-	Power supply 5 V		-
V_{SS50} - V_{SS55}				
V_{DD30} - V_{DD32}	-	Connection for external capacities[Note]		-
V_{SS30} - V_{SS32}		Connection for external capacities, connect to V_{SS5x}		
CV_{DD}	-	Connection for external capacities to stabilize clock oscillator power supply		-
CV_{SS}		Connection for external capacities to stabilize clock oscillator power supply, connect to V_{SS5x}		
X1	input	System clock oscillator connection pins.	See Chapter 3.4 on page 18	-
X2	-			-
CLOCKIN	input	External system clock input	10 K to V_{SS5x}	2
V_{PP0}, V_{PP1}	-	Flash memory programming voltage	10 K to V_{SS5x}	-
MODE1	input	Selects operating mode (internal rom / rom less)	V_{DD5} or V_{SS5x}	2
MODE0, MODE2	input	Have to be fixed to V_{SS}	V_{SS5x}	2
$\overline{RESET}$	input	System reset input		2
CLKOUT	output	Internal CPU system clock output	-	5-K
CLKSEL	input	Clock generator operation mode	10 K V_{DD5x} or V_{SS5x}	2
AV_{DD}	-	Power supply for A/D converter	V_{DD5x}	-
AV_{SS}			V_{SS5x}	-
AV_{REF}	input	reference voltage input for A/D converter	AV_{DD}	-
NMI	input	non maskable interrupt input	100 K to V_{DD5x}	5-K
VCMPOUT	output	voltage comparator feedback output	-	1
VCMPIN	input	voltage comparator compare input	100 K to V_{DD5x}	
ANI0 - ANI11	input	analog input to A/D converter	V_{SS5x}	7
IC	input	internal connection (connect to V_{SS5x})	V_{SS5X}	-
SI0	input	serial receive data input to CSI0-CSI1	100 K to V_{DD5x}	5
SI1			100 K to V_{DD5x}	5-K
SO0	output	serial transmit data output from CSI0-CSI1	100 K to V_{DD5x}	5-K
SO1			100 K to V_{DD5x}	5-K
$\overline{SCK0}$	I/O	serial clock I/O from CSI0	100 K to V_{DD5x}	5
$\overline{SCK1}$	I/O	serial clock I/O from CSI1	100 K to V_{DD5x}	5-K
RXD0	input	serial receive data input to UART0-UART2	100 K to V_{DD5x}	5-K
RXD1			100 K to V_{DD5x}	5-K
TXD0	output	serial transmit data output from UART0-UART2	100 K to V_{DD5x}	5-K
TXD1			100 K to V_{DD5x}	5-K
CRXD1	input	serial receive data input to FCAN0	100 K to V_{DD5x}	5-K

Table 1-2: Pin Functions: Functions

Pin Name	I/O	Function	Termination	Driver Type
CTXD1	output	serial transmit data output from FCAN0	100 K to V_{DD5x}	5-K
RX0VAN0	input	serial receive data input to FVAN0	100 K to V_{DD5x}	2
RX1VAN0	input		100 K to V_{DD5x}	
RX2VAN0	input		100 K to V_{DD5x}	
RX0VAN1	input	serial receive data input to FVAN1	100 K to V_{DD5x}	2
RX1VAN1	input		100 K to V_{DD5x}	
RX2VAN1	input		100 K to V_{DD5x}	
TXVAN0	output	serial transmit data output from FVAN0	100 K to V_{DD5x}	19
TXVAN1	output	serial transmit data output from FVAN1	100 K to V_{DD5x}	19
CCLK	input	CAN clock input	100 K to V_{DD5x}	5-K
D0 - D15	I/O	data bus of external bus	PDL0 - PDL15, 100 K to V_{DD5x}	5-K
A0 -A7	output	address bus of external bus	100 K to V_{DD5x}	5
A8 - A15				
A16 - A23				
$\overline{WR0}$	I/O	write strobe lower byte (bit 0 -7)	100 K to V_{DD5x}	5-K
$\overline{WR1}$		write strobe upper byte (bit 8 -15)	100 K to V_{DD5x}	5-K
$\overline{RD}$		read strobe for external bus	100 K to V_{DD5x}	5-K
$\overline{WAIT}$	input	control signal input for external bus	100 K to V_{DD5x}	5-K
$\overline{CS2}$ - $\overline{CS4}$	output	chip select output for external bus	PCS2 - PCS4 100 K to V_{DD5x}	5-K
INT0 - INT2	input	external interrupt request	100 K to V_{DD5x}	5-K
TIE0	input	Timer E channel 0 capture 0 input	100 K to V_{DD5x}	5-K
TOE10 - TOE40	I/O	Timer E channel 0 capture 1 - 4 input/output	100 K to V_{DD5x}	5-K
TCLRE0	input	Timer E channel 0 capture 5 input or timer clear input	100 K to V_{DD5x}	5-K
TIE1	input	Timer E channel 1 capture 0 input	100 K to V_{DD5x}	5-K
TOE11 - TOD41	I/O	Timer E channel 1 capture 1 - 4 input/output	100 K to V_{DD5x}	5-K
TCLRE1	input	Timer E channel 1 capture 5 input or timer clear input	100 K to V_{DD5x}	5-K
TIE2	input	Timer E channel 2 capture 0 input	100 K to V_{DD5x}	5-K
TOE12 - TOE42	I/O	Timer E channel 2 capture 1 - 4 input/output	100 K to V_{DD5x}	5-K
TCLRE2	input	Timer E channel 2 capture 5 input or timer clear input	100 K to V_{DD5x}	5-K

Note: All V_{DD3x} power supply pins must be tied together externally. Resistance between V_{DD3x} pins must not exceed 0.1 Ω DC / 2.5 Ω @ 20 MHz.

Figure 1-1: I/O Circuit



2. PROGRAMMING FLASH MEMORY

The device µPD76F0018 supports the programming of the internal flash in two ways: Either by using the *flash*MASTER programming tool or by performing self-programming using software functions and I/O communications.
For programming details about both methods, see the User’s Manual. For timing characteristics about the initial programming using *flash*MASTER and some more electrical data about the Flash Memory, see Chapter: “FLASH EPROM Characteristics” on page 32.

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

(T_A = 25°C, V_{SS3x} = 0 V)

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage	V_{DD5x}			-0.5 ~ +6.0	V
	AV_{DD}			-0.5 ~ +6.0	V
	AV_{SS}			-0.5 ~ +0.5	V
	A_{SS5x}			-0.5 ~ +0.5	V
Input voltage	(all except V_{PP}, X1, X2)	V_{I1}	$V_{I1} < V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	V
	V_{PP}	V_{I3}	V_{DD5x} = 4.5 V - 5.5 V	-0.5 ~ 8.5	V
Output current low	1 pin	I_{OL0}		4.0	mA
	All pins	I_{OL1}		50	mA
	group 1, 2**Note 1**	I_{OL2}		18	mA
	group 3, 4**Note 2**	I_{OL3}		36	mA
Output current high	1 pin	I_{OH0}		-4.0	mA
	All pins	I_{OH1}		-50	mA
	group 1, 2**Note 1**	I_{OH2}		-18	mA
	group 3, 4**Note 2**	I_{OH3}		-36	mA
Output voltage		V_O	$V_O < V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	V
Operating temperature		T_{OPR}		-40 ~ +85	°C
Operating temperature		T_{PRG}	during programming	0 ~ +70	°C
Storage temperature		T_{STGB}	Before program	-55 ~ +150	°C
		T_{STGA}	After program	-55 ~ +125	°C

Notes: 1. Group 1 pins: P1, P2, VCMPOUT, TXVAN0
Group 2 pins: P3, P4, P5

2. Group 3 pins: PAL, PAH
Group 4 pins: PCS, PCT, PCM, P6, TXVAN1

3.2 Operating Conditions

Table 3-2: Operating Conditions

Clock Mode	Operation Mode	Operating Temperature (T_A)	Supply Voltage (V_{DD5x})	Inside Operation Clock Frequency[Note 1]
Direct Mode[Note 2]	ALL Modes	-40 ~ +85°C	4.5 V ~ 5.5 V	4 MHz $\leq f_{CPU} \leq$ 20 MHz
OSC Mode, PLL on[Note 3]				16 MHz $\leq f_{CPU} \leq$ 20 MHz
OSC Mode, PLL off [Note 4]				4 MHz $\leq f_{CPU} \leq$ 5 MHz

Notes: 1. f_{CPU} = CPU operating frequency, as output (if enabled) on the CLOCKOUT pin.

2. See “External Clock in Direct mode” on page 18 for clock mode definition.
The inside clock frequency is half of the applied external frequency.

3. See “Crystal or Ceramic Resonator connection in OSC mode (T_A = -40 ~ +85°C)” on page 18 for clock mode definition.
The inside clock frequency is the quartz frequency, multiplied by 4.

4. See “Crystal or Ceramic Resonator connection in OSC mode (T_A = -40 ~ +85°C)” on page 18 for clock mode definition.
The inside clock frequency is the quartz frequency.
The PLL must be set permanently off by clearing the PLLEN flag.

3.3 General Characteristics

3.3.1 Oscillator Characteristics

Table 3-3: Oscillator Characteristics

(T_A= -40 ~ +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE		10		ms

3.3.2 PLL Characteristics

Table 3-4: PLL Characteristics

(T_A= -40 ~ +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL lock time	T_{PLL}	OSC MODE			1	ms

3.3.3 I/O Capacitances

Table 3-5: I/O Capacitances

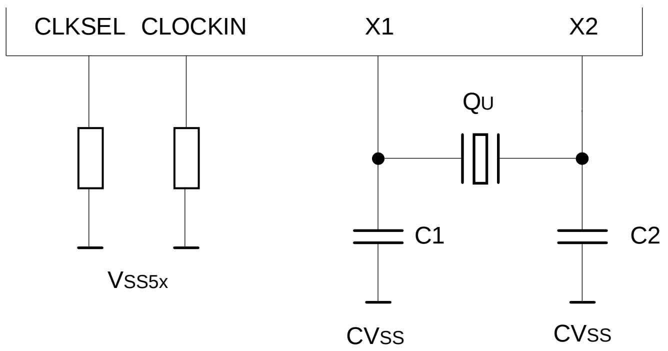
(T_A = 25°C, V_{DD5x} = V_{SS5x} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

3.4 Oscillator Recommendations

(a) Crystal or Ceramic Resonator connection in OSC mode (T_A = -40 ~ +85°C)

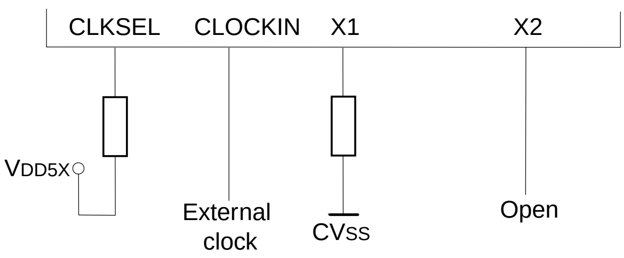
Figure 3-1: Crystal or Resonator connection in OSC mode



Remark: Values of capacitors depend on used resonator,
must be specified in cooperation with resonator manufacturer

(b) External Clock in Direct mode

Figure 3-2: External Clock in Direct Mode



Remarks: 1. CLKSEL Termination Resistor value: 1 K to 10 K to V_{DD5}

2. X1 Termination Resistor value: 1 K to 10 K to V_{SS5x}

3.5 DC Characteristics

Table 3-6: DC Characteristics

(T_A = -40 ~ +85°C, V_{DD5x} = 4.5 V ~ 5.5 V , V_{SS5x} = 0 V)

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	all except: P20,P22,X1 ,X2,PAH, RXVAN-pins[Note1]	V_{IH1}		0.8 V_{DD5x}		V_{DD5x}	V
Input voltage low		V_{IL1}		0		0.2 V_{DD5x}	V
Input voltage high	PAH, RXVAN-pins[Note1]	V_{IH2}		0.7 V_{DD5x}		V_{DD5x}	V
Input voltage low		V_{IL2}		0		0.3 V_{DD5x}	V
Input voltage high	P20,22	V_{IHT}		2.2		V_{DD5x}	V
Input voltage low	P20,22	V_{ILT}		0		0.8	V
Output voltage high		V_{OH0}	I_{OH0} = -3.0 mA	V_{DD5x} -1.0 V			V
Output voltage low	all except: TXVAN0 - 1	V_{OL0}	I_{OL0} = 3.0 mA			0.4	V
	TXVAN0 - 1	V_{OL4}	I_{OL4} = 3.2 mA **Note 2**			0.4	V
Input leakage current, high		I_{LIH}	$V_I = V_{DD5}$			5	μA
Input leakage current, low		I_{LIL}	V_I = 0			-5	μA

Notes: 1. RXVAN-pins: RX0VAN0, RX1VAN0, RX2VAN0, RX0VAN1, RX1VAN1, RX2VAN1

2. Under this test condition, current is limited to 1.5mA for the following pins:
P1, P2, VCMPOUT

Table 3-7: Power Supply Currents

(T_A = -40 ~ +85°C, V_{DD5x} = 4.5 V ~ 5.5 V , V_{SS5x} = 0 V)

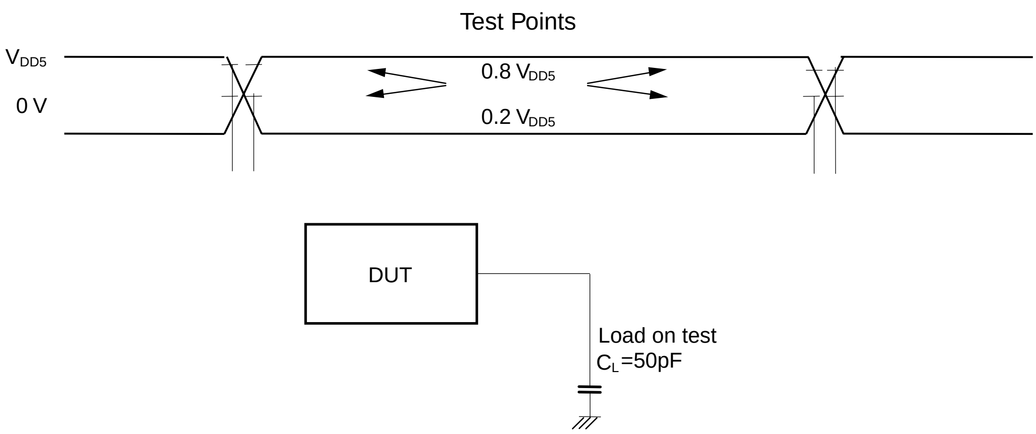
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current	I_{DD1D}	Operating (f_{cpu} = 20 MHz) Direct Mode		65	130	mA
	I_{DD1P}	Operating (f_{cpu} = 20 MHz) OSC Mode x 4		65	130	mA
	I_{DD1D1}	Operating (f_{cpu} = 16 MHz) Direct Mode		53	110	mA
	I_{DD1P1}	Operating (f_{cpu} = 16 MHz) OSC Mode x 4		53	110	mA
	I_{DD1P2}	Operating (f_{cpu} = 4 MHz) OSC Mode x 1		14	30	mA
	I_{DD2D}	HALT (f_{cpu} = 20 MHz) Direct Mode		50	100	mA
	I_{DD2P}	HALT (f_{cpu} = 20 MHz) OSC Mode x 4		50	100	mA
	I_{DD2D1}	HALT (f_{cpu} =16 MHz) Direct Mode		42	85	mA
	I_{DD2P1}	HALT (f_{cpu} = 16 MHz) OSC Mode x 4		42	85	mA
	I_{DD2P2}	HALT (f_{cpu} = 4 MHz) OSC Mode x 1		11	22	mA
	I_{DD3D}	IDLE (f_{cpu} = 20 MHz) Direct Mode		6.5	15	mA
	I_{DD3P}	IDLE (f_{cpu} = 20 MHz) OSC Mode x 4		6.5	15	mA
	I_{DD3D1}	IDLE (f_{cpu} = 16 MHz) Direct Mode		6	14	mA
	I_{DD3P1}	IDLE (f_{cpu} = 16 MHz) OSC Mode x 4		6	14	mA
	I_{DD3P2}	IDLE (f_{cpu} = 4 MHz) OSC Mode x 1		3	8	mA
	I_{DD4D}	WATCH (f_{cpu} = 5 MHz) Direct Mode		0.8	3.2	mA
	I_{DD4P}	WATCH (f_{cpu} = 5 MHz) OSC Mode x 1		0.8	3.2	mA
	I_{DD4P1}	WATCH (f_{cpu} = 4 MHz) OSC Mode x 1		0.6	3.0	mA

3.6 AC Characteristics

3.6.1 General

(T_A = -40 ~ +85°C, V_{DD5x} = 4.5 V ~ 5.5 V, V_{SS5x} = 0 V, Output pin load capacitance: C_L= 50 pF)

Figure 3-3: AC Test Input/Output Waveform, AC Test Load Condition

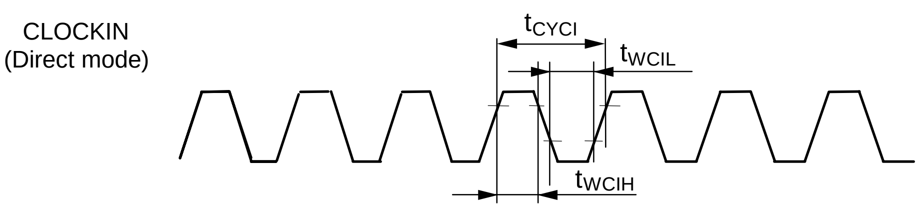


3.6.2 Clock

Table 3-8: Clock AC Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
CLOCKIN input cycle	t_{CYCI}	Direct Mode	25	125	ns
CLOCKIN input high-level width	t_{WCIH}	Direct Mode	12		ns
CLOCKIN input low-level width	t_{WCIL}	Direct Mode	12		ns

Figure 3-4: Clock AC Characteristics



3.6.3 External Memory Access Read Timing

Table 3-9: External Memory Access Read Timing

Parameter		Symbol	MIN.	MAX.	Unit
Data input set up time (vs.address)	<10>	T_{SAID}		$(2+w+w_D+w_{AS})T - 70$	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}		$(1.5+w+w_D)T - 60$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDL}	$(1.5+w+w_D)T - 15$		ns
$\overline{RD}$ High level width	<13>	T_{WRDH}	$(0.5+w_{AS}+i)T - 23$		ns
Address, $\overline{CSn} \rightarrow \overline{RD}\downarrow$ delay time	<14>	T_{DARD}	$(0.5+w_{AS})T - 25$		ns
$\overline{RD}\uparrow \rightarrow$ address delay time	<15>	T_{DRDA}	iT		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDID}	0		ns
$\overline{RD}\uparrow \rightarrow$ data output delay time	<17>	T_{DRDOD}	$(0.5+i)T$		ns
$\overline{WAIT}$ set up time (vs.address)	<31>	T_{SAW}		$(1+w_{AS}+ w_D)T - 70$	ns
$\overline{WAIT}$ high level width	<32>	T_{WWH}	T		ns

Remarks: 1. T : $1/f_{CPU}$ (= frequency of CLKOUT)

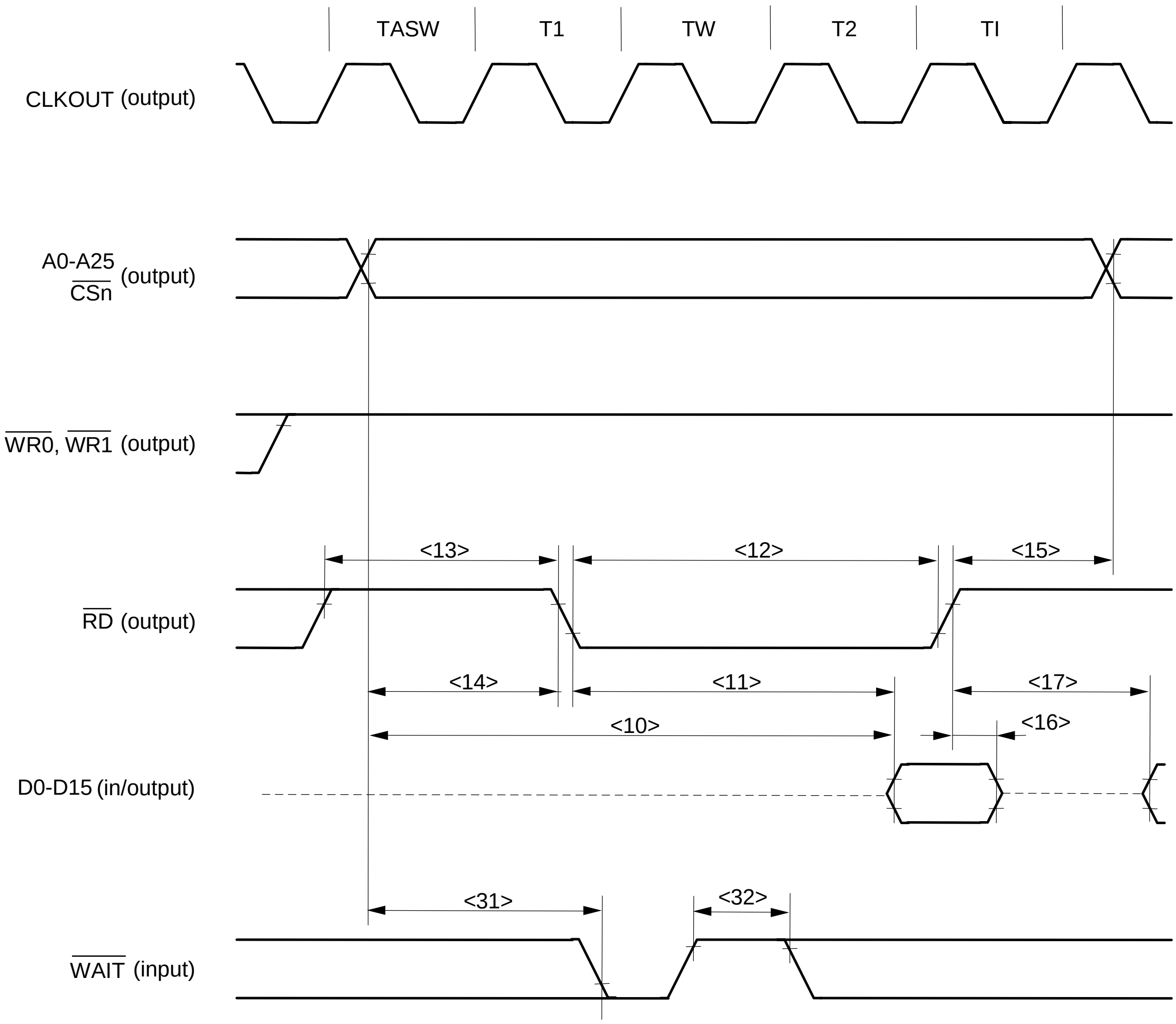
2. i : Number of idle states specified by BCC register

3. w_{AS}: Number of waits specified by ASC register

4. w_D: Number of waits specified by DWC1, DWC2 register; $W_D \geq 1$

5. w : Number of waits due to $\overline{WAIT}$

Figure 3-5: External Memory Access Read Timing



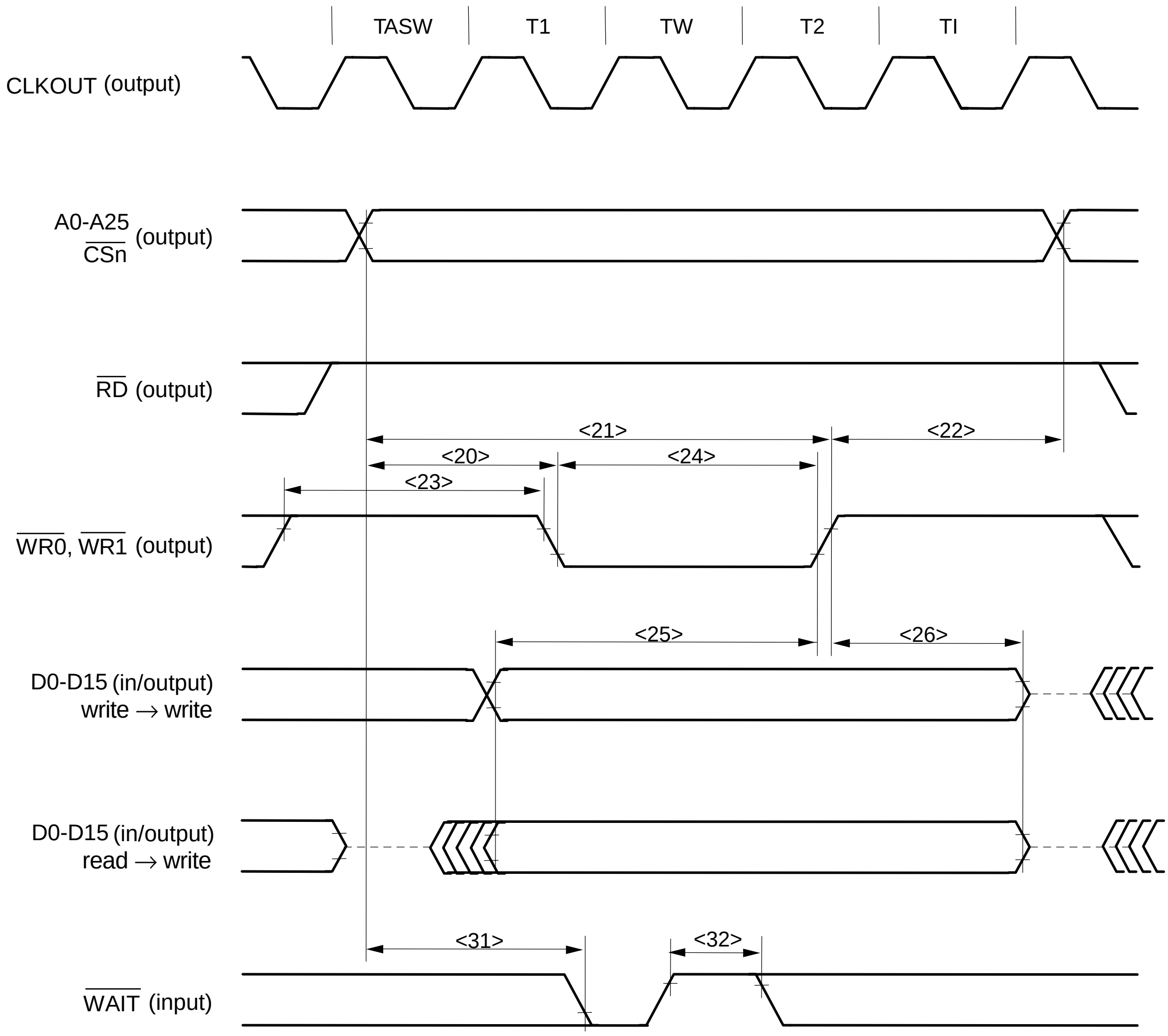
3.6.4 External Memory Access Write Timing

Table 3-10: External Memory Access Write Timing

Parameter		Symbol	MIN.	MAX.	Unit
Address, $\overline{CSn}$ → $\overline{WR0}$, $\overline{WR1}$↓ delay time	<20>	T_{DAWR}	$(0.5+w_{AS})T - 20$		ns
Address set up (vs. $\overline{WR0}$, $\overline{WR1}$↑)	<21>	T_{SAWR}	$(1.5+w+w_D+ w_{AS})T -25$		ns
$\overline{WR0}$, $\overline{WR1}$↑ → address delay time	<22>	T_{DWRA}	$(0.5+i)T - 15$		ns
$\overline{WR0}$, $\overline{WR1}$ High level width	<23>	T_{WWRH}	$(0.5+i+w_{AS})T - 15$		ns
$\overline{WR0}$, $\overline{WR1}$ Low level width	<24>	T_{WWRL}	$(1+w+w_D)T - 20$		ns
Data output set up time (vs. $\overline{WR0}$, $\overline{WR1}$↑)	<25>	T_{SODWR}	$(0.5+w+w_D+ w_{AS})T -25$		ns
Data output hold time (vs. $\overline{WR0}$, $\overline{WR1}$↑)	<26>	T_{HWROD}	$(0.5+i)T - 15$		ns
$\overline{WAIT}$ set up time (vs.address)	<31>	T_{SAW}		$(1+w_{AS}+ w_D)T - 70$	ns
$\overline{WAIT}$ High level width	<32>	T_{WWH}	T		ns

Remarks:
1. T : $1/f_{CPU}$ (= frequency of CLKOUT)
2. i : Number of idle states specified by BCC register
3. w_{AS}: Number of waits specified by ASC register
4. w_D: Number of waits specified by DWC1, DWC2 register; $W_D \geq 1$
5. w : Number of waits due to $\overline{WAIT}$

Figure 3-6: External Memory Access Write Timing



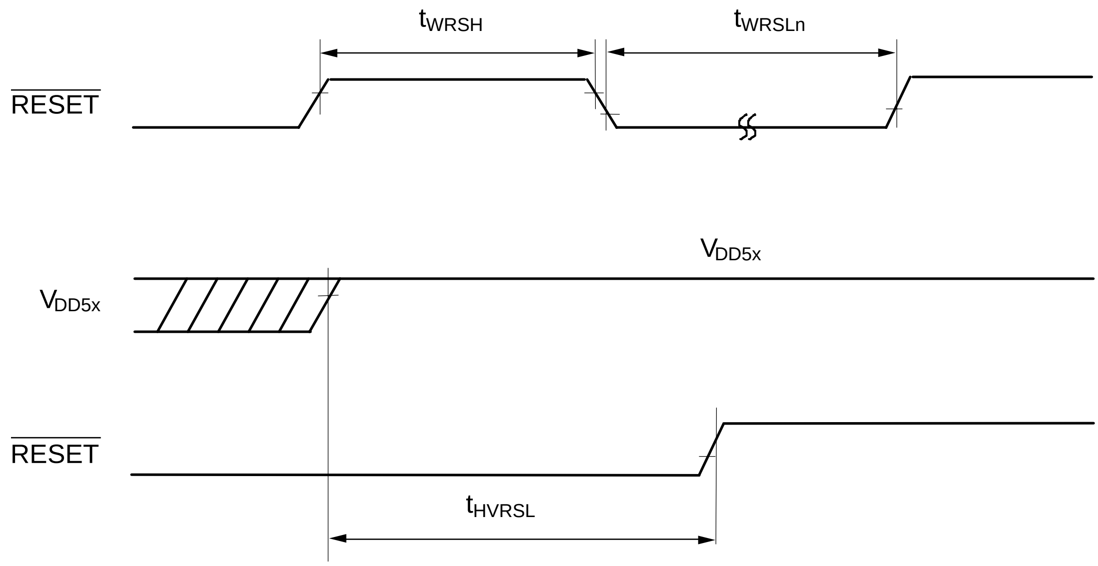
3.6.5 Reset

Table 3-11: Reset Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL0}	STOP Mode release, OSC mode	T_{OST} Note		ms
	t_{WRSL1}	STOP Mode release, Direct mode	1.5		ms
	t_{WRSL2}	except STOP Mode release	1.5		ms
$\overline{\text{RESET}}$ hold time (from V_{DD5x})	t_{HVRSL0}	OSC Mode on power-on	T_{OST}		ms
	t_{HVRSL1}	Direct mode on power-on	1.5		ms

Note: T_{OST}: Oscillation stabilization time

Figure 3-7: Reset Timing



Remark: n = 0 to 2

3.6.6 Interrupt Timing

Table 3-12: Interrupt Timing

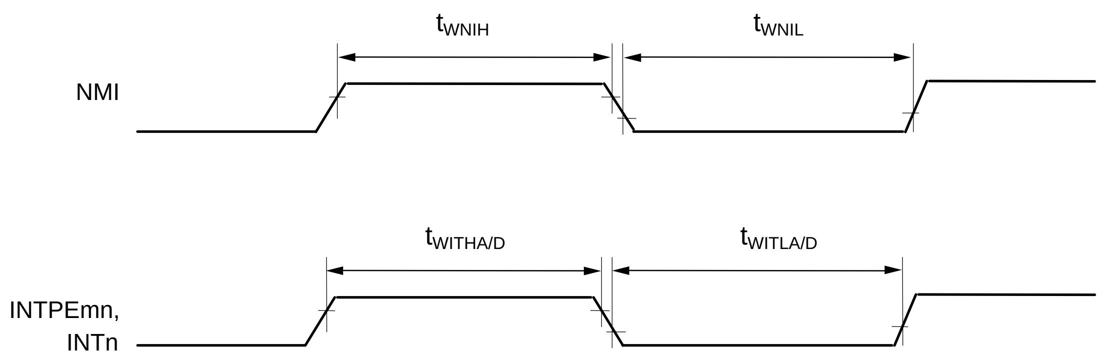
Parameter[Note 1]	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI high-level width	t_{WNIH}		500[Note 2]		ns
NMI low-level width	t_{WNIL}		500[Note 2]		ns
INTPEmn, INTn [Note 1] high-level width	t_{WITHA}	Analog filter	500[Note 2]		ns
IINTPEmn, INTn[Note 1] low-level width	t_{WITLA}	Analog filter	500[Note 2]		ns
INTPEmn, INTn[Note 1] high-level width	t_{WITHD}	Digital filter	$5T_{sam}+10$[Note 3]		ns
INTPEmn, INTn[Note 1] low-level width	t_{WITLD}	Digital filter	$5T_{sam}+10$[Note 3]		ns

Notes: 1. m = 0 ~ 5, n = 0 ~ 2

2. Design constraint is 100 ns

3. $T_{SAM} = 1/f_{SAM}$ (f_{SAM} is set by register setting in filter. $f_{SAM} = f_{CPU}$ or $f_{CPU}/2$ or $f_{CPU}/16$)

Figure 3-8: Interrupt Timing



3.7 Peripheral Function Characteristics

3.7.1 Timer E

Table 3-13: Timer E Characteristics

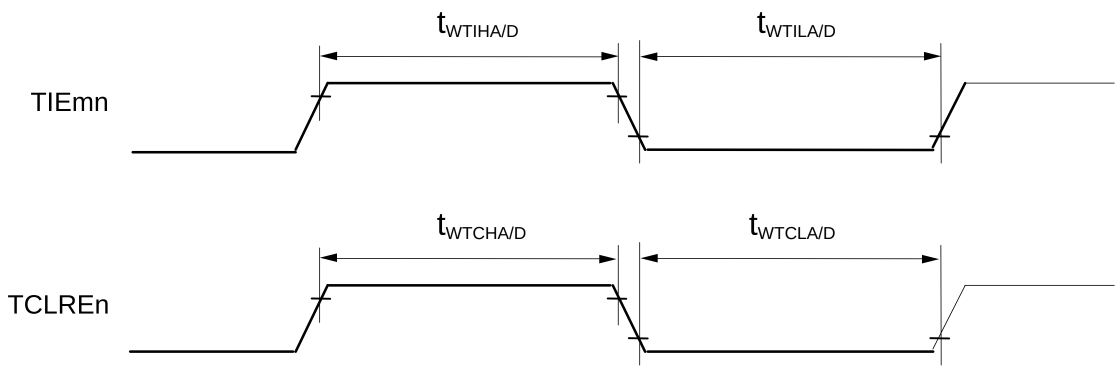
Parameter Note 1	Symbol	Test Conditions	MIN.	MAX.	Unit
TIEmn high-level width**Note 1**	t_{WTIHA}	no filter	T **Note 2** + 10		ns
TIEmn low-level width**Note 1**	t_{WTILA}	no filter	T **Note 2** + 10		ns
TCLREn high-level width	t_{WTCHA}	no filter	T **Note 2** + 10		ns
TCLREn low-level width	t_{WTCLA}	no filter	T **Note 2** + 10		ns
TIEmn high-level width**Note 1**	t_{WTIHD}	Digital filter	$5T_{sam}$**Note 3** + 10		ns
TIEmn low-level width**Note 1**	t_{WTILD}	Digital filter	$5T_{sam}$**Note 3** + 10		ns
TCLREn high-level width	t_{WTCHD}	Digital filter	$5T_{sam}$**Note 3** + 10		ns
TCLREn low-level width	t_{WTCLD}	Digital filter	$5T_{sam}$**Note 3** + 10		ns

Notes: 1. m = 0 - 5, n = 0 - 2

2. $T = 1/f_{CPU}$

3. $T_{SAM} = 1/f_{SAM}$ (f_{SAM} is set by register setting in filter. $f_{SAM} = f_{CPU}$ or $f_{CPU}/2$ or $f_{CPU}/16$)

Figure 3-9: Timer E Characteristics



3.7.2 CSI

I

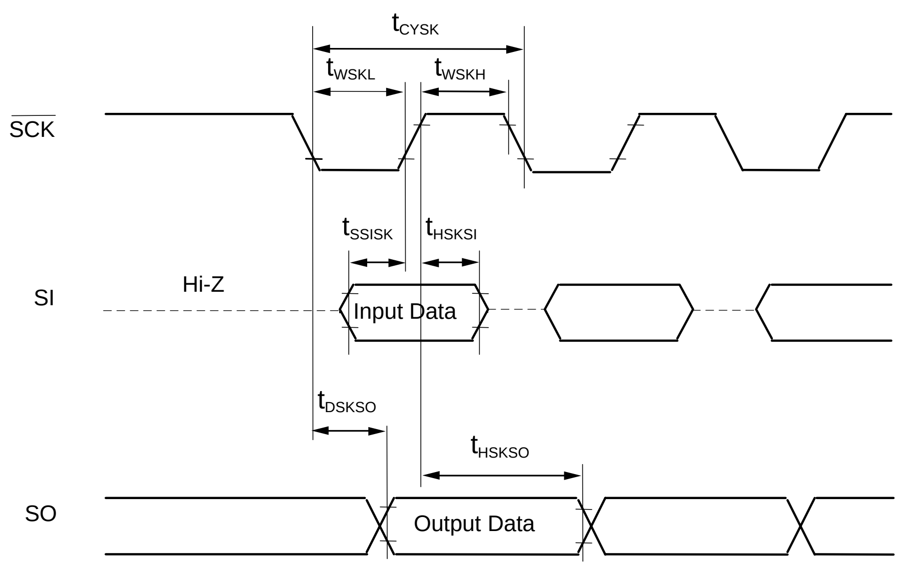
Table 3-14: CSI Master Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{CYSK}	Output	200		ns
$\overline{\text{SCK}}$ high level width	t_{WSKH}	Output	0.5 t_{CYSK}-15		ns
$\overline{\text{SCK}}$ low level width	t_{WSKL}	Output	0.5 t_{CYSK}-15		ns
SI set up time (to $\overline{\text{SCK}}$ ↑)	t_{SSISK}		45		ns
SI hold time (from $\overline{\text{SCK}}$ ↑)	t_{HSKSI}		45		ns
SO output delay time (from $\overline{\text{SCK}}$ ↓)	t_{DSKSO}			30	ns
SO output hold time (from $\overline{\text{SCK}}$ ↑)	t_{HSKSO}		0.5 t_{CYSK}-5		ns

Table 3-15: CSI Slave Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{CYSK}	Input	200		ns
$\overline{\text{SCK}}$ high level width	t_{WSKH}	Input	90		ns
$\overline{\text{SCK}}$ low level width	t_{WSKL}	Input	90		ns
SI set up time (to $\overline{\text{SCK}}$ ↑)	t_{SSISK}		50		ns
SI hold time (from $\overline{\text{SCK}}$ ↑)	t_{HSKSI}		50		ns
SO output delay time (from $\overline{\text{SCK}}$ ↓)	t_{DSKSO}			50	ns
SO output hold time (from $\overline{\text{SCK}}$ ↑)	t_{HSKSO}		t_{WSKH}		ns

Figure 3-10: CSI Slave Mode Characteristics



3.7.3 UART

Table 3-16: UART Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UART}	$f_{CPU} \geq 5$ MHz		312500	bps

3.7.4 FVAN

Table 3-17: FVAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FVAN}	$f_{CPU} \geq 16$ MHz		1	Mbps

3.7.5 FCAN

Table 3-18: FCAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	$f_{CPU} \geq 16$ MHz		1	Mbps

3.7.6 A/D Converter

Table 3-19: A/D Converter Characteristics

(T_A = -40 ~ +85°C, V_{DD5x} = 4.5 ~ 5.5 V, AV_{DD} = V_{DD5x})

Parameter	Symbol	Test Cond.	MIN.	TYP.	MAX.	Unit
Resolution	-			10		Bit
Overall Error **Note 1**	-	$AV_{REF} = AV_{DD}$		±3	±6	LSB
Conversion Time **Note 2**	t_{CONV}		5			μs
Sampling Time **Note 3**	t_{SAM}		0.9			μs
Analogue Input Voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference Voltage	AV_{REF}		AV_{SS}		AV_{DD}	V
Reference Voltage Input Current **Note 4**	I_{AVREF}	$AV_{REF} = AV_{DD}$		1	2	mA

Notes: 1. Quantization error is not included

2. t_{CONV} depends on register ADSCM1

3. t_{SAM} depends on register ADSCM1

4. If ADC is set to standby mode, AV_{REF} can be disconnected externally (left open) to reduce current consumption

3.7.7 Voltage Comparator Characteristics

Table 3-20: Voltage Comparator Characteristics

(T_A = -40 ~ +85°C, V_{DD5x} = 4.5 V ~ 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Comparator Analog Input voltage	V_{CIN}		0		V_{DD5x}	V
Threshold voltage	V_{TH}	V_{DD5x} = 4.5 ~ 5.5 V	1.1	1.25	1.4	V

3.8 FLASH EPROM Characteristics

Table 3-21: Flash EPROM Programming Characteristics Basic Specification

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	f_X		4		20	MHz
Supply voltage	V_{DD5x}		4.5		5.5	V
	V_{PPL}	Low input	-0.3		V_{DD5x}	V
	V_{PPH}	Programming mode	7.5	7.8	8.1	V
Maximum times of reprogramming	C_{WRT}				100	times
Write time	T_{IWRTW}	Word (32-bit) **Note 1**		50	200	µs
Write Back time / block	T_{WBACK}	**Note1**			10	s
Erase time	T_{ERASCB}	block (128 KByte)**Note 1**		2	30	s
	T_{ERASCC}	chip (256 KByte)**Note 1**		20	60	s
Programming temperature	T_{PRG}		0		+70	°C
Erase / Write current	$I_{PPE/W}$	V_{PPH} = TYP.**Note 2**			100	mA

Notes: 1. Exclusive recovery time, firmware execution and verify

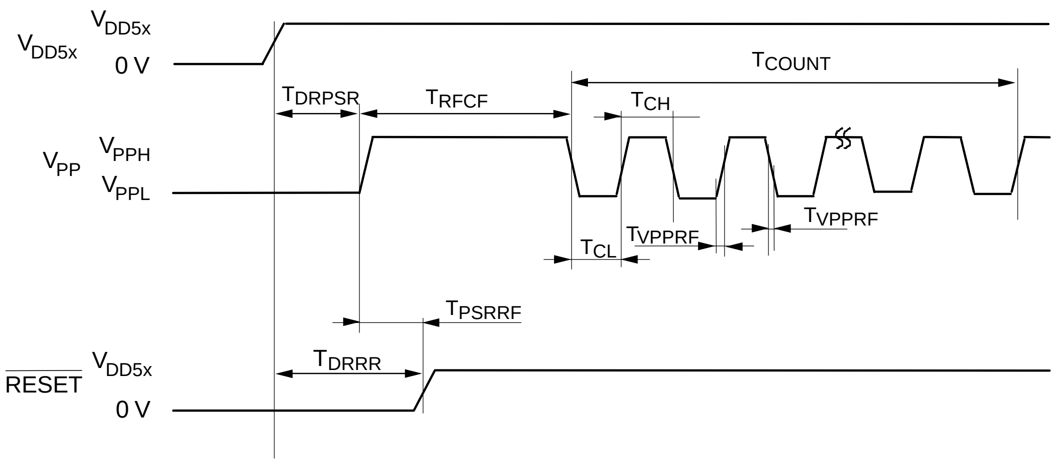
2. Measured condition after TPE (erase-time) = 100 mS

Table 3-22: Flash EPROM Serial Programming Operation Characteristics

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
V_{DD}↑ setup time (to $\overline{RESET}$↑)	T_{DRRR}		10			ms
V_{DD}↑ setup time (to V_{PP}↑)	T_{DRPSR}		10			µs
V_{PP}↑ set time (to $\overline{RESET}$↑)	T_{PSRRF}		1.0			µs
Count start setup time from V_{PP}↑	T_{RFCF}		5T **Note** + 500			µs
Times of V_{PP} counting	T_{COUNT}				10	ms
V_{PP} count Hi/Low level width	T_{CH},T_{CL}		1.0			µs
V_{PP} count rise/fall time	T_{VPPRF}				0.2	ms

Note: $T = 1/f_{CPU}$

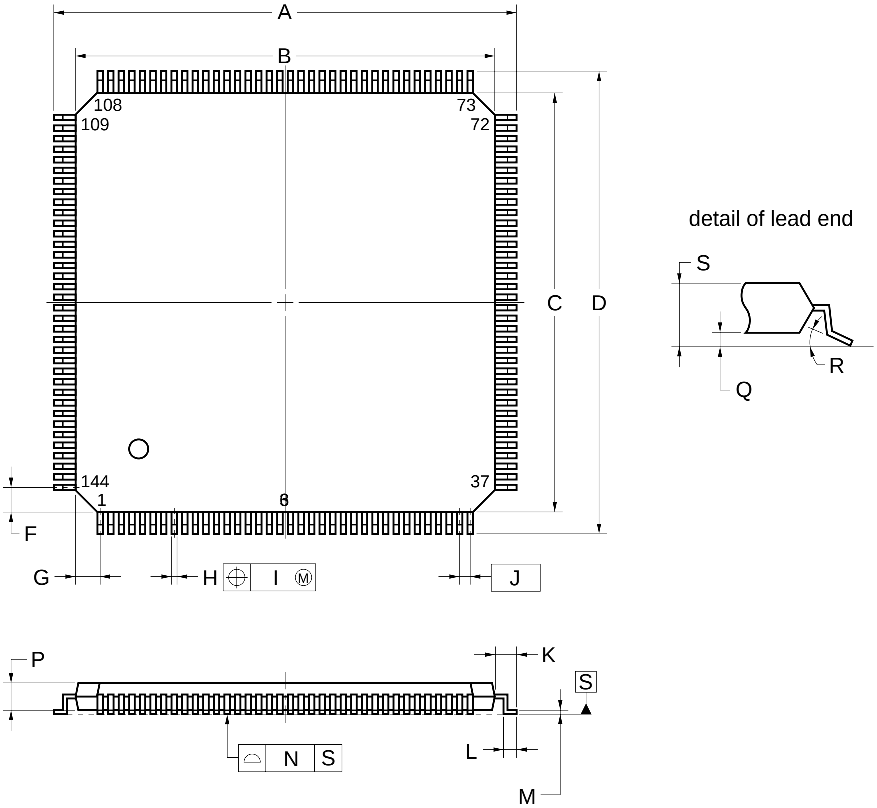
Figure 3-11: Flash EPROM Programming Timing



4. PACKAGE DRAWING

Figure 4-1: Package Drawing

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{?0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3°^{+4°}_{?3°}$
S	1.5±0.1

S144GJ-50-UEN

5. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:

Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended, consult NEC.

Table 5-1: Soldering Conditions

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 3 Note 1	IR30-103-2
VPS	Package peak temperature: 215°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 3 Note 1	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	-

Notes: 1. After that, prebaking is necessary at 125°C for 10 hours.

2. The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution: Do not use two or more soldering methods in combination (except partial heating method).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

6. REVISION HISTORY

Version	Date (xx.xx.2002)	Author	Remarks
0.1	25.05.2000	E. Gebing	1st Preparation PPI
1.0	23.05.2001	E. Gebing	Preliminary Data Sheet
2.0	14.01.2002	E.Gebing	Data Sheet
2.1	23.01.2002	E.Gebing	Data Sheet

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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