

Application Specific Discretes $A.S.D.^{TM}$

TRANSIL[™] ARRAY FOR ESD PROTECTION

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- COMPUTER
- PRINTERS
- COMMUNICATION SYSTEMS

It is particulary recommended for RS232 I/O port protection where the line interface withstands only 2 kV ESD surges.

FEATURES

- 6 BIDIRECTIONAL TRANSILTM FUNCTIONS
- VERY LOW CAPACITANCE : C= 20 pF @ V_{RM}
- 150 W peak pulse power (8/20 μs)

DESCRIPTION

The ESDA25B1 is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against EDS.

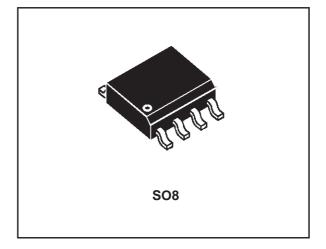
BENEFITS

High ESD protection level : up to 25 kV High integration Suitable for high density boards

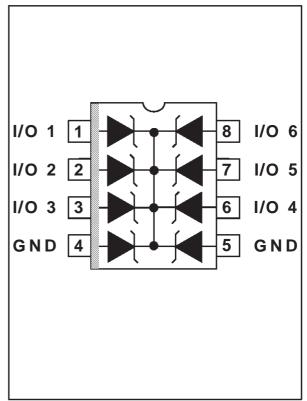
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 1000-4-2: level 4

MIL STD 883C-Method 3015-6 : class 3 (human body model)



FUNCTIONAL DIAGRAM

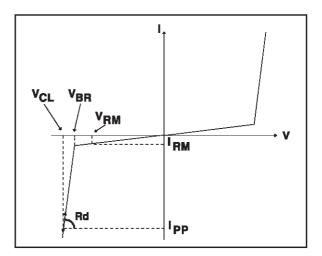


Symbol	Parameter	Value	Unit
Vpp	Electrostatic discharge MIL STD 883C - Method 3015-6	25	kV
P _{PP}	Peak pulse power (8/20µs)	150	W
T _{stg} Tj	Storage temperature range Maximum junction temperature	- 55 to + 150 125	°C ℃
TL	Maximum lead temperature for soldering during 10s	260	°C

ABSOLUTE MAXIMUM RATINGS (Tamb = 25°C)

ELECTRICAL CHARACTERISTICS (Tamb = 25°C)

Symbol	Parameter				
V _{RM}	Stand-off voltage				
Vbr	Breakdown voltage				
Vcl	Clamping voltage				
I _{RM}	Leakage current				
IPP	Peak pulse current				
ατ	Voltage temperature coefficient				
С	Capacitance				
Rd	Dynamic resistance				



Types	V _{BR} @		IR	I _{RM} @	Vrm	Rd	αΤ	С
	min. max.			max.		typ.	max.	typ.
	note 1			note 1		note 2	note 3	0V bias
	V	V	mA	μA	V	Ω	10 ⁻⁴ /°C	рF
ESDA25B1	25	30	1	2	24	1.5	9.7	15

note 1 : Between any I/O pin and Groung **note 2** : Square pulse, Ipp = 25A, tp=2.5 μ s. **note 3** : Δ V_{BR} = α T* (Tamb -25°C) * V_{BR} (25°C)



CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

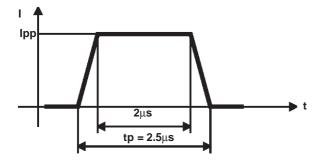
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL} . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

 $V_{CL} = V_{BR} + Rd I_{PP}$

Where lpp is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical $8/20\mu s$ and $10/1000\mu s$ surges.



2.5µs duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.



Fig. 1: Peak power dissipation versus initial junction temperature.

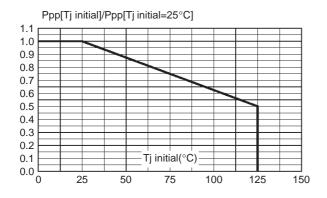


Fig. 3 : Clamping voltage versus peak pulse current (Tj initial = 25 °C). Rectangular waveform tp = $2.5 \,\mu$ s.

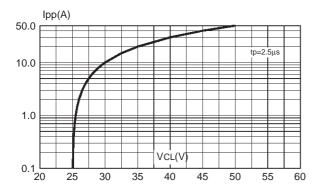


Fig. 5 : Relative variation of leakage current versus junction temperature (typical values).

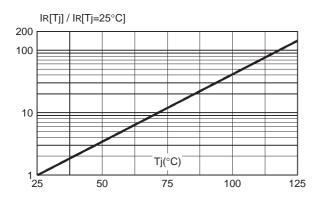


Fig. 2: Peak pulse power versus exponential pulse duration (Tj initial = 25 °C).

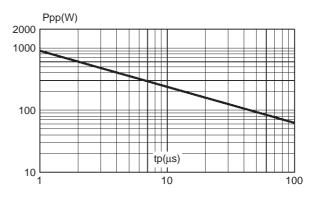
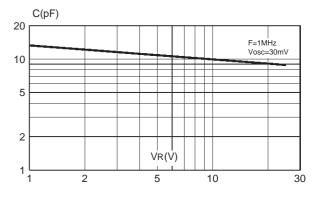
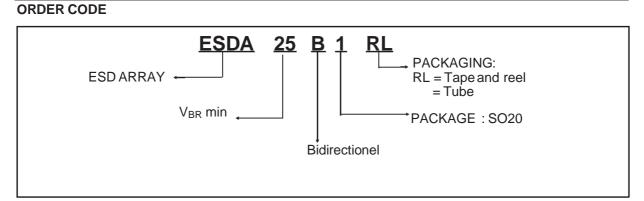


Fig. 4 : Capacitance versus reverse applied voltage (typical values).





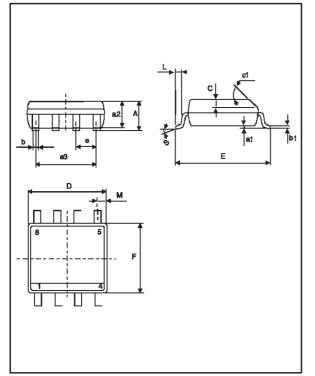
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PACKAGE MECHANICAL DATA

SO8 Plastic



	DIMENSIONS						
REF.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α			1.75			0.069	
a1	0.1		0.25	0.004		0.010	
a2			1.65			0.065	
a3	0.65		0.85	0.026		0.033	
b	0.35		0.48	0.014		0.019	
b1	0.19		0.25	0.007		0.010	
С	0.25		0.5	0.010		0.020	
c1	45°(typ)						
D	4.8		5.0	0.189		0.197	
E	5.8		6.2	0.228		0.244	
е		1.27			0.050		
e3		3.81			0.150		
F	3.8		4.0	0.15		0.157	
L	0.4		1.27	0.016		0.050	
М			0.6			0.024	
S	8° (max)						

Packaging : Preferred packaging is tape and reel. **Weight :** 0.08g.

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