PROCESS CP206

Small Signal Transistor

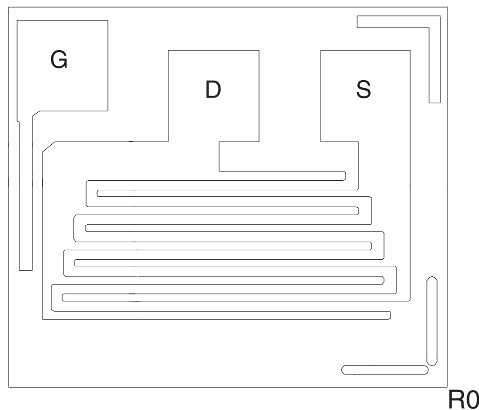
N - Channel Switch/Chopper J FET Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	21 x 18 MILS
Die Thickness	8.0 MILS
Drain Bonding Pad Area	3.8 X 3.8 MILS
Source Bonding Pad Area	3.8 X 3.8 MILS
Gate Bonding Pad Area	3.8 X 3.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 6,000Å

GEOMETRY



BACKSIDE GATE

GROSS DIE PER 4 INCH WAFER

30,950

PRINCIPAL DEVICE TYPES

2N4391
2N4392
2N4393
CMPF4391
CMPF4392
CMPF4393

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Typical Electrical Characteristics

The Typical Electrical Characteristics data
for this chip is currently being revised.

For the latest updated data for this Chip Process,
please visit our website at:

www.centralsemi.com/chip

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