PROCESS CP311

Power Transistor

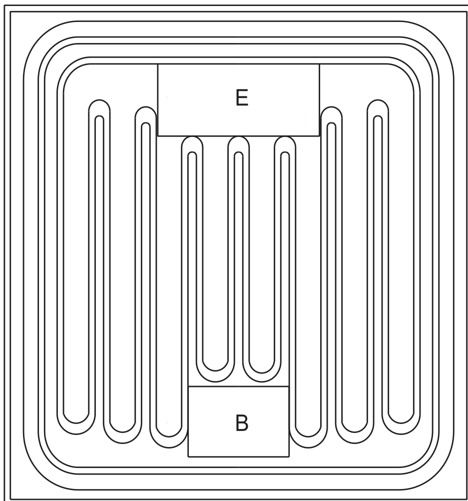
NPN High Voltage Transistor Chip

Central™ Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	109.5 x 109.5 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	23.6 x 15.4 MILS
Emitter Bonding Pad Area	37.8 x 15.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti / Ni / Ag - 11,300Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER

900

PRINCIPAL DEVICE TYPES

CJDD3110

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R1 (1-August 2002)

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Typical Electrical Characteristics

The Typical Electrical Characteristics data
for this chip is currently being revised.

For the latest updated data for this Chip Process,
please visit our website at:

www.centralsemi.com/chip

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