PROCESS CP566

Small Signal Transistor

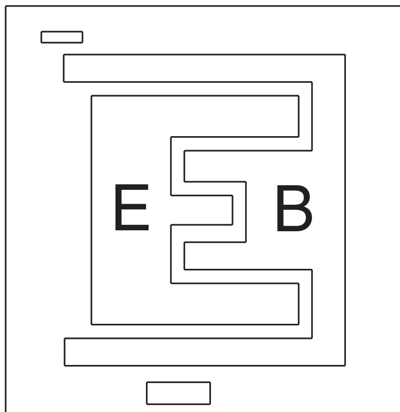
PNP - Silicon Chopper Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	31.5 x 31.5 MILS
Die Thickness	11 MILS
Base Bonding Pad Area	7.8 x 6.2 MILS
Emitter Bonding Pad Area	8.0 x 5.3 MILS
Top Side Metalization	Al - 12,000Å
Back Side Metalization	Au - 10,000Å

GEOMETRY



GROSS DIE PER 4 INCH WAFER
11,380

PRINCIPAL DEVICE TYPES
CMPT404A
MPS404A

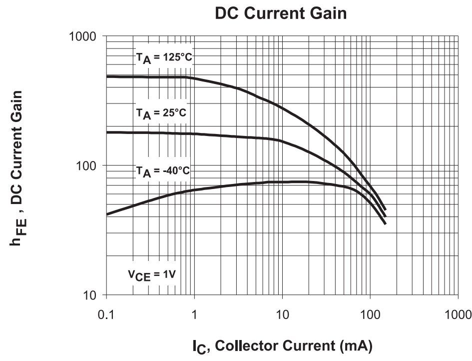
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

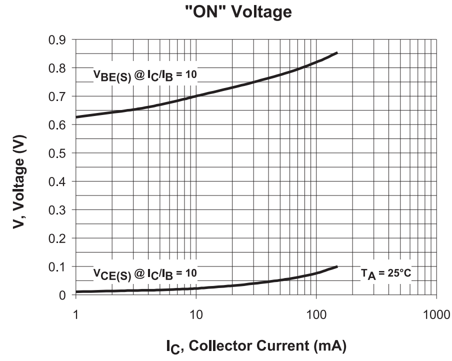
R2 (1-August 2002)

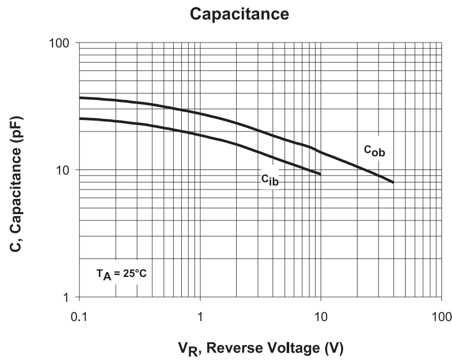
Central™ Semiconductor Corp.

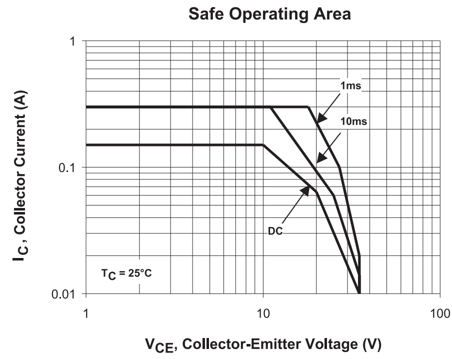
PROCESS CP566

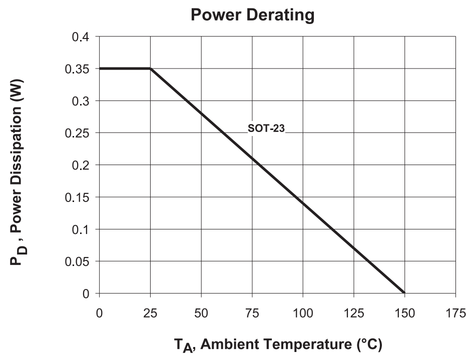
Typical Electrical Characteristics

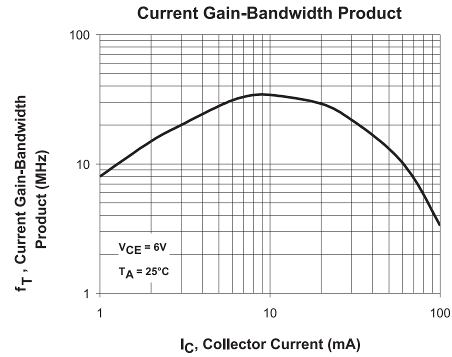












145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R2 (1-August 2002)