Central™ Semiconductor Corp.

PROCESS CP603

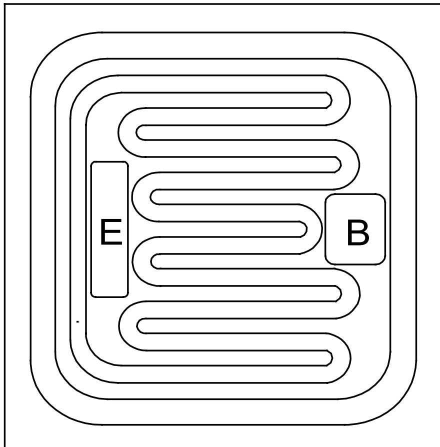
Small Signal Transistors

PNP - Saturated Switch Transistor Chip

PROCESS DETAILS

PROCESS	EPITAXIAL PLANAR
DIE SIZE	30 x 30 MILS
DIE THICKNESS	7.5 MILS
BASE BONDING PAD AREA	5.0 x 4.0 MILS
EMITTER BONDING PAD AREA	9.0 x 3.5 MILS
TOP SIDE METALIZATION	Al
BACK SIDE METALIZATION	Au - 15,000Å

GEOMETRY



BACKSIDE COLLECTOR

PRINCIPAL DEVICE TYPES

2N3467
2N3468

Please refer to selection guide on page 18.

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