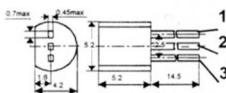


ML 406

Silicon controlled rectifier (SCR)
in TO-92 package



Pinouts:

1- Anode, 2- Gate, 3- Cathode

Maximum ratings

Symbol	Parameter, units	Limits
V_{dgm}	Peak repetitive forward voltage, V_f , $R_{ig}=1\text{k}\Omega$	400
V_{frm}	Repetitive peak reverse voltage, V	6
$I_{f(rms)}$	On-state current, A	All Conduction Angles
$I_{f(AV)}$	Average on-state current, A	Half Cycle, $\theta=180^\circ$
$I_{f(sm)}$	Nonrepetition on-state current, A	Half Cycle, 50Hz
V_{grm}	Peak reverse gate voltage, V	$I_g=0.01\text{mA}$
		6.0

Electrical characteristics ($T_A = 25^\circ\text{C}$)

Symbol	Parameter, units test conditions	Limits	
		min	max
I_{dgm}	Off state leakage current, μA , $@V_{grm}, R_{ig}=1\text{k}\Omega$		1
V_t	On state voltage, V, $I_f=1.2\text{A}$		1.93
I_{gt}	Gate trigger current, mA, $V_g=6\text{V}$		0.12
V_{gt}	Gate trigger voltage, V, $V_g=6\text{V}$		0.8
I_h	Holding current, mA, $R_{ig}=1\text{k}\Omega$		5
dV/dt	Crit. rate of voltage rise, $\text{V}/\mu\text{s}$, $V_g=0.67V_{dgm}, R_{ig}=1\text{k}\Omega$	25	
dl/dt	Crit. rate of current rise, $\text{A}/\mu\text{s}$, $I_g=10\text{mA}, dl_g/dt=0.1\text{A}/\mu\text{s}$	30	
t_{gd}	Gate control delay time, ns, $I_g=10\text{mA}, dl_g/dt=0.1\text{A}/\mu\text{s}$		200