

MOS FIELD EFFECT TRANSISTOR

NP24N06HLB, NP24N06ILB

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
 $R_{DS(on)1} = 70 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 12 \text{ A)}$
 $R_{DS(on)2} = 90 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5.0 \text{ V, } I_D = 5 \text{ A)}$
- Low C_{iss} : $C_{iss} = 860 \text{ pF TYP.}$
- Built-in gate protection diode

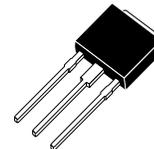
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP24N06HLB	TO-251
NP24N06ILB	TO-252

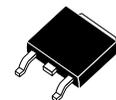
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 24	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 40	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.2	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	51	W
Single Avalanche Current ^{Note2}	I_{AS}	24 / 10 / 4	A
Single Avalanche Energy ^{Note2}	E_{AS}	5.7 / 10 / 80	mJ
Repetitive Avalanche Current ^{Note3}	I_{AR}	10	A
Repetitive Avalanche Energy ^{Note3}	E_{AR}	5.1	mJ
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$

(TO-251)



(TO-252)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$ (See Figure 4.)

3. $T_{ch} \leq 175^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, Duty cycle $\leq 3\%$

THERMAL RESISTANCE

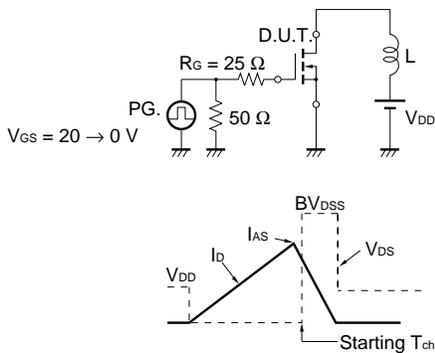
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.94	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

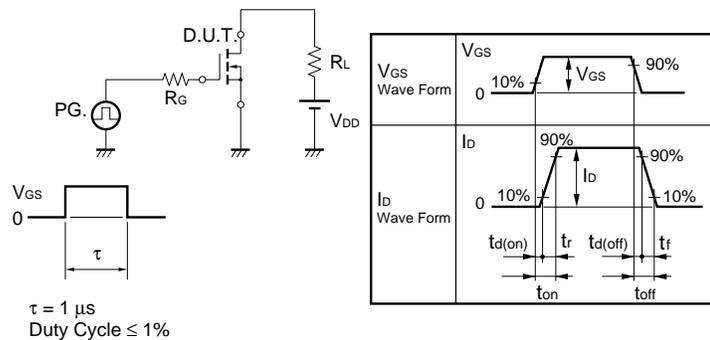
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 5 A	7	12		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 12 A		45	70	mΩ
	R _{DS(on)2}	V _{GS} = 5.0 V, I _D = 5 A		53	90	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 5 A		58	95	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		860	1900	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		440	700	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		110	200	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 5 A		15	40	ns
Rise Time	t _r	V _{GS} = 10 V		90	230	ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		75	150	ns
Fall Time	t _f			35	90	ns
Total Gate Charge	Q _G	V _{DD} = 48 V		24	36	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		2.6		nC
Gate to Drain Charge	Q _{GD}	I _D = 10 A		6.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		85		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		220		nC

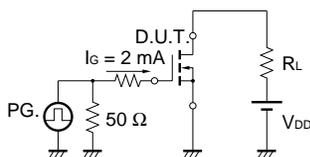
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



★ TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

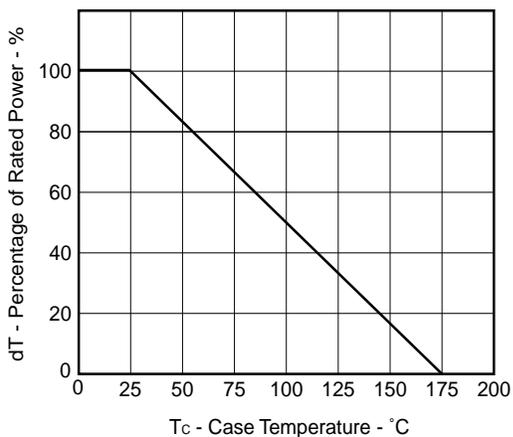


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

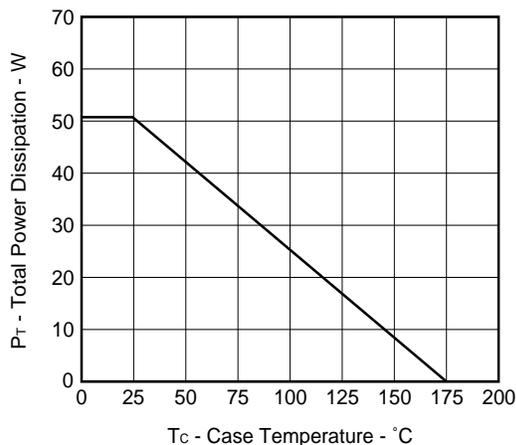


Figure3. FORWARD BIAS SAFE OPERATING AREA

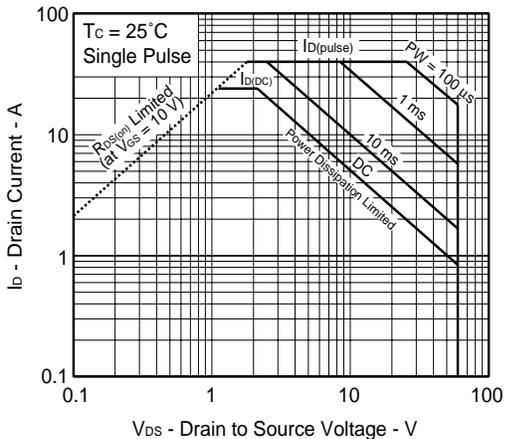


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

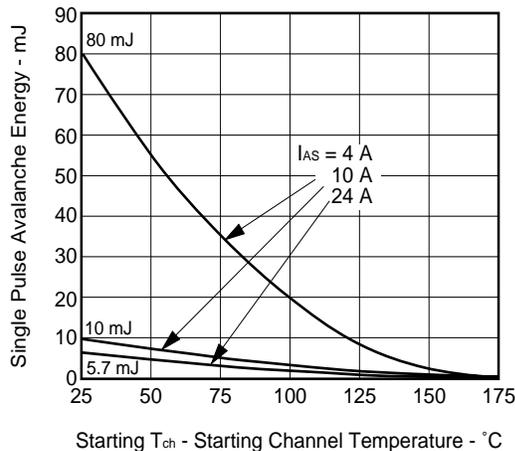


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

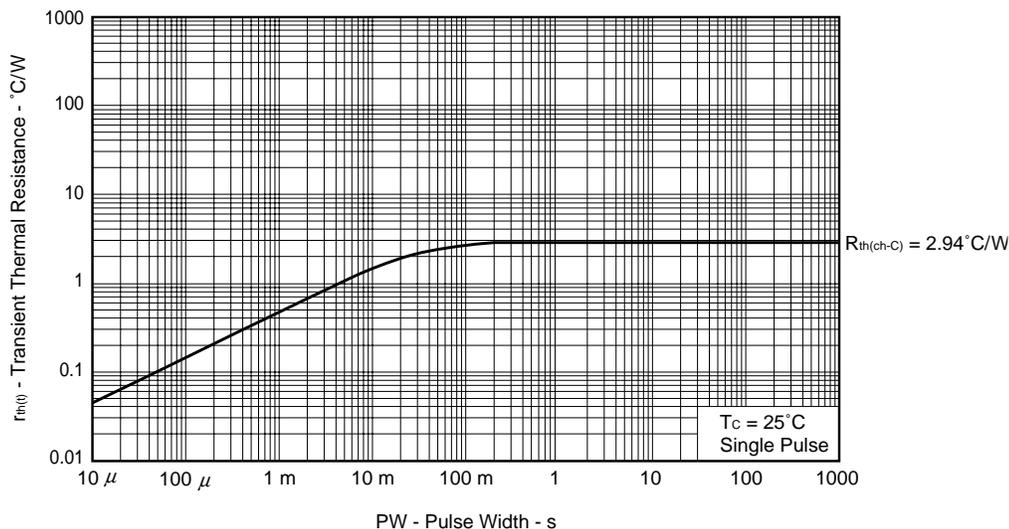


Figure6. FORWARD TRANSFER CHARACTERISTICS

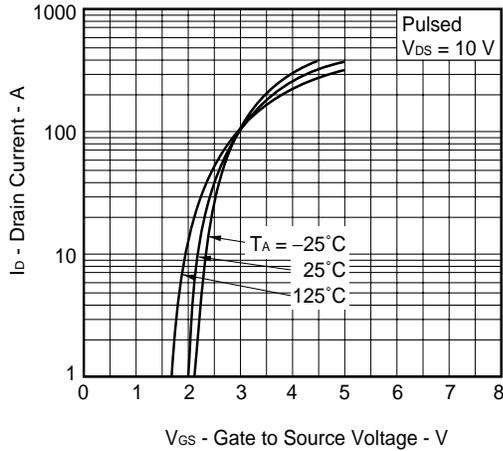


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

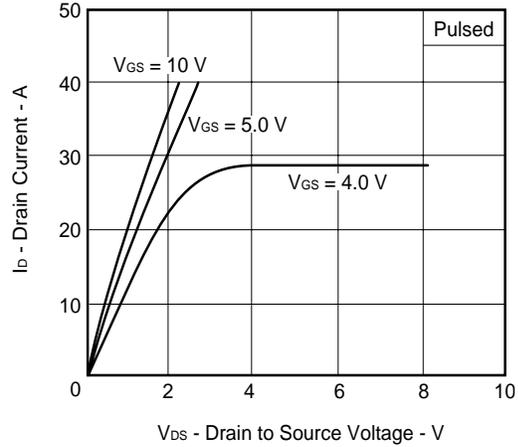


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

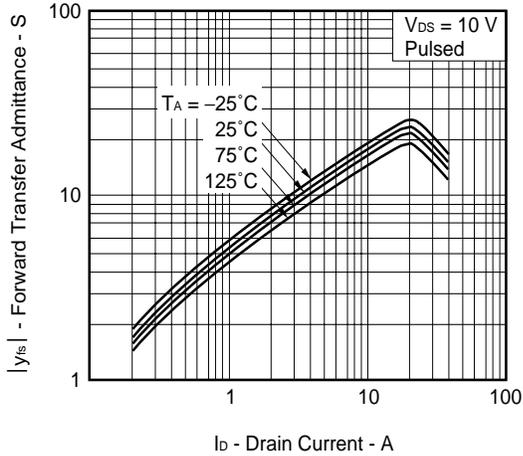


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

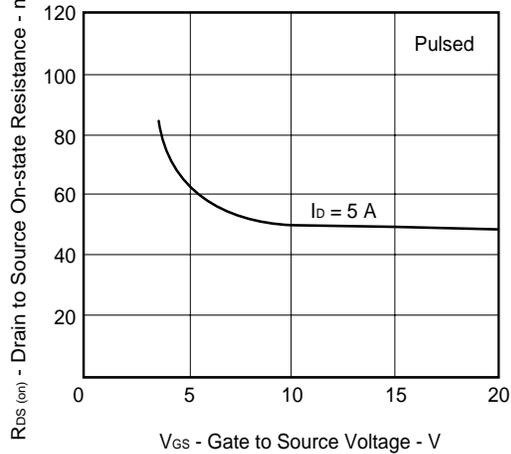


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

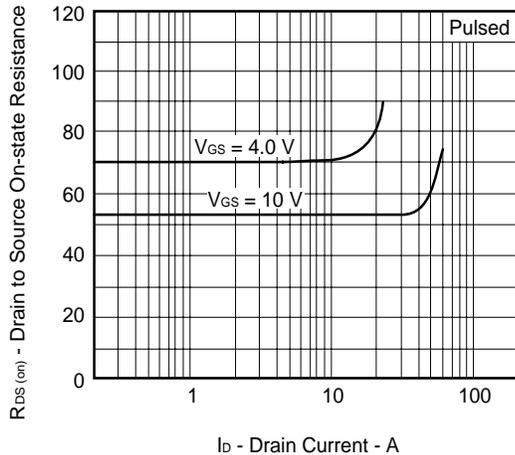


Figure11. GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

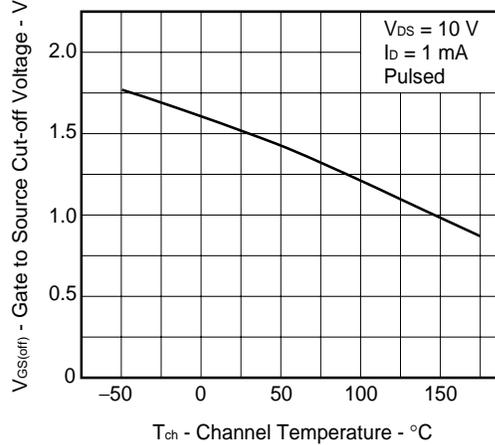


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

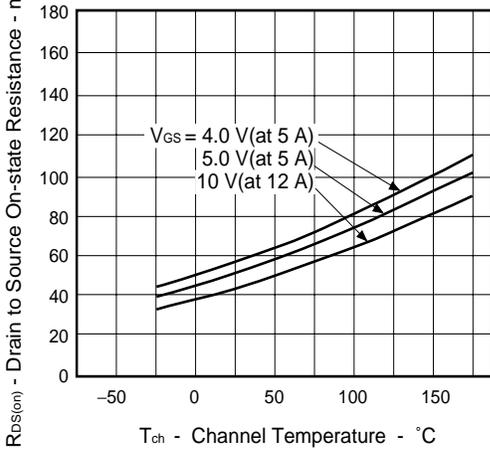


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

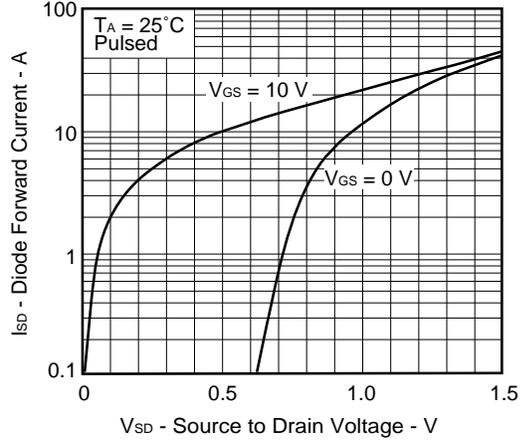


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

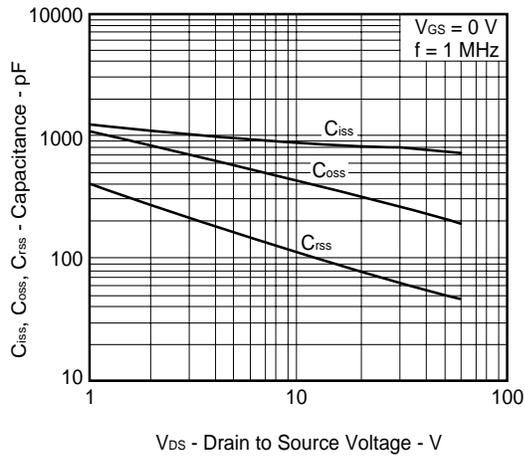


Figure15. SWITCHING CHARACTERISTICS

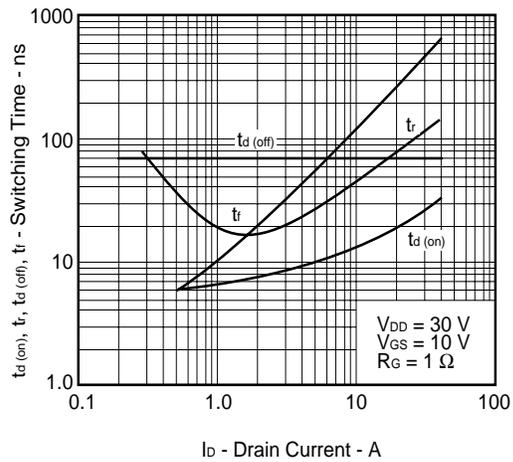


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

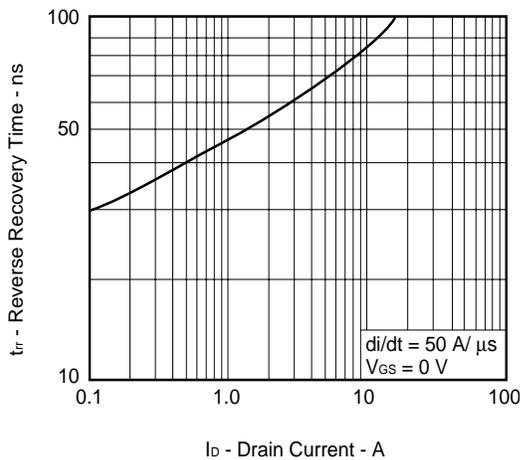
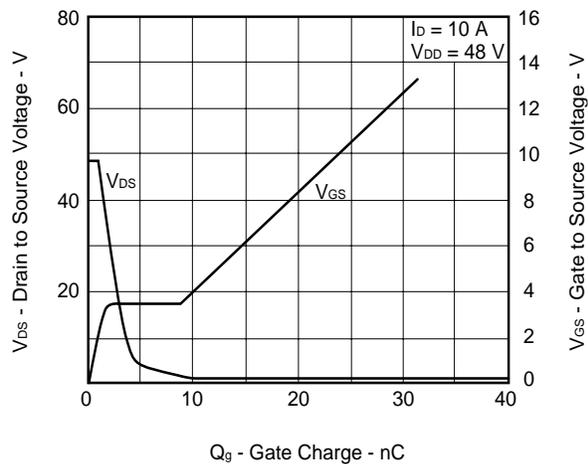
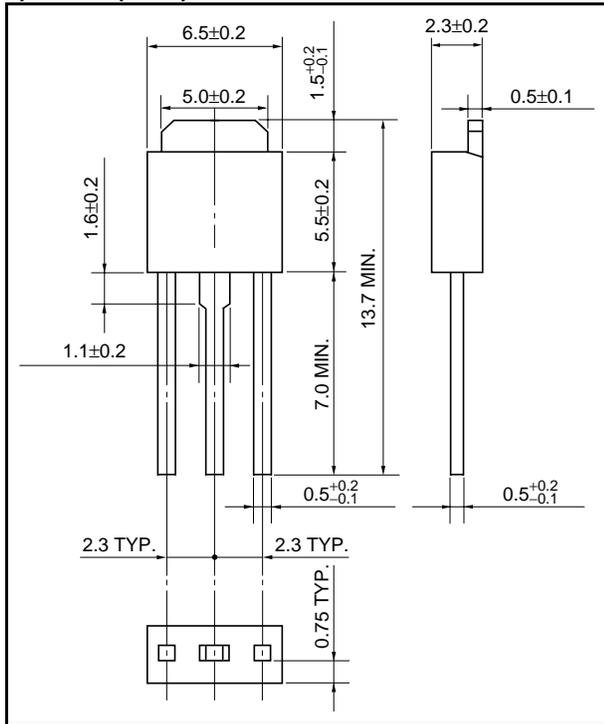


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

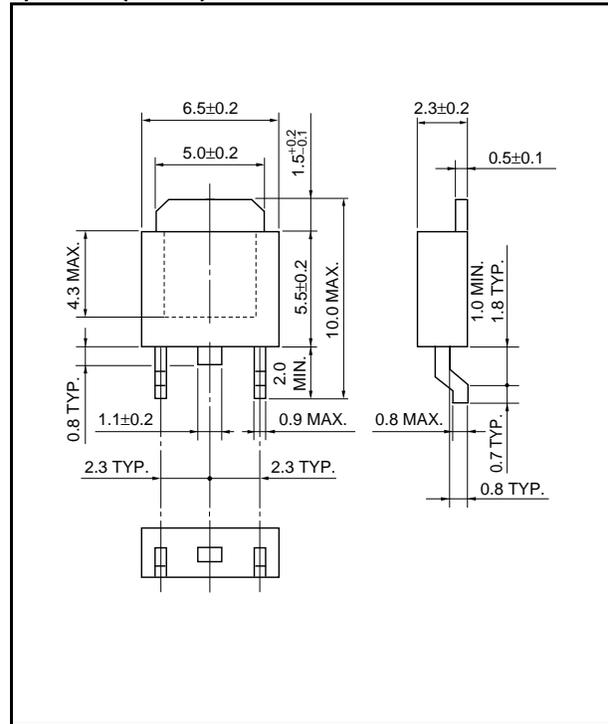


PACKAGE DRAWINGS (Unit: mm)

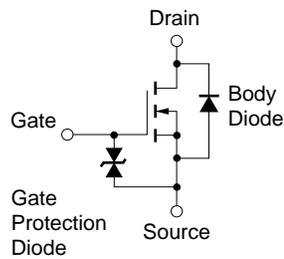
1)TO-251 (MP-3)



2)TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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